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# MS-7778 VER: 0A

uATX 9.6" x 9.6"

## CPU:

**AMD FM2**

## System Chipset:

**AMD - Hudson D3**

## On Board Chipset:

**Fintek Super I/O -- F71808A**

**LAN -- Atheros AR8161L**

**HD Codec -- IDT 92HD73E**

**BIOS -- SPI ROM 64M**

## Main Memory:

**DDR III X 4 (Max 16GB)**

## Expansion Slots:

**PCI Express X16 Slot \* 1**

**PCI Express X1 Slot \* 3**

**PCI Express X1 Slot \*1 for MINI CARD**

## PWM:

**Controller -- Intersil ISL6277**

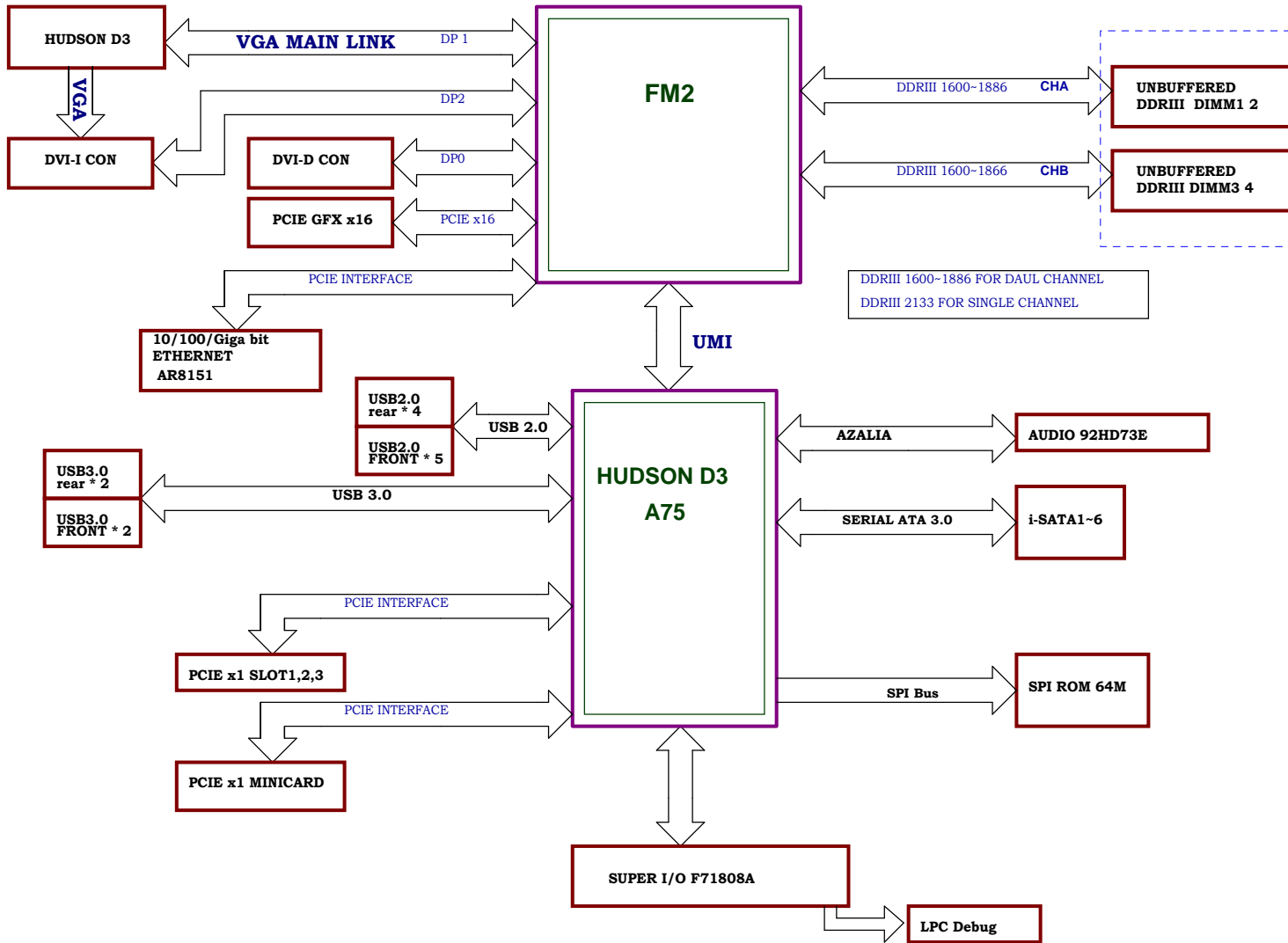


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**HP SCH P/N: (MSI MS-7778)**

Size Custom	Document Description <a href="#">Cover Sheet</a>	Rev 0A
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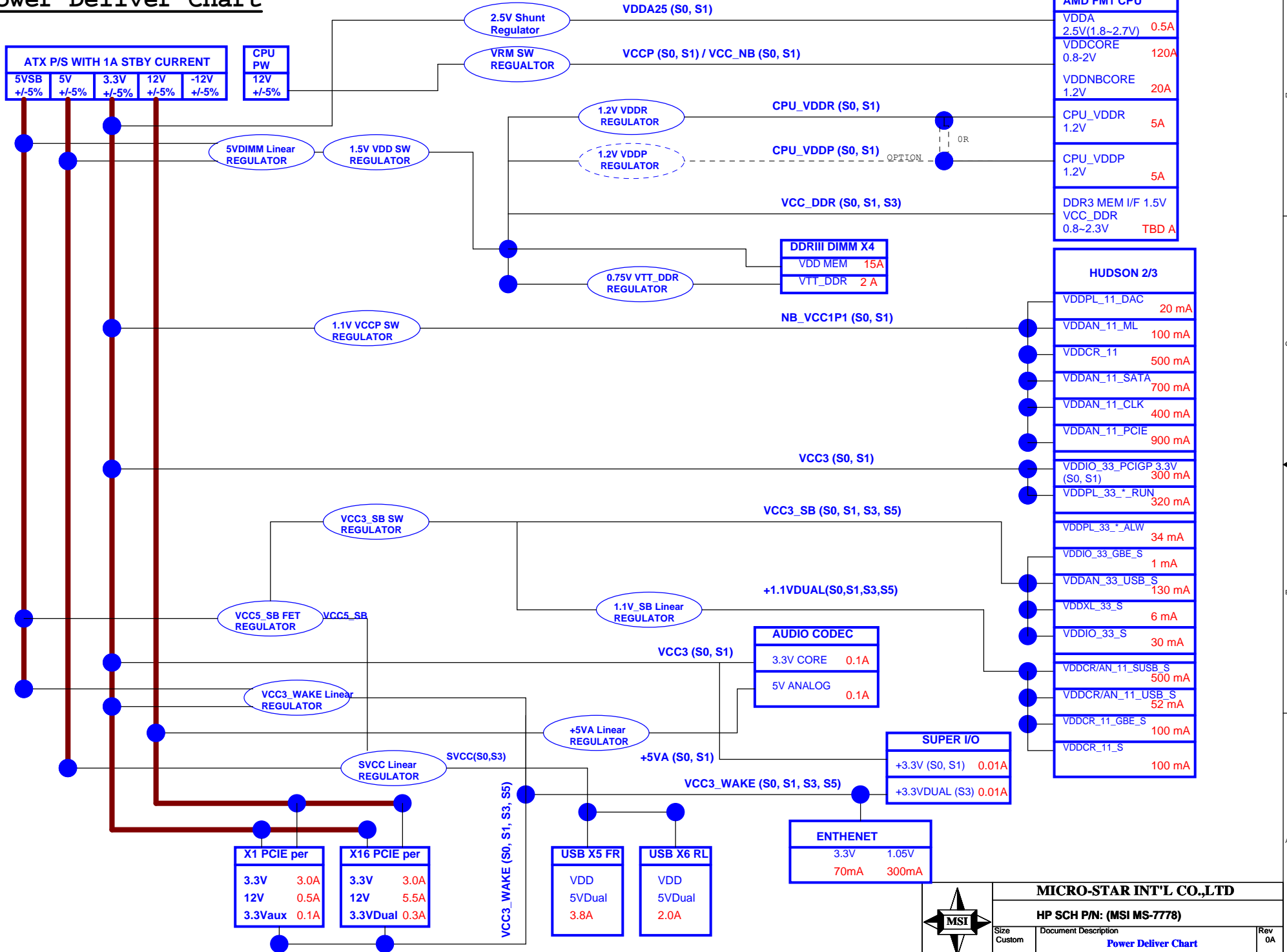
# FUSION BLOCK DIAGRAM



# Power Deliver Chart

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW
12V
+/-5%



AMD FM1 CPU		
VDDA	2.5V(1.8~2.7V)	0.5A
VDDCORE	0.8-2V	120A
VDDNBCORE	1.2V	20A
CPU_VDDR	1.2V	5A
CPU_VDDP	1.2V	5A
DDR3 MEM I/F 1.5V	VCC_DDR	0.8~2.3V
		TBD A

HUDSON 2/3		
VDDPL_11_DAC		20 mA
VDDAN_11_ML		100 mA
VDDCR_11		500 mA
VDDAN_11_SATA		700 mA
VDDAN_11_CLK		400 mA
VDDAN_11_PCIE		900 mA
VDDIO_33_PCIGP 3.3V (S0, S1)		300 mA
VDDPL_33*_RUN		320 mA
VDDPL_33*_ALW		34 mA
VDDIO_33_GBE_S		1 mA
VDDAN_33_USB_S		130 mA
VDDXL_33_S		6 mA
VDDIO_33_S		30 mA
VDDCR/AN_11_SUSB_S		500 mA
VDDCR/AN_11_USB_S		52 mA
VDDCR_11_GBE_S		100 mA
VDDCR_11_S		100 mA

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE per	
3.3V	3.0A
12V	5.5A
3.3VDual	0.3A

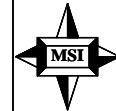
USB X5 FR	
VDD	
5VDual	3.8A

USB X6 RL	
VDD	
5VDual	2.0A

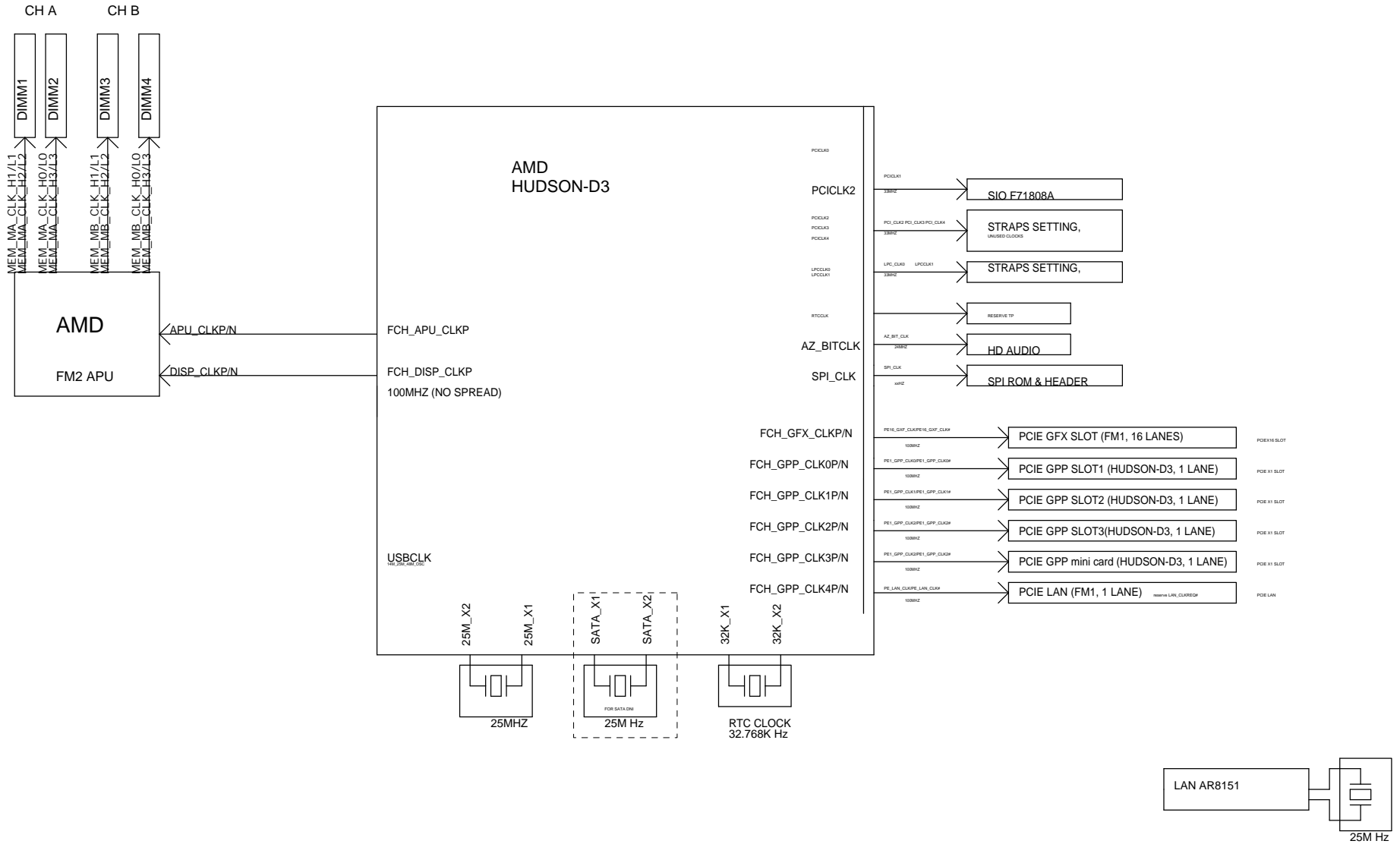
ETHERNET	
3.3V	1.05V
70mA	300mA

SUPER I/O	
+3.3V (S0, S1)	0.01A
+3.3VDUAL (S3)	0.01A

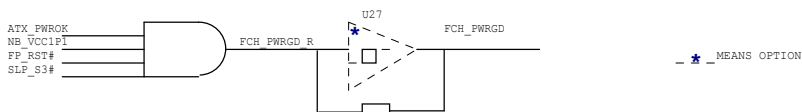
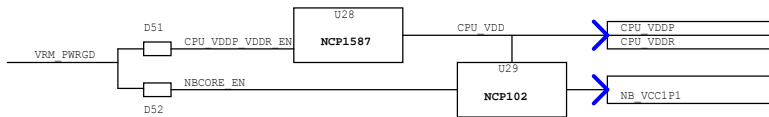
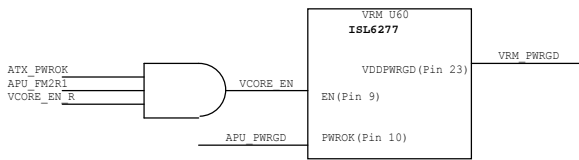
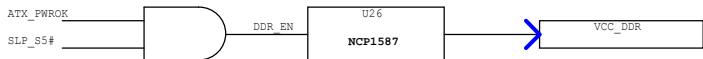
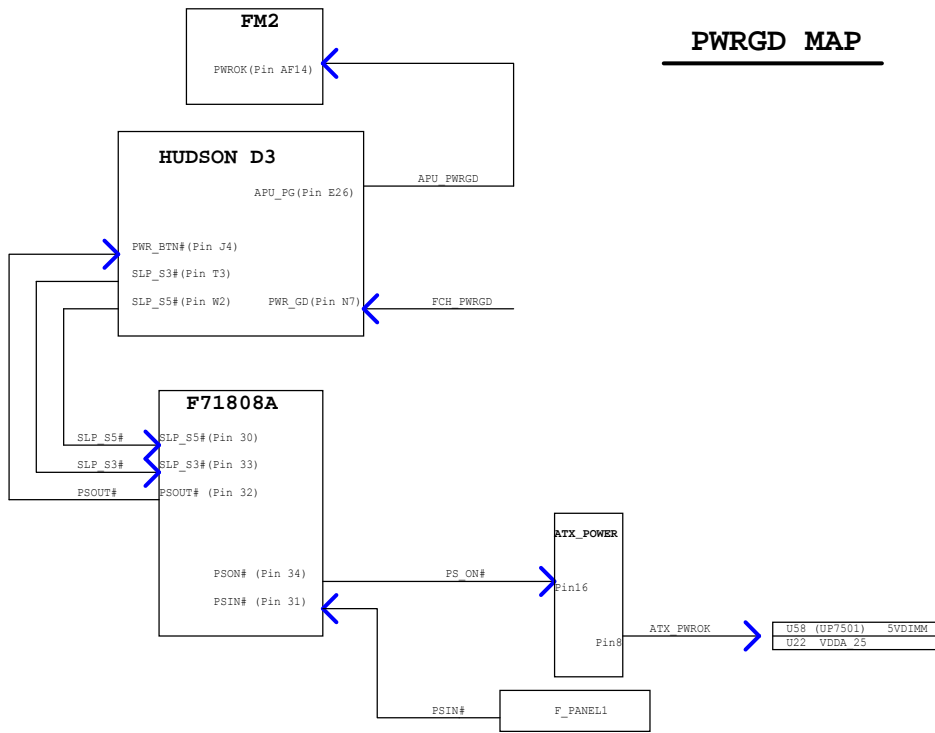
AUDIO CODEC	
3.3V CORE	0.1A
5V ANALOG	0.1A



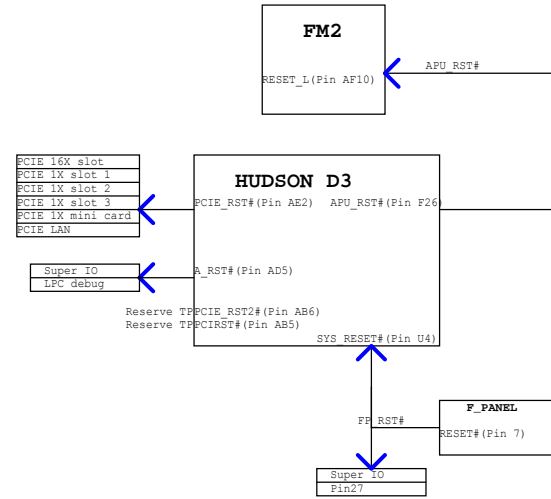
# INTERNAL CLOCK MODE



## PWRGD MAP



## RESET MAP



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Size Custom	Document Description <b>PWRGD&amp;RESET Map</b>	Rev 0A
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SUPER I/O F71808A GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
20	GP22	VSB	POP_MUTE	
22	LEDVSB/GP24	VSB	LED1	
23	LEDVCC/GP25	VSB	LED_SW	
26	GP67	VSB	DEEP_S5	
53	GP00	VSB	EN_LD	
54	GP01	VSB	EN_HP	
55	GP02	VSB	EN_UVP	
58	GP05	VSB	FDO	
60	GP07	VSB	F_AUDIO_DET#	

FCH HUDSON D3 GPIO Config

Name.	Pin.	Function Description.
GPIO0.	AJ3.	CLEAR CMOS.
GPIO1.	AL5.	WLAN PWRON.
GPIO2.	AG4.	USB20F1A.
GPIO3.	AL6.	USB20F1B.
GPIO4.	AH3.	USB20F2A.
GPIO5.	AJ5.	USB20F2B.
GPIO6.	AL1.	USB20F3.
GPIO7.	AN5.	USB30FA.
GPIO8.	AN6.	USB30FB.
GPIO12.	AM7.	HW_ID1.
GPIO13.	AJ6.	HW_ID2.
GPIO14.	AK7.	HW_ID3.
GPIO15.	AN8.	HW_ID4.
GPIO23.	AE21.	STRAPPING.
GPIO24.	AC12.	STRAPPING.
GPIO25.	AE13.	STRAPPING.
GPIO26.	AF13.	STRAPPING.
GPIO27.	AH13.	STRAPPING.
GPIO36.	AF1.	STRAPPING.
GPIO38.	AG2.	STRAPPING.
GPIO39.	AF6.	STRAPPING.
GPIO42.	AM17.	STRAPPING.
GPIO43.	AD26.	SMBus Clock 0.
GPIO46.	AK17.	STRAPPING.
GPIO47.	AD25.	SMBus Data 0.
GPIO52.	AH16.	STRAPPING.
GPIO67.	AD22.	SATA_LED.
GPIO162.	V3.	SPI Clock.
GPIO163.	V5.	SPI Data Out.
GPIO164.	V6.	SPI Data In.
GPIO165.	T6.	SPI Chip Select 1.
GPIO170.	Y1.	HD Audio Serial Data.
GPIO181.	M1.	LAN_ISOLATEB.
GPIO199.	J22.	STRAPPING.

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-A	10100010B A4H	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H3/L3
DIMM 3 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H3/L3

SMBus TABLE

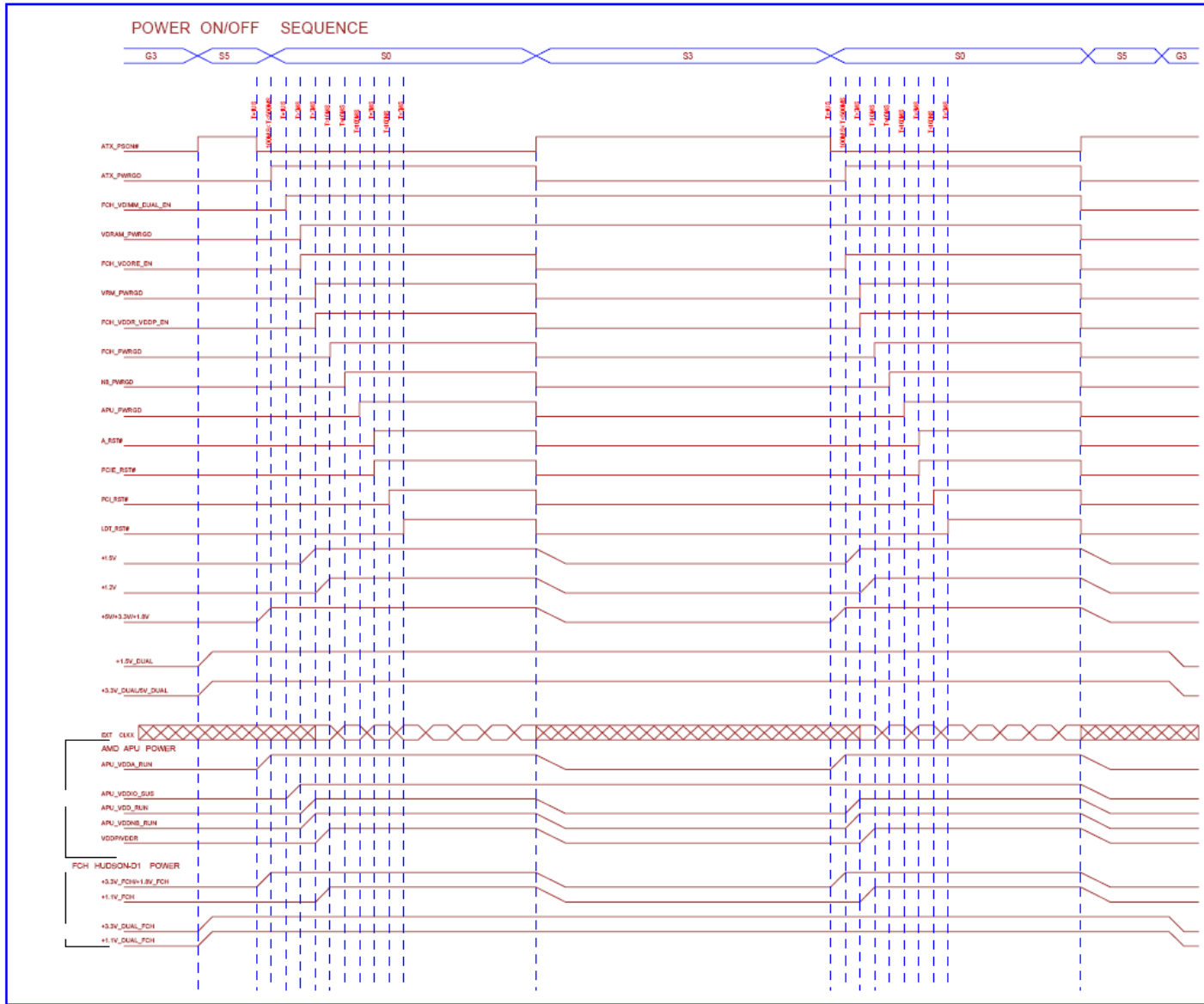
SOURCE	SINGLE NAME	LINKED DEVICE
APU	DPO_AUXP_C /DPO_AUXN_C	DVI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,CLOCK GEN ,SIO
	SCLK1/SDATA1	LAN,PCIE SLOTS,MINI_PCIE
	SCLK3/SDATA3	TP

RESET TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCIe 16X,1X,LAN,MINI_PCIE
	A_RST#	SIO,LPC debug
	PCIE_RST2#	RESERVE TP
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
	FRONT PANEL	FP_RST#



# POWER ON SEQUENCE



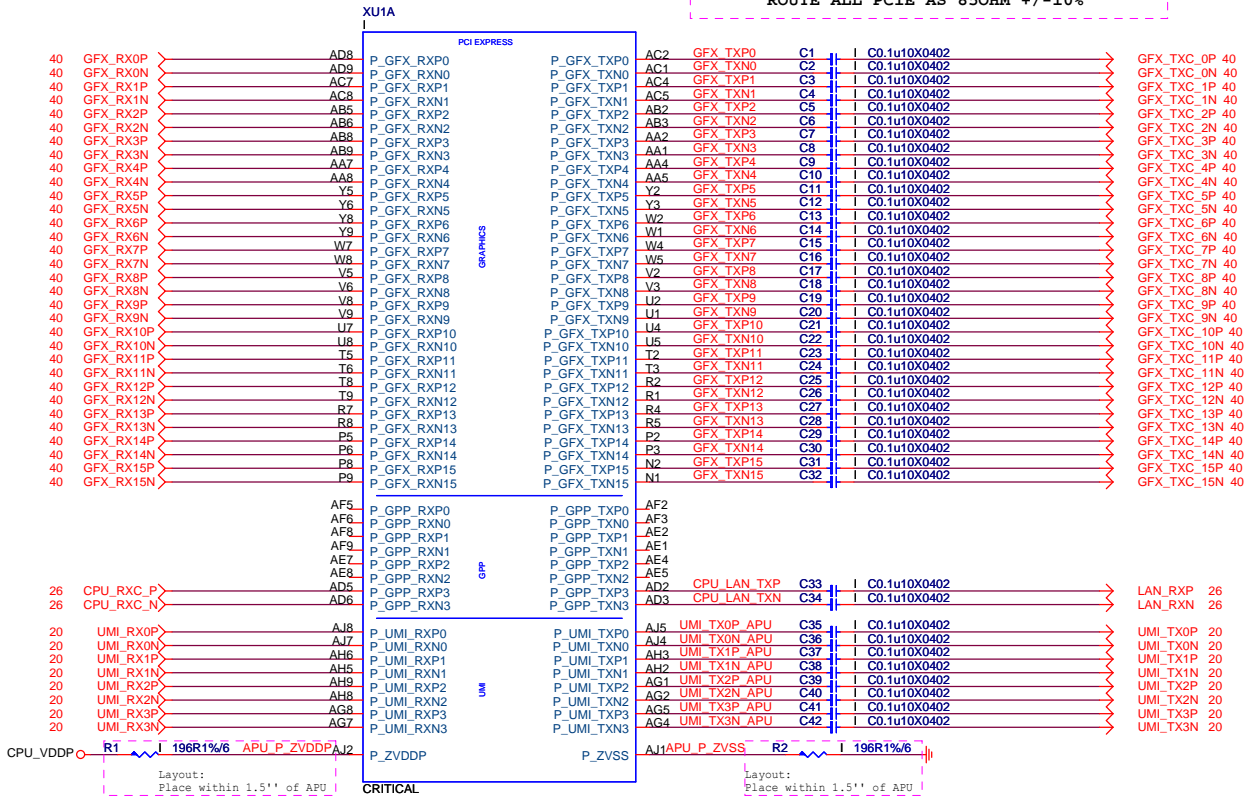
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

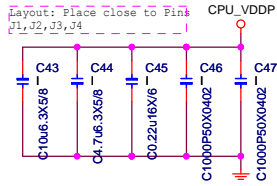
Size Custom	Document Description <b>POWER ON SEQUENCE</b>	Rev 0A
Date:	Sheet 7 of 45	

**FM2 PCIE I/F**

**mach@CRB PCIE AC Capacitors:75nF to 200nF**  
**Layout: PLACE CAPS WITH APU < 1 INCH**  
**ROUTE ALL PCIE AS 85OHM +/-10%**



**N12-9040030-F02**



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Size Custom	Document Description	Rev 0A
	<b>FM2 PCIE I/F</b>	
Date:		Sheet 8 of 45



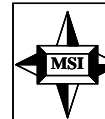
14,15 MEM\_MA\_DQS\_L[7..0] ↔  
 14,15 MEM\_MA\_DQS\_H[7..0] ↔  
 14,15 MEM\_MA\_DM[7..0] ←

MEM\_MA\_DATA[63..0] 14,15 ↔

XU1B



CRITICAL  
 ZIF-SOCKET904-HF N12-9040030-F02

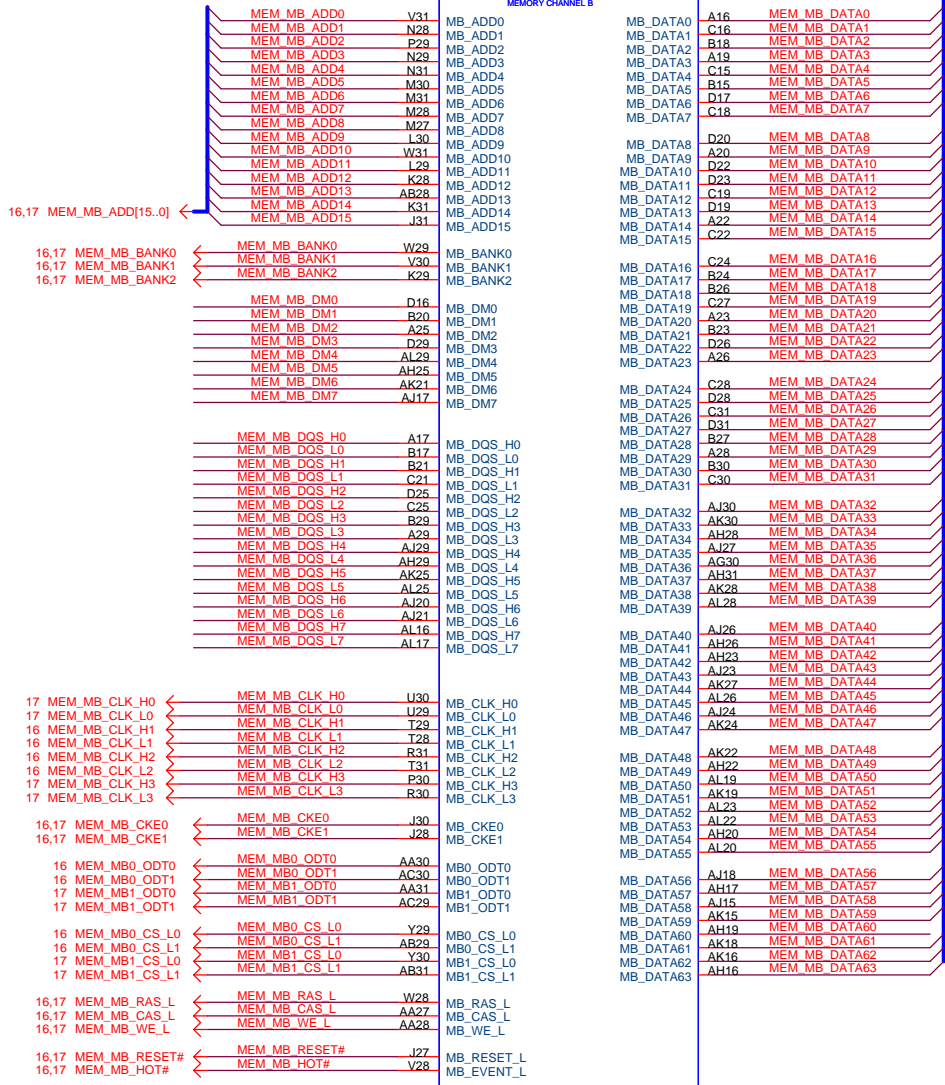


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>FM2 DDR3 I/F(A)</b>	Rev 0A
Date:	Sheet 9 of 45	

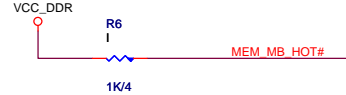
16,17 MEM\_MB\_DQS\_L[7..0] ←  
 16,17 MEM\_MB\_DQS\_H[7..0] ←  
 16,17 MEM\_MB\_DM[7..0] ←

XU1C

MEMORY CHANNEL B



MEM\_MB\_DATA[63..0] 16,17



CRITICAL  
 ZIF-SOCKET904-HF  
**N12-9040030-F02**

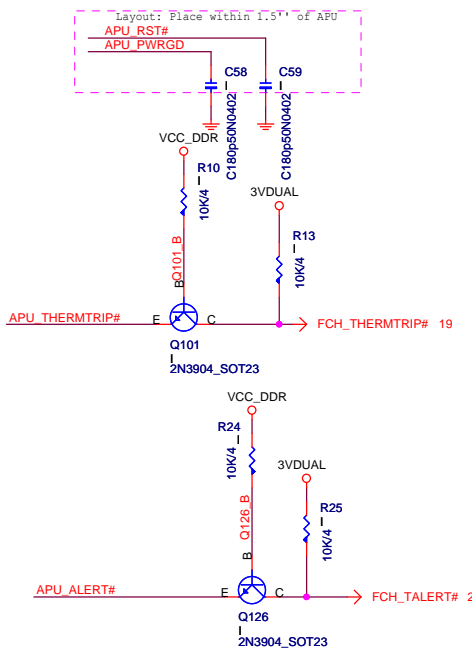


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>FM2 DDR3 I/F(B)</b>	Rev 0A
Date:	Sheet 10 of 45	

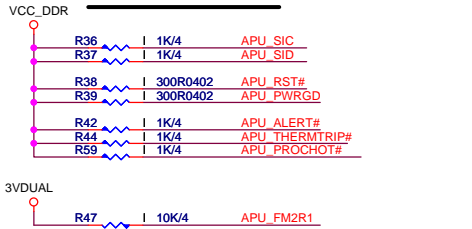
# FM1 DISPLAY I/F

Note: Several vias on the DP0 interface violate the minimum distance rules for via to via spacing between diff pairs. These violations have been reviewed and approved on an individual basis, and pose no significant signal integrity issues for this implementation since the route lengths are under the maximum allowed spec, and the via distance violations are not severe.

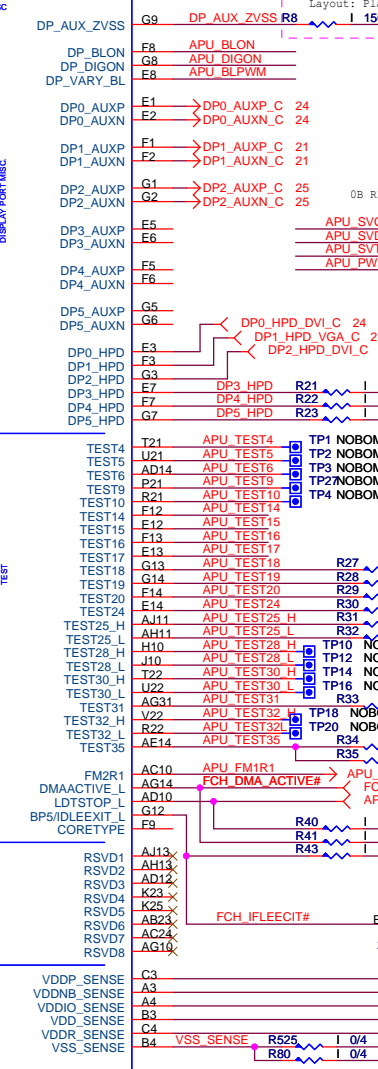
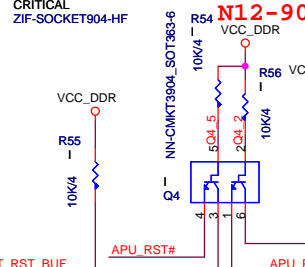
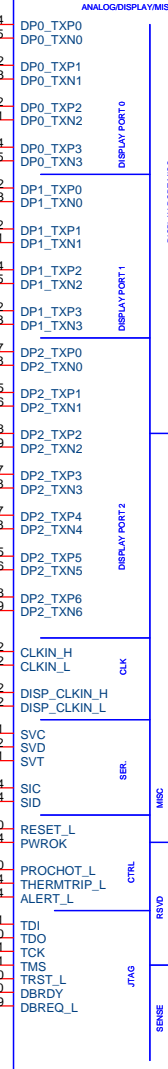
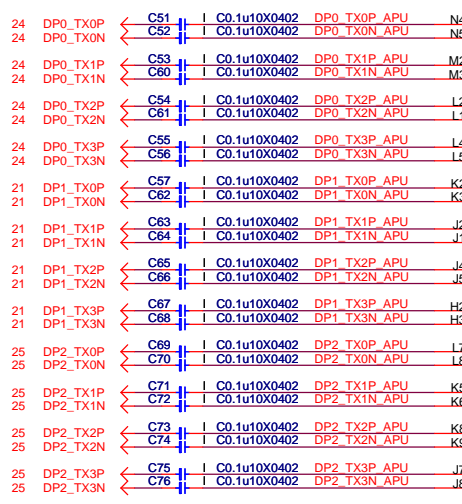
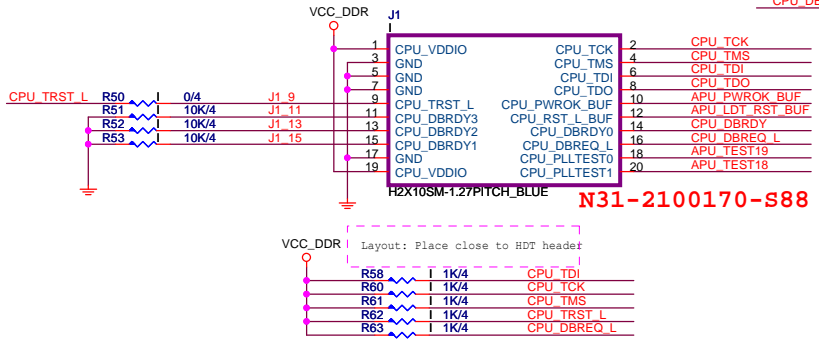
ROUTE PCIE AS 850HM +/-10%  
PLACE CAPS WITH APU < 1 INCH  
Trace length within 10"



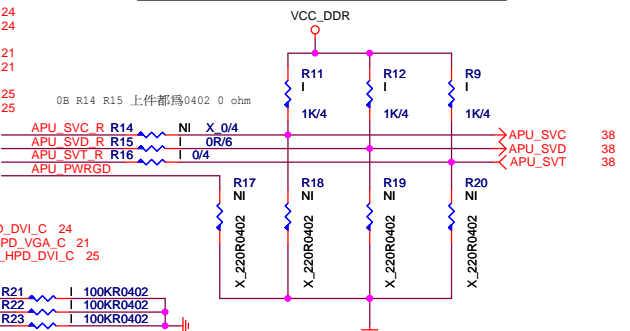
## PULL UP



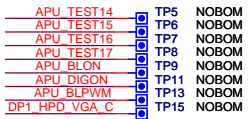
## HDT+ Connector



## VID OVERRIDE CIRCUIT



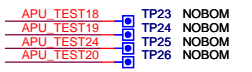
## GPU DEBUG



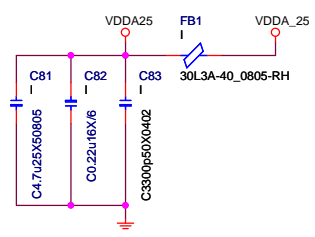
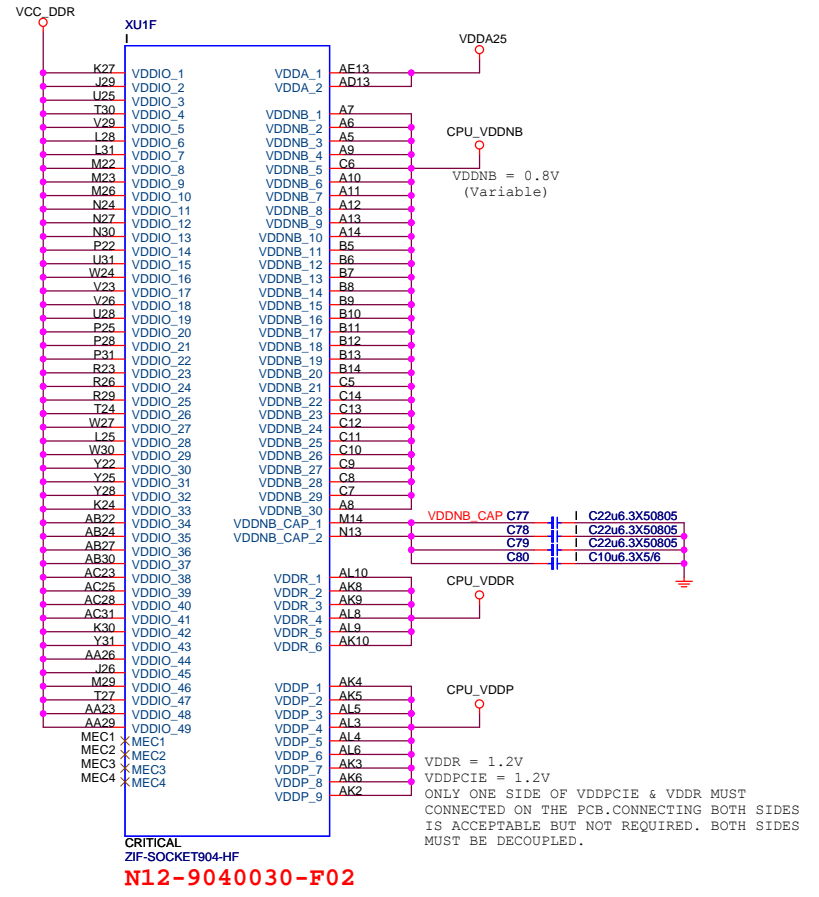
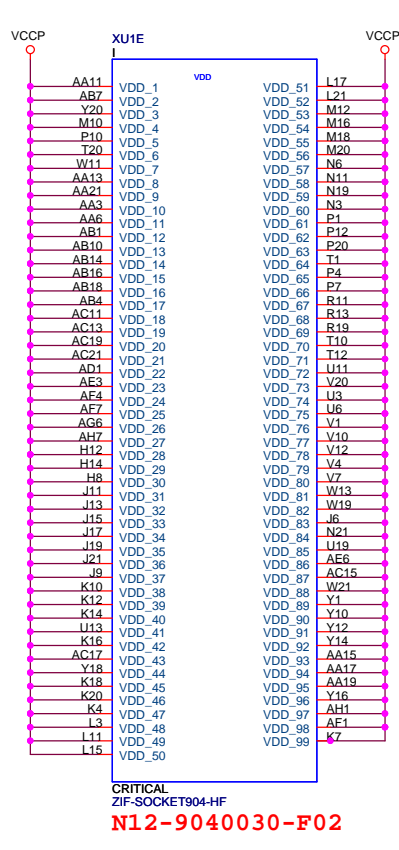
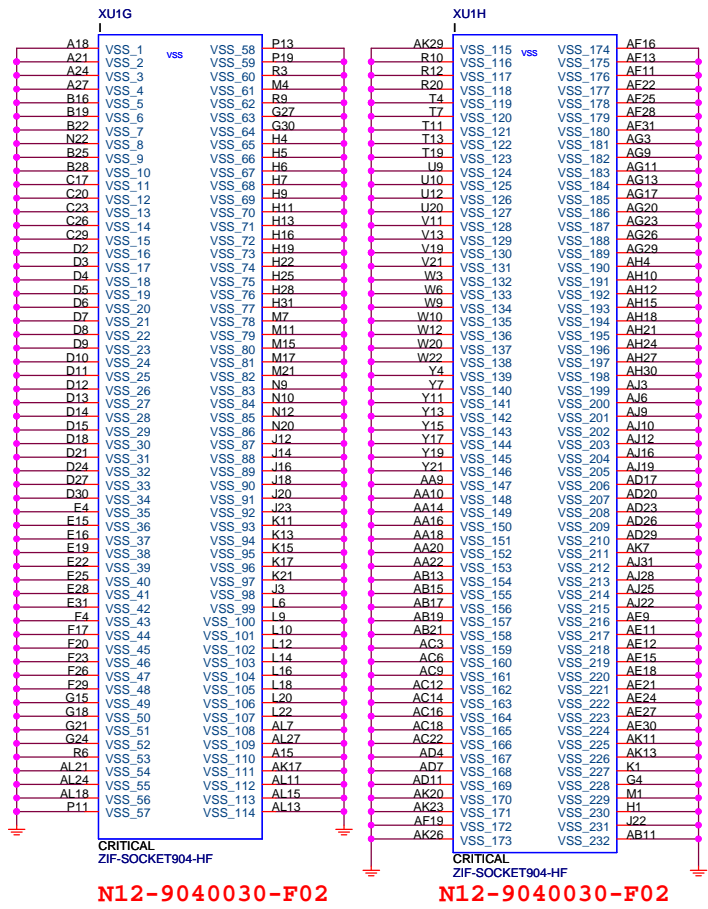
## WARM RESET



## SCAN Conn,

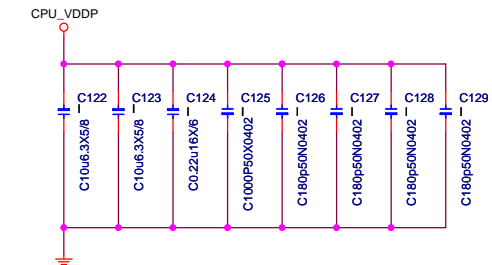
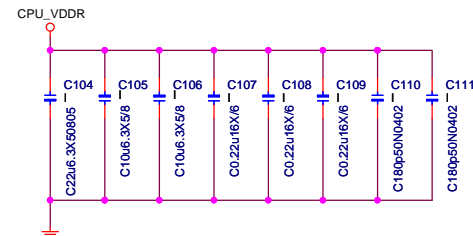
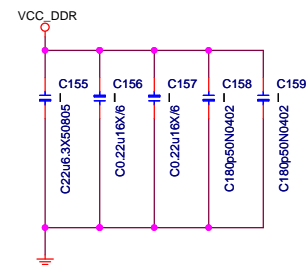
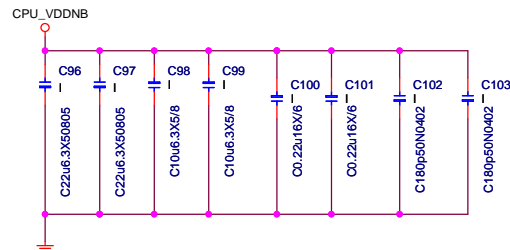
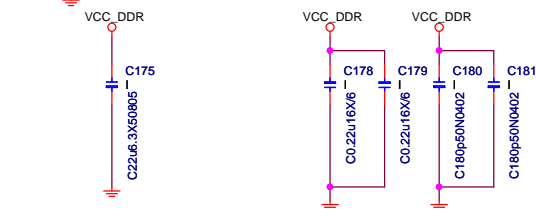
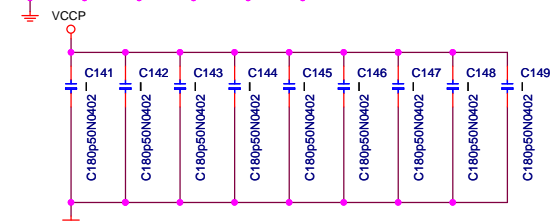
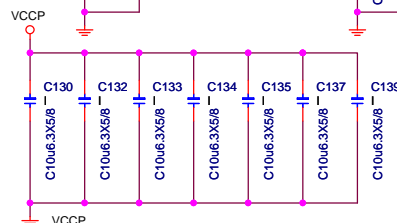
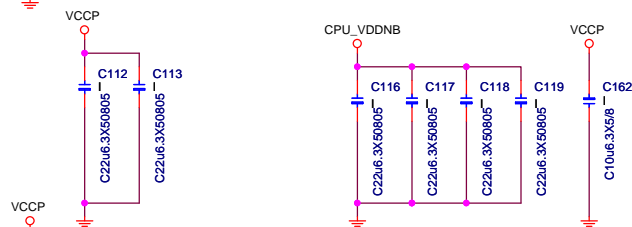
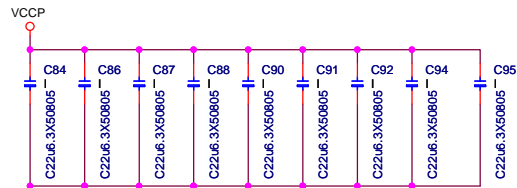


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 Size Custom Document Description  
**FM2 DISPLAY/MSIC**  
 Rev 0A  
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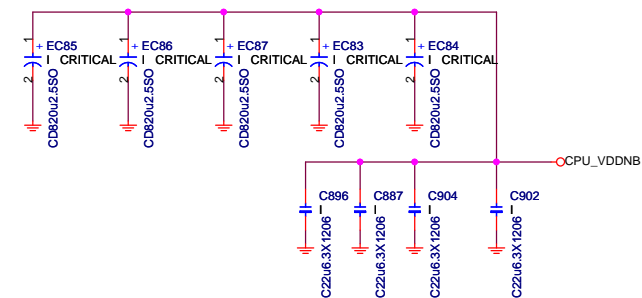
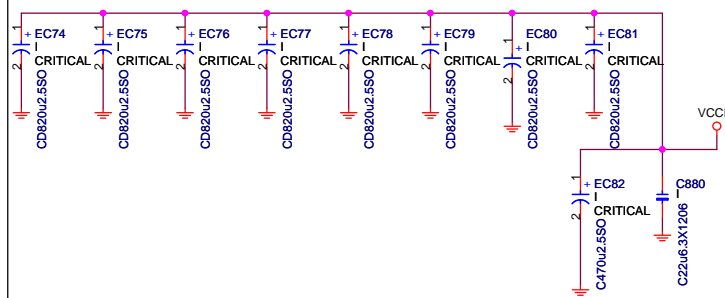


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>HP SCH P/N: (MSI MS-7778)</b>			
Size Custom	Document Description <b>FM2 POWER/GND</b>		Rev 0A
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Sheet 12 of 45			

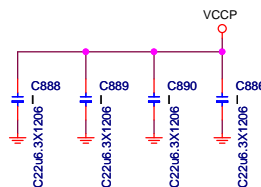
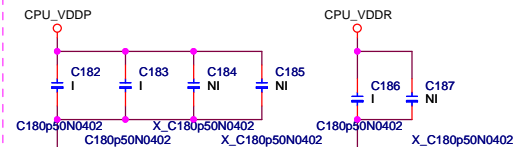
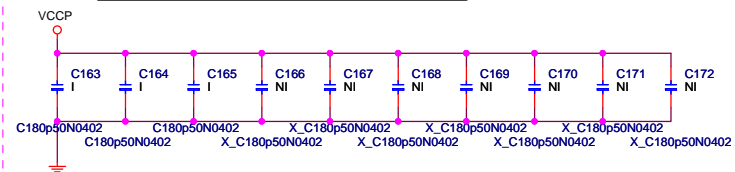
# CPU POWER CAPS



# VCORE CAPS



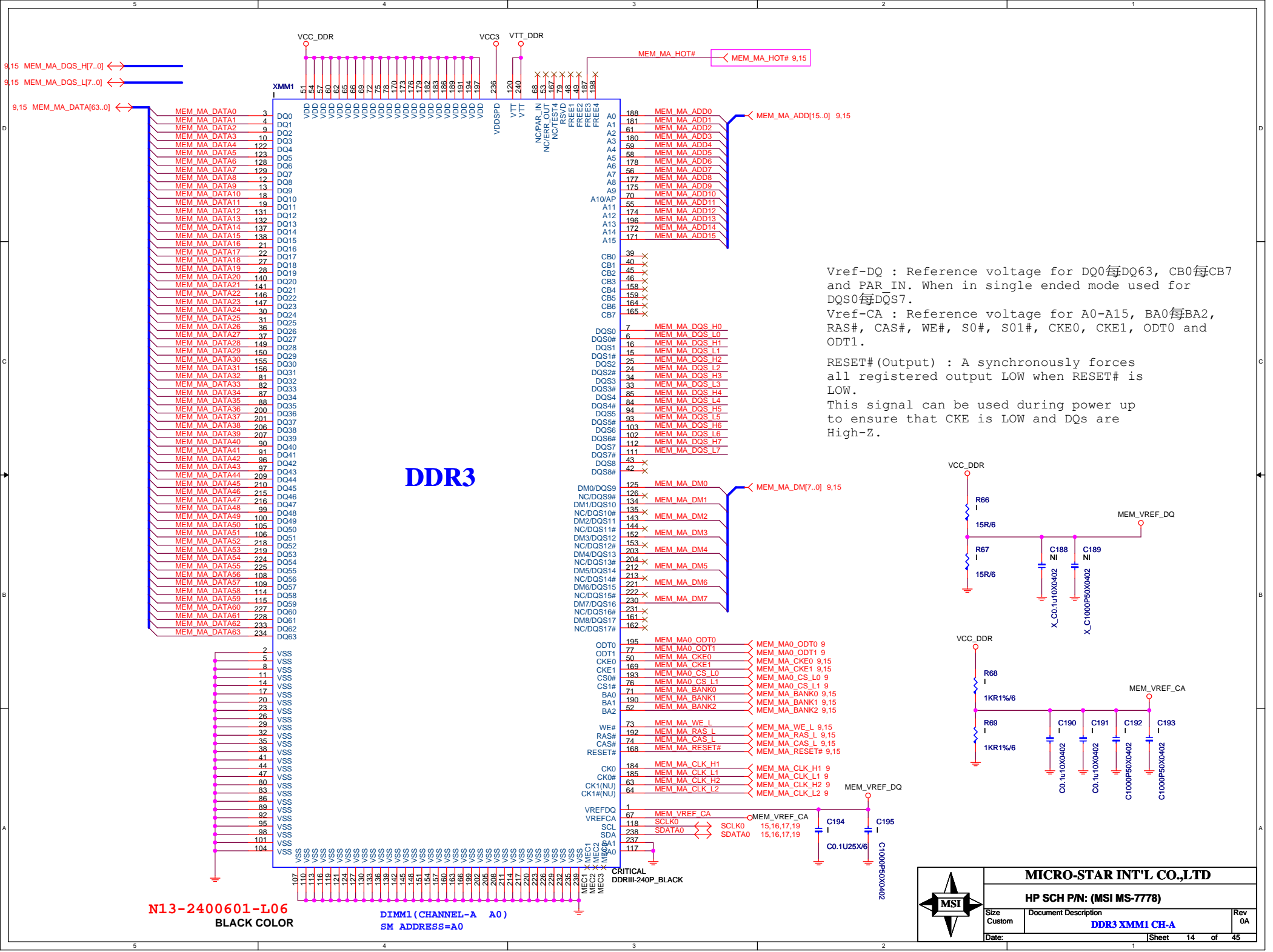
# EMC Caps On Bottom side



MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

Size Custom	Document Description	Rev 0A
FM2 CAPS & VCORE CAP		



# DDR3

Vref-DQ : Reference voltage for DQ0每DQ63, CB0每CB7 and PAR IN. When in single ended mode used for DQS0每DQS7.

Vref-CA : Reference voltage for A0-A15, BA0每BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

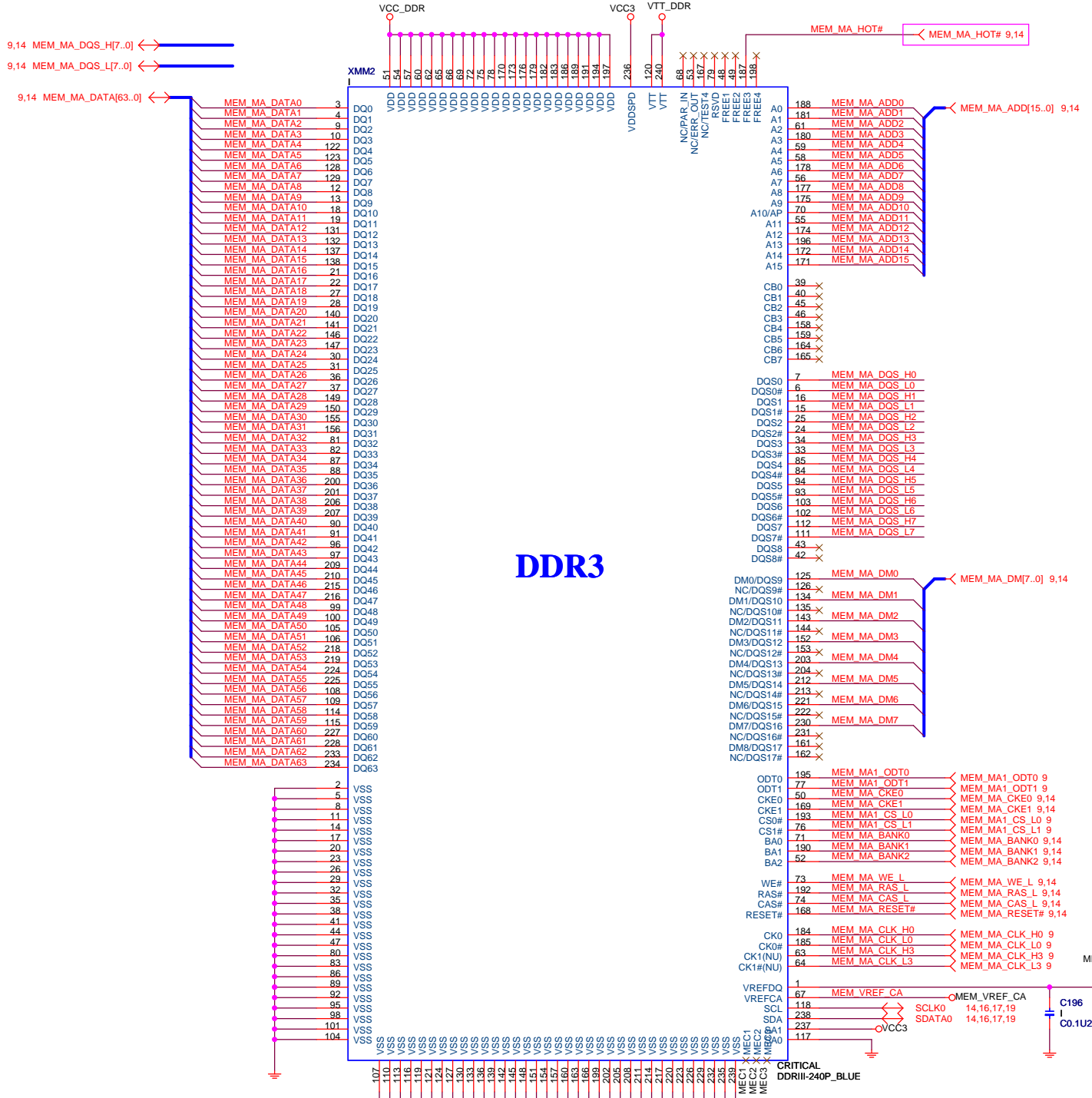
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

N13-2400601-L06  
BLACK COLOR

DIMM1 (CHANNEL-A A0)  
SM ADDRESS=A0



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>DDR3 XMM1 CH-A</b>	Rev 0A
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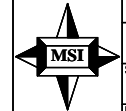


### DDR3

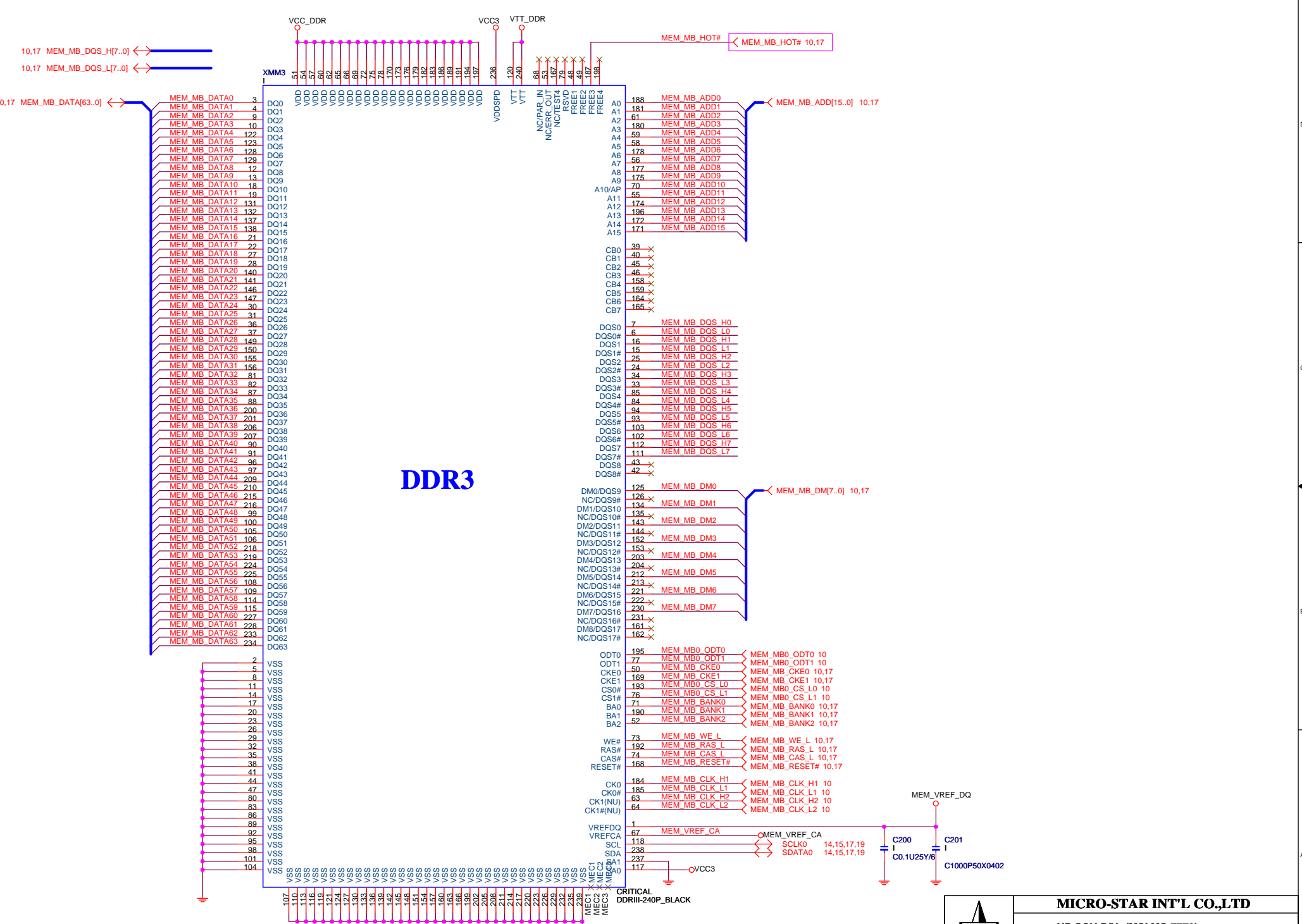
**N13-2400921-I.06**  
BLUE COLOR

DI MM2 (CHANNEL-A A1)  
SM ADDRESS=A4

CRITICAL  
DDRIII-240P\_BLUE



<b>MICRO-STAR INT'L CO.,LTD</b>	
<b>HP SCH P/N: (MSI MS-7778)</b>	
Size Custom	Document Description
<b>DDR3 XMM2 CH-A</b>	
Date:	Rev 0A



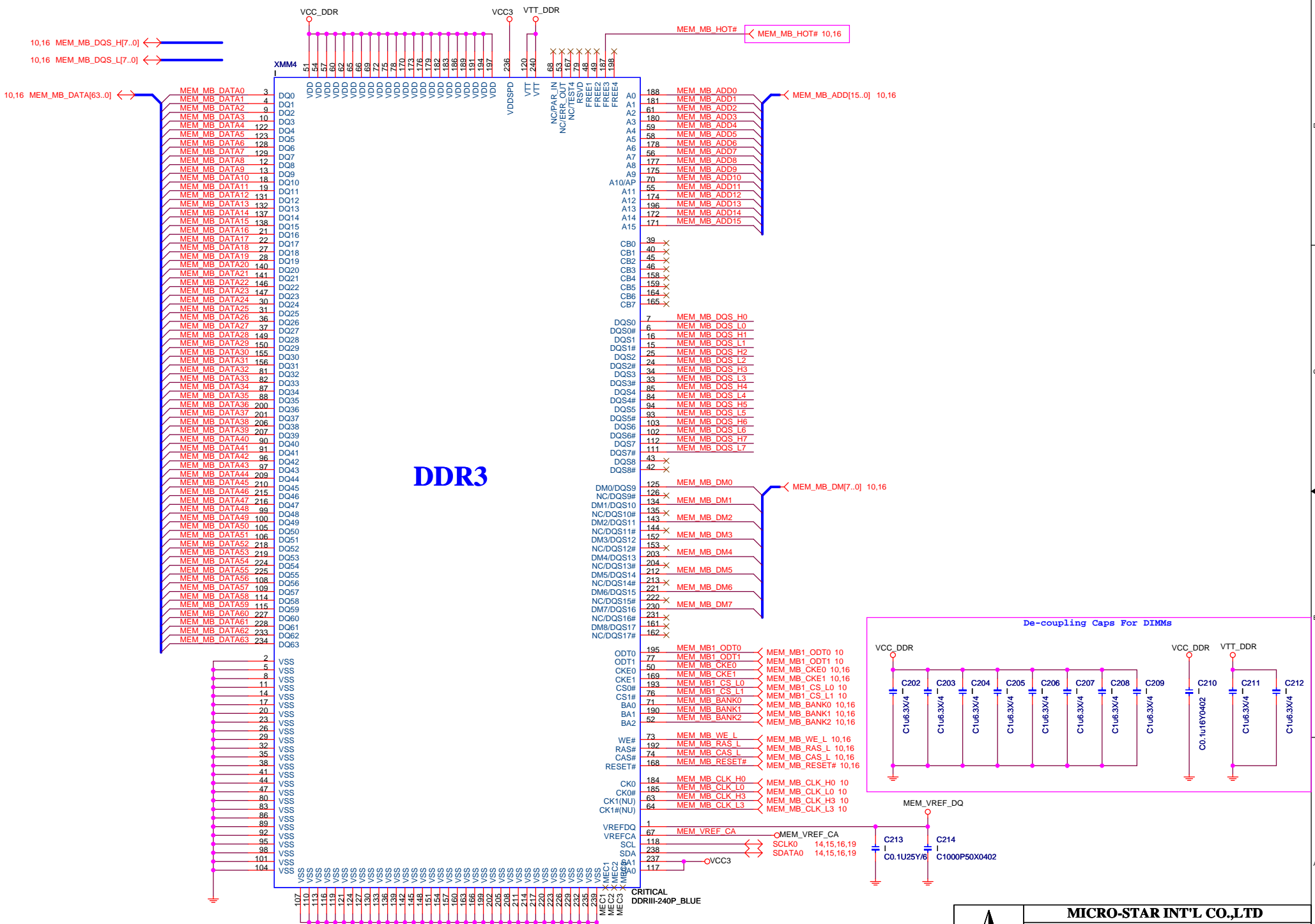
**N13-2400601-I.06**  
BLACK COLOR

**DIMM3 (CHANNEL-B B0)**  
SM ADDRESS=A2



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description	Rev 0A
<b>DDR3 XMM3 CH-B</b>		
Date:	Sheet 16	of 45





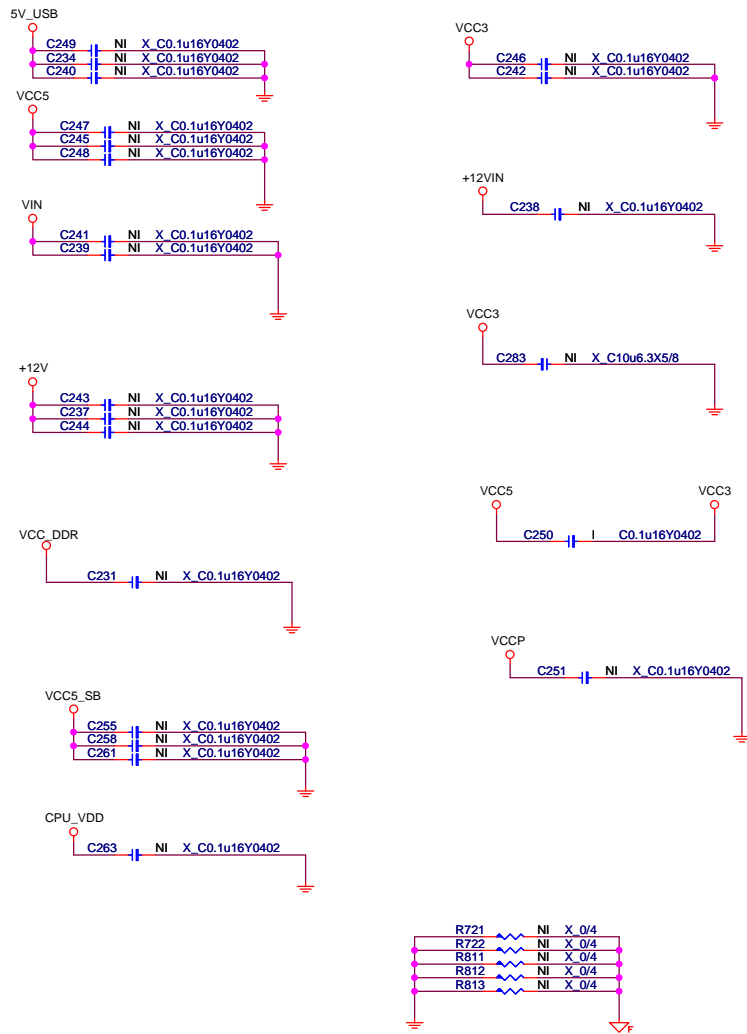
**N13-2400921-F02**  
**BLUE COLOR**

**DIMM4 (CHANNEL-B B1)**  
**SM ADDRESS=A6**



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>DDR3 XMM4 CH-B/Cap For DIMM</b>	Rev 0A
Date:	Sheet 17	of 45

# EMI Reserved



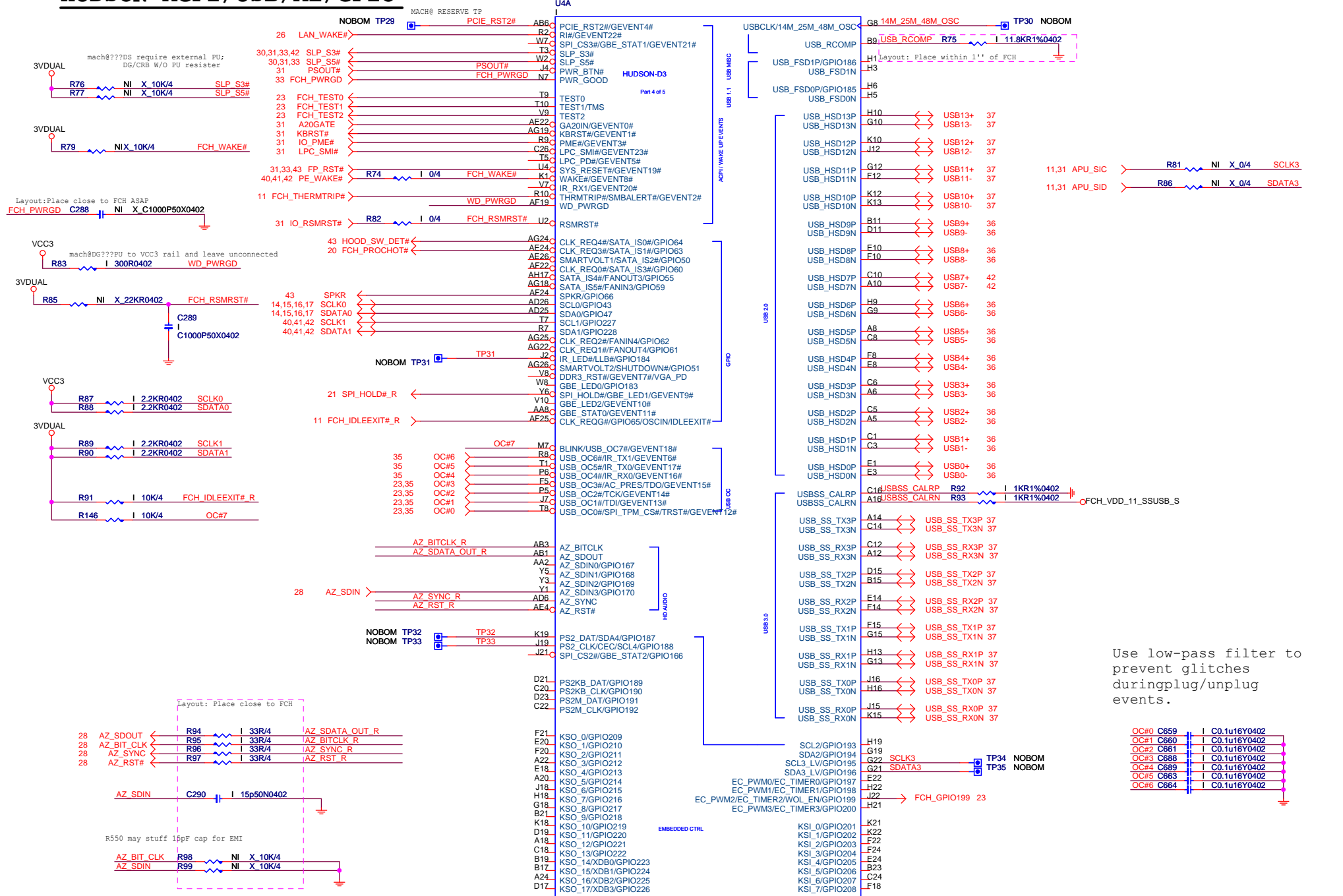
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

Size Custom	Document Description <b>EMI Reserved</b>	Rev 0A
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Date: Sheet 18 of 45

HUDSON ACPI/USB/AZ/GPIO



Use low-pass filter to prevent glitches during plug/unplug events.

- OC#0 C659 | I C0.1u16Y0402
- OC#1 C660 | I C0.1u16Y0402
- OC#2 C661 | I C0.1u16Y0402
- OC#3 C658 | I C0.1u16Y0402
- OC#4 C659 | I C0.1u16Y0402
- OC#5 C663 | I C0.1u16Y0402
- OC#6 C664 | I C0.1u16Y0402



**MICRO-STAR INT'L CO.,LTD**

**HP SCH P/N: (MSI MS-7778)**

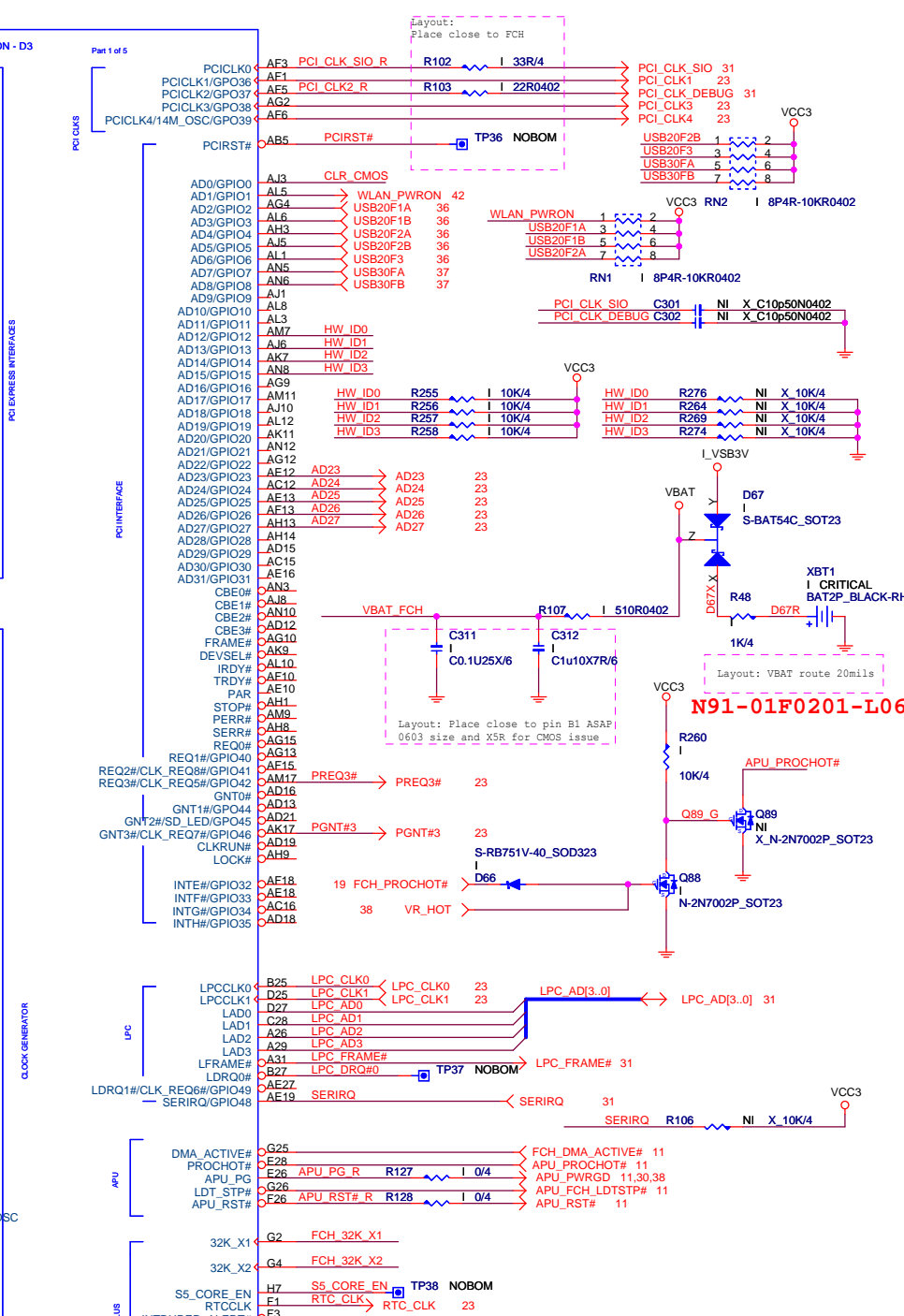
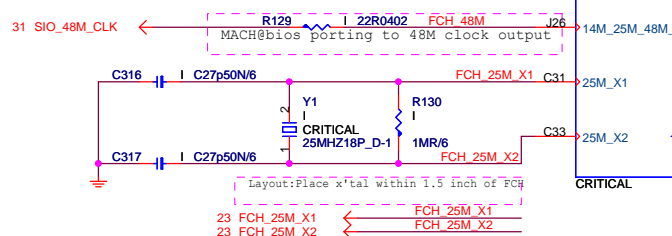
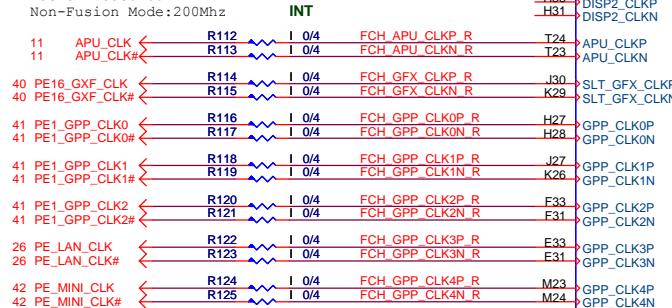
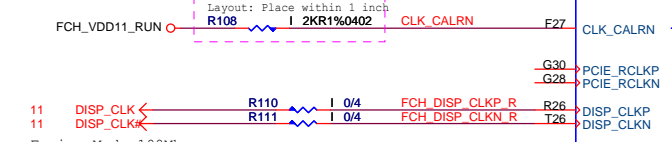
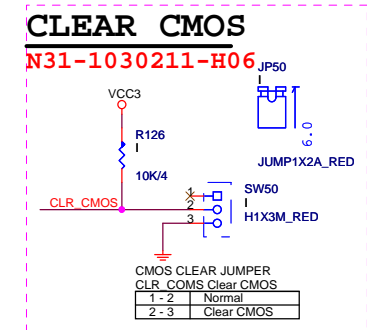
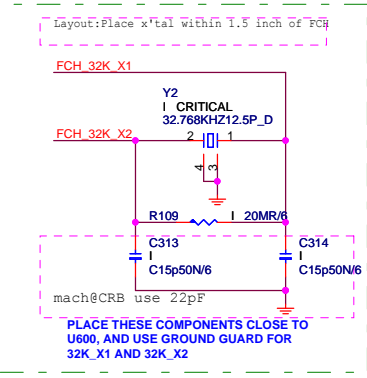
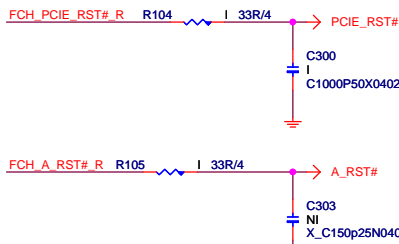
Size Custom	Document Description	Rev 0A
<b>HUDSON ACPI/USB/AZ/GPIO</b>		
Date:	Sheet 19	of 45

B01-21807B5-AX8

CRITICAL AMD-218-0755044-A13-RH

# HUDSON PCIE/PCI/APU/LPC/CLK

A\_RST# for LPC device:  
PCIE\_RST# for APU PCIE device:  
PCIE\_RST#2 FCH PCIE device



B01-21807B5-AX8



**MICRO-STAR INT'L CO.,LTD**

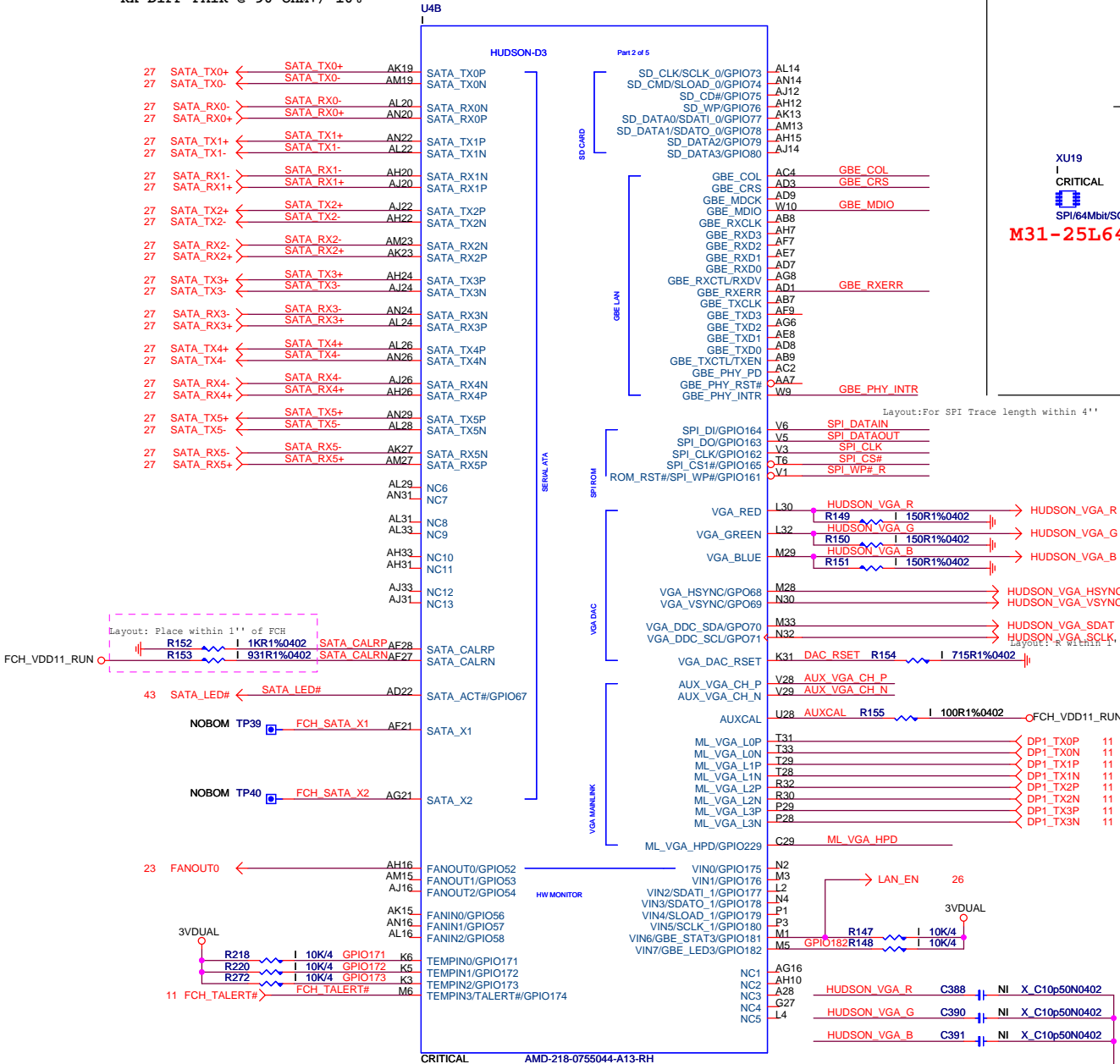
**HP SCH P/N: (MSI MS-7778)**

Size Custom Document Description **HUDSON PCIE/PCI/APU/LPC/CLK** Rev 0A

Date: \_\_\_\_\_ Sheet 20 of 45

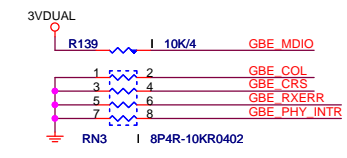
**HUDSON SATA/VGA/SPI/HWM**

LAYOUT:  
 ROUTE SATA TX DIFF PAIR @ 100 OHM+/-10%  
 RX DIFF PAIR @ 90 OHM+/-10%

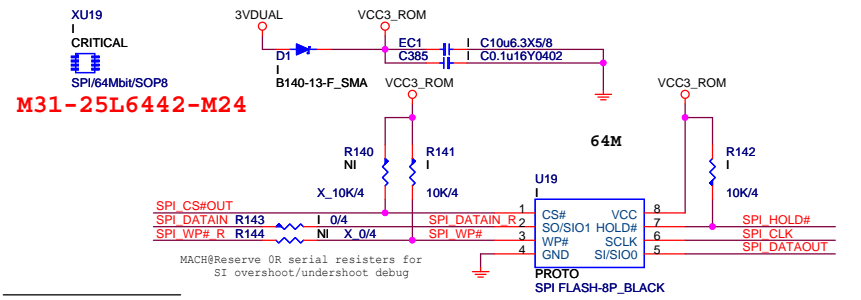


**B01-21807B5-AX8**

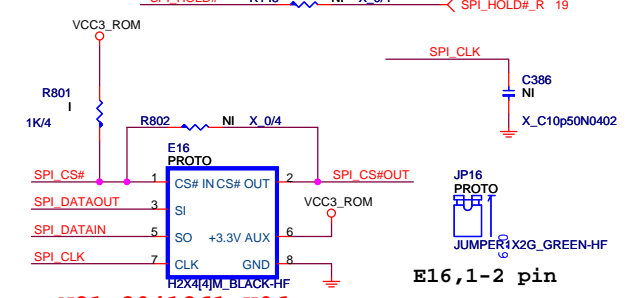
**GBE NOT ENABLED**



**SPI ROM & DEBUG HEADER**

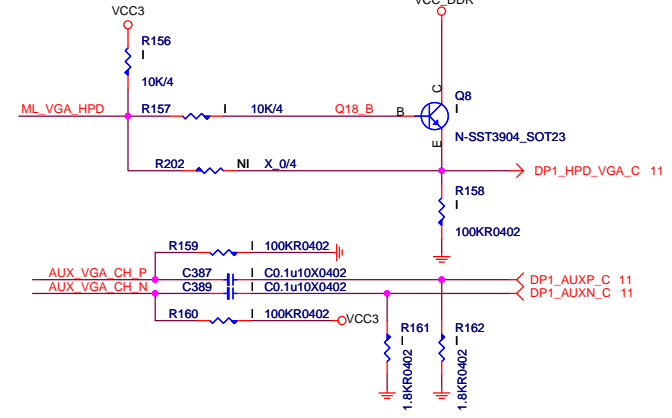


**N14-0080030-L06**



**N31-2041261-H06**

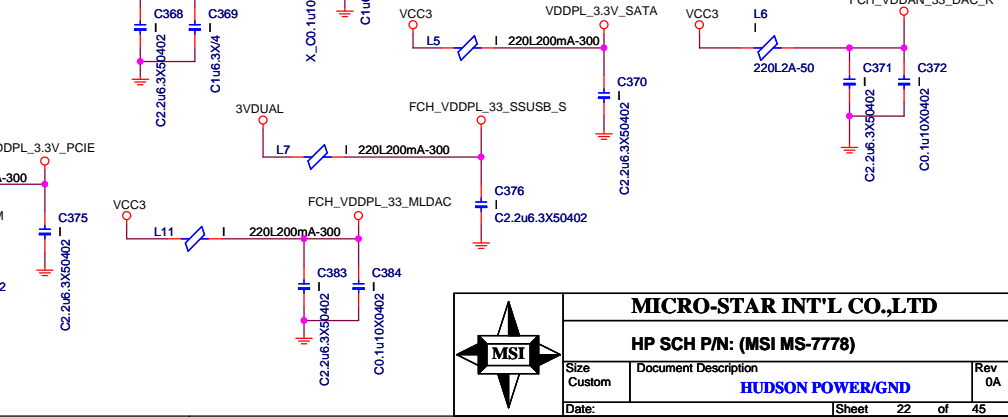
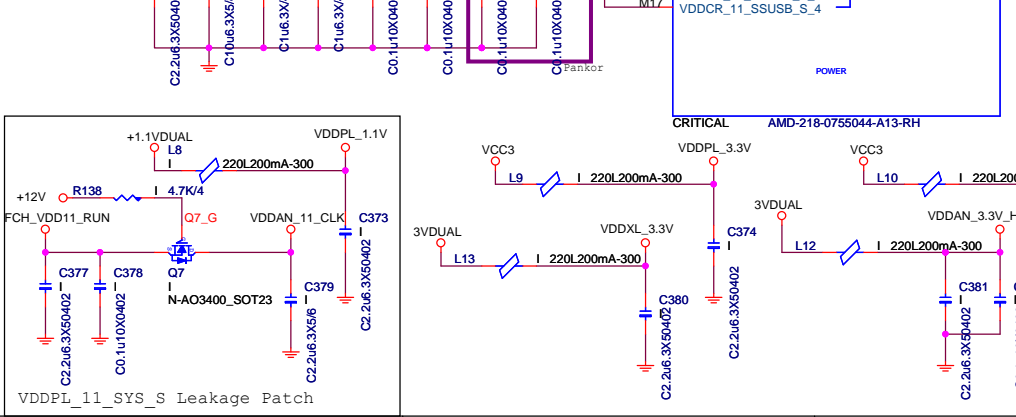
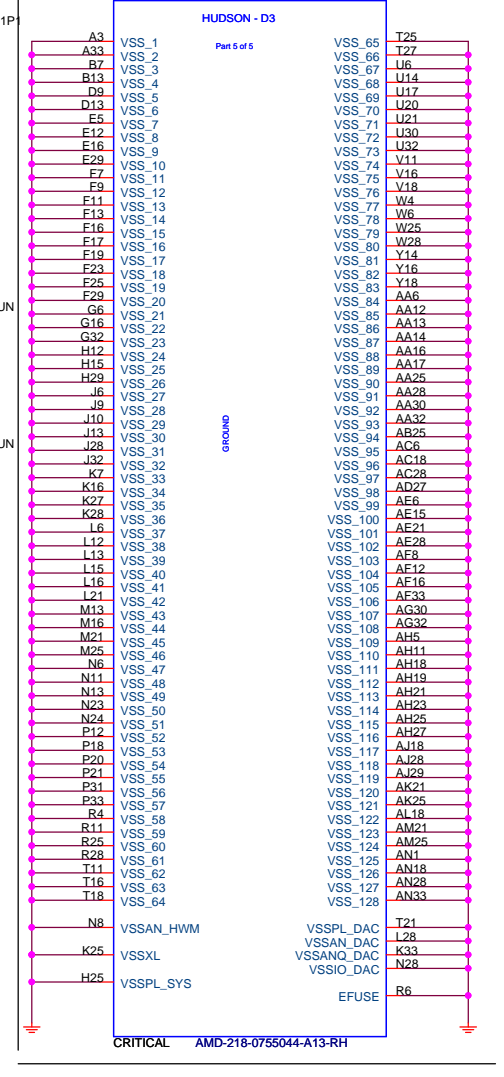
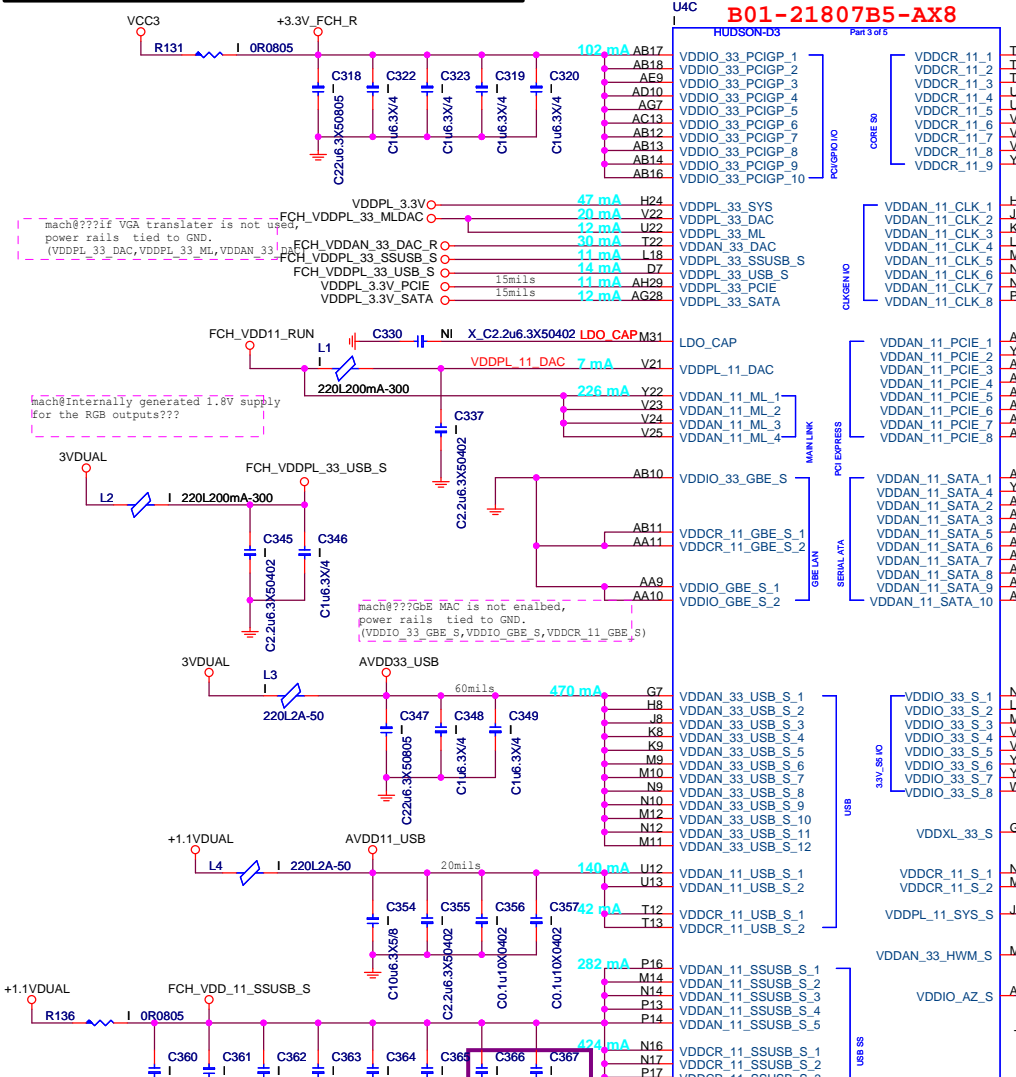
**VGA HWP**



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>HUDSON SATA/VGA/HWM/SPI</b>	Rev 0A
Date:		Sheet 21 of 45

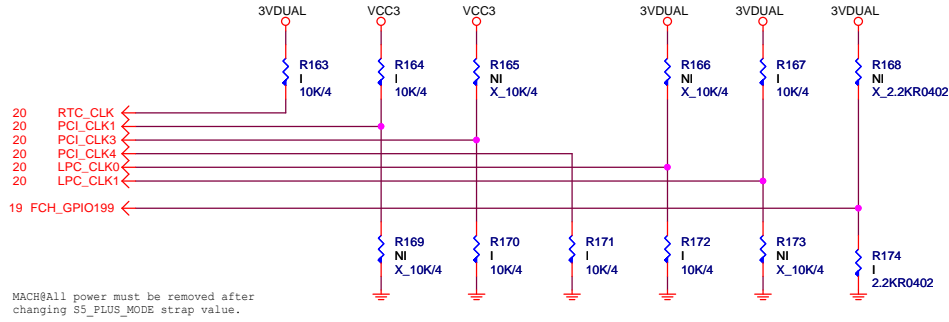
# HUDSON POWER&DECOUPLING

Connected directly to the power plane with width = 100 mils with area fill under the PCH.



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>HUDSON POWER/GND</b>	Rev 0A
Date:	Sheet	22 of 45

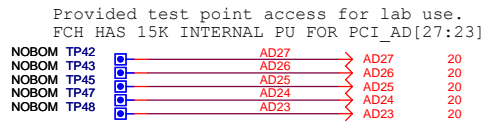
# FCH REQUIRED STRAPS



MACH#All power must be removed after changing S5\_PLUS\_MODE strap value.

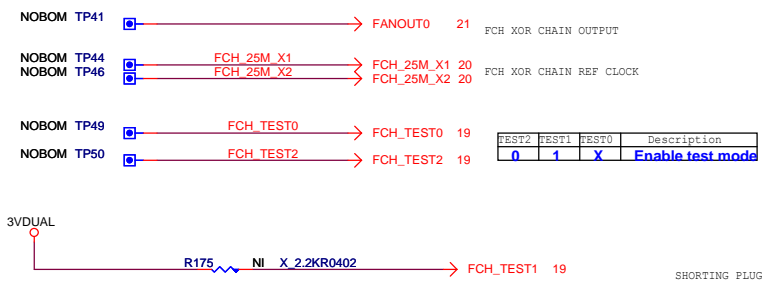
	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
<b>PULL HIGH</b>	S5 PLUS MODE DISABLED <small>DEFAULT</small>	ALLOW PCIE GEN2 <small>DEFAULT</small>	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED <small>DEFAULT</small>	LPC ROM
<b>PULL LOW</b>	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS <small>DEFAULT</small>	Required setting for intergrated CLOCK MODE <small>DEFAULT</small>	EC DISABLED <small>DEFAULT</small>	INTERNAL CLOCK GEN DISABLED	SPI ROM <small>DEFAULT</small>

# FCH DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL <small>DEFAULT</small>	RESERVED	Normal REFCLK Termination <small>DEFAULT</small>	USE DEFAULT PCIE STRAPS <small>DEFAULT</small>	DISABLE PCI MEM BOOT <small>DEFAULT</small>
<b>PULL DOWN</b>	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

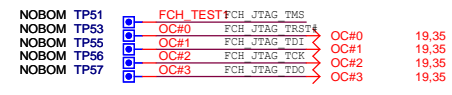
## FCH XOR CHAIN TEST



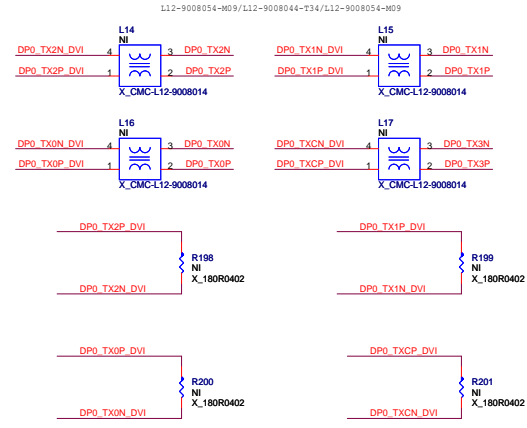
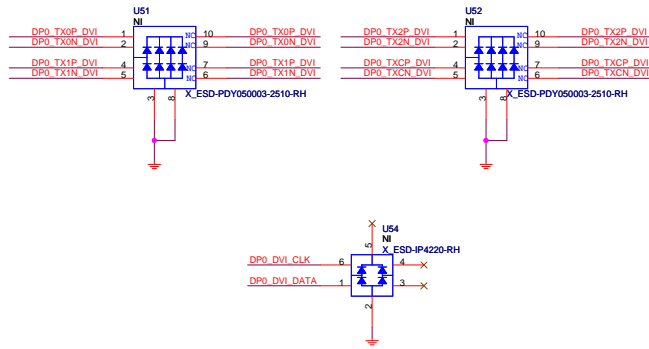
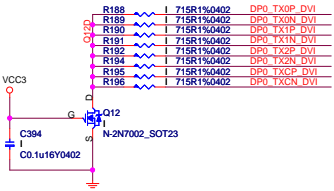
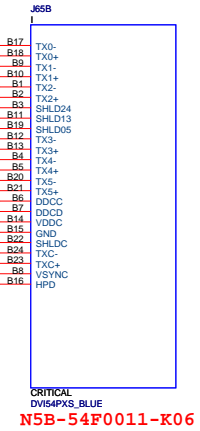
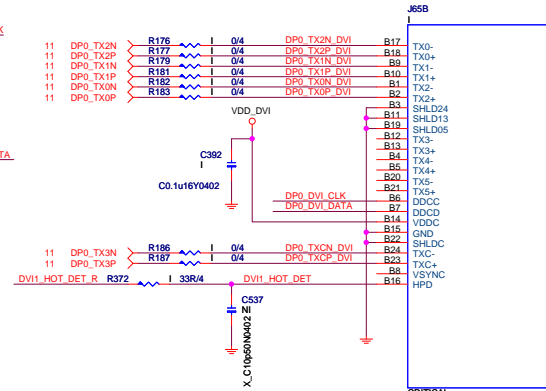
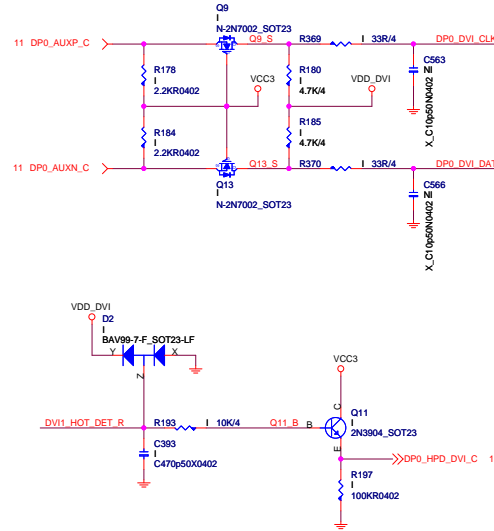
## FCH PCIE EEPROM STRAPS



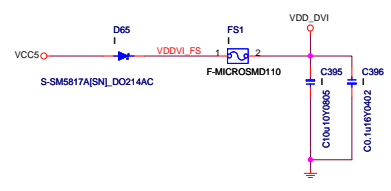
## FCH ICE DEBUG /JTAG TEST PINS



# DVI1 CONNECTOR



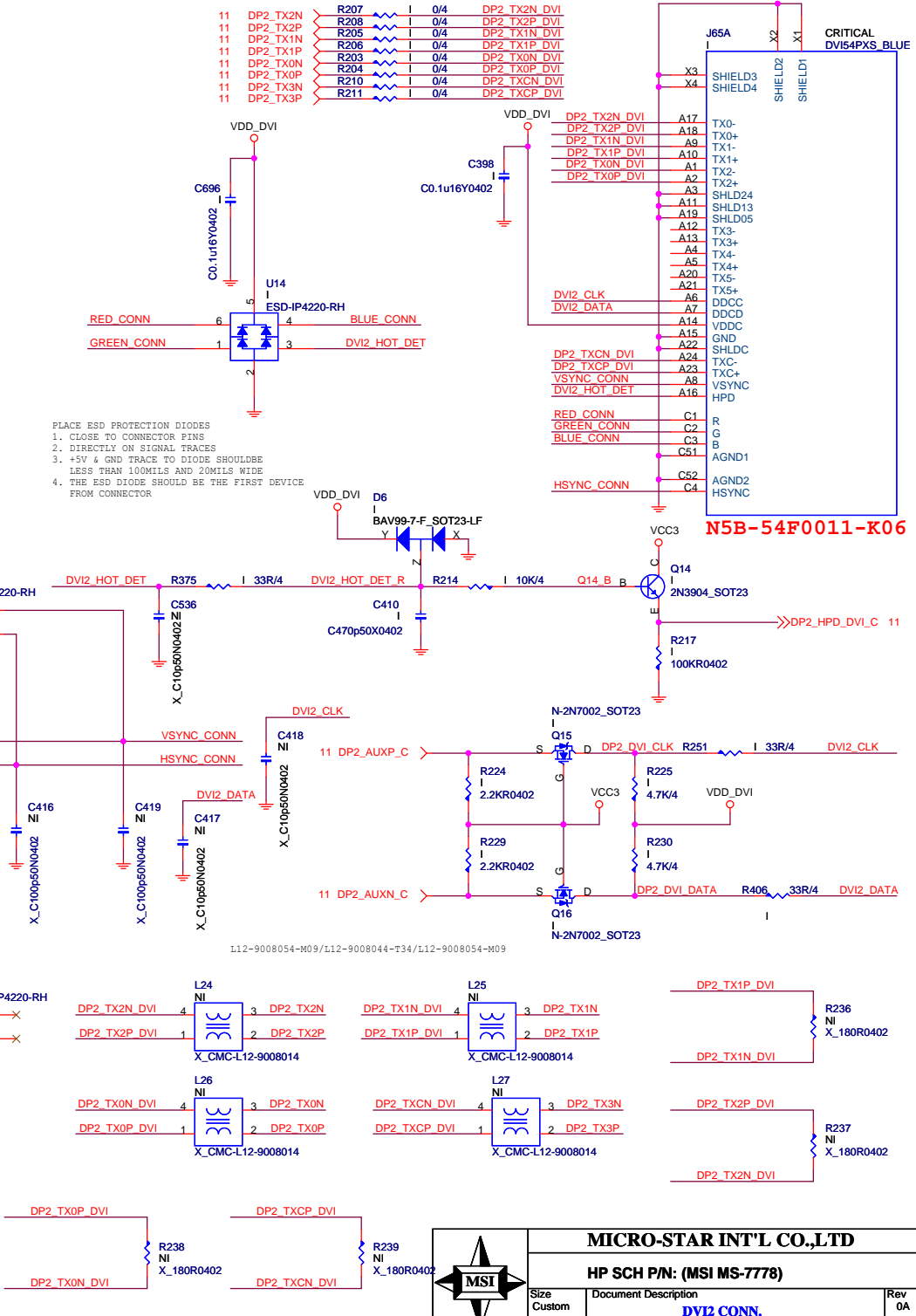
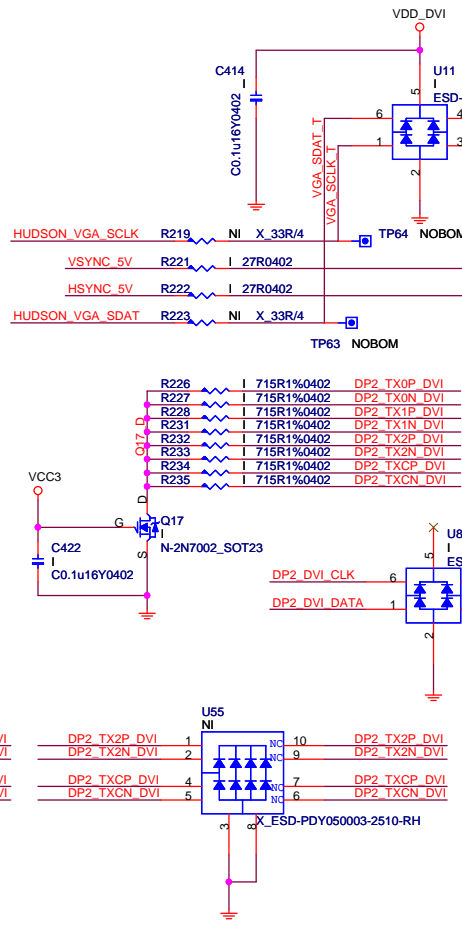
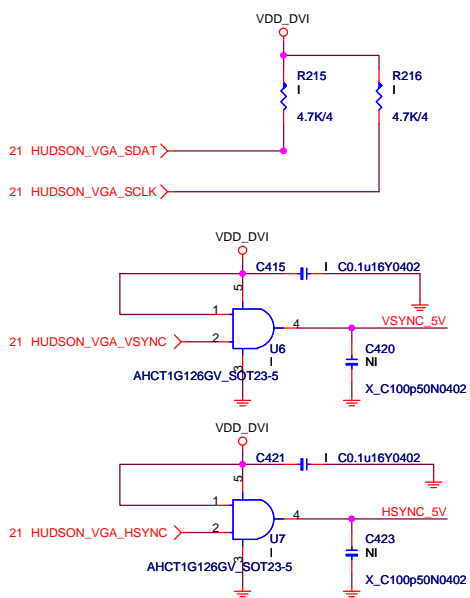
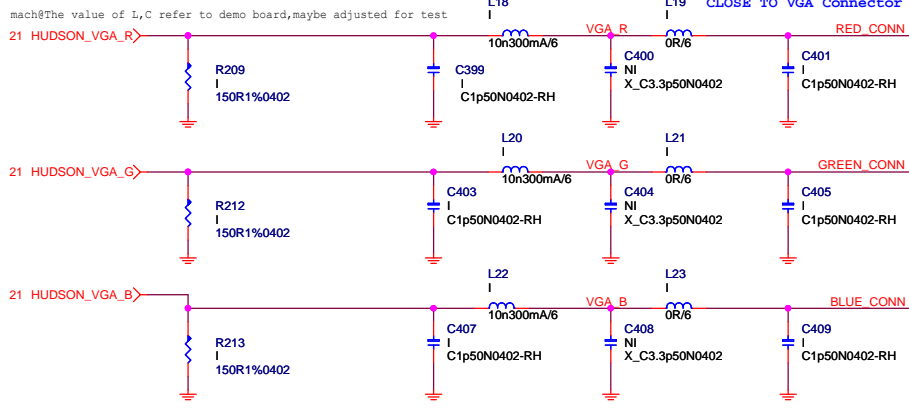
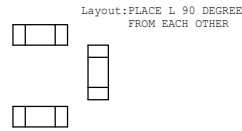
## DVI POWER

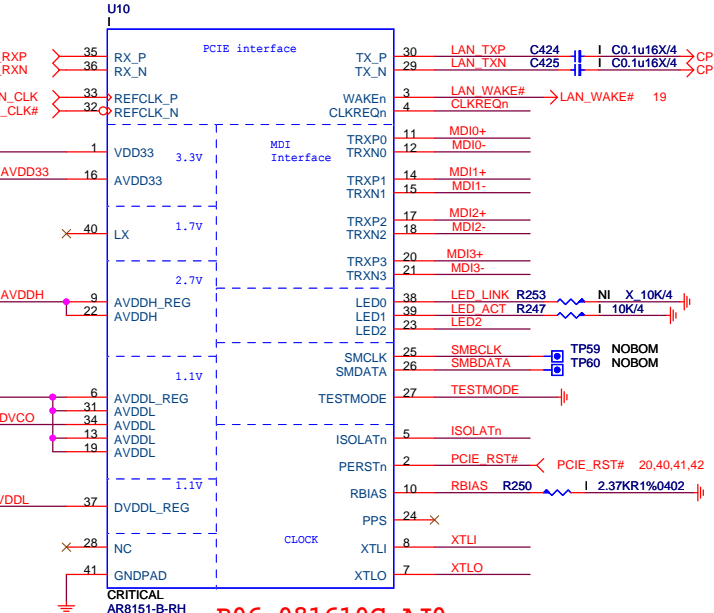
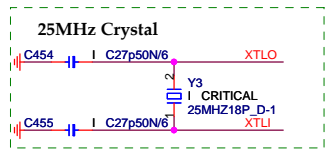
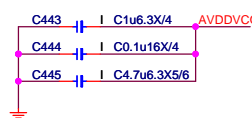
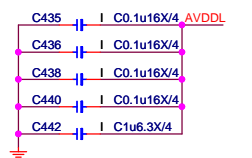
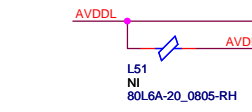
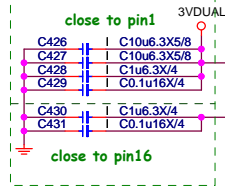




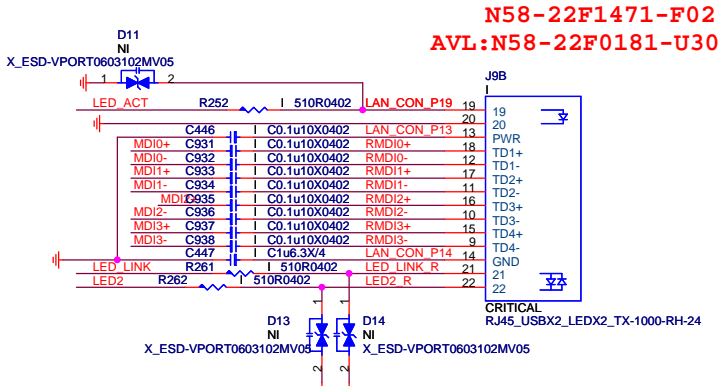
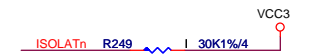
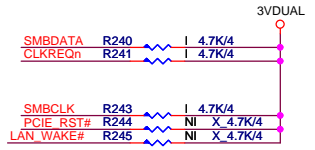
# DVI2 CONNECTOR

R932-R934 CLOSE TO CRT CONNECTOR, THE TRACE IMPEDANCE BETWEEN NB AND 150OHM RESISTOR SHOULD BE 37OHM+/-15%. THE TRACE IMPEDANCE BETWEEN THE 2 150OHM RESISTOR SHOULD BE 50 OHM +/-15%. THE IMPEDANCE BETWEEN THE 2ND RESISTOR TO THE CONNECTOR SHOULD BE 75OHM+/-15%

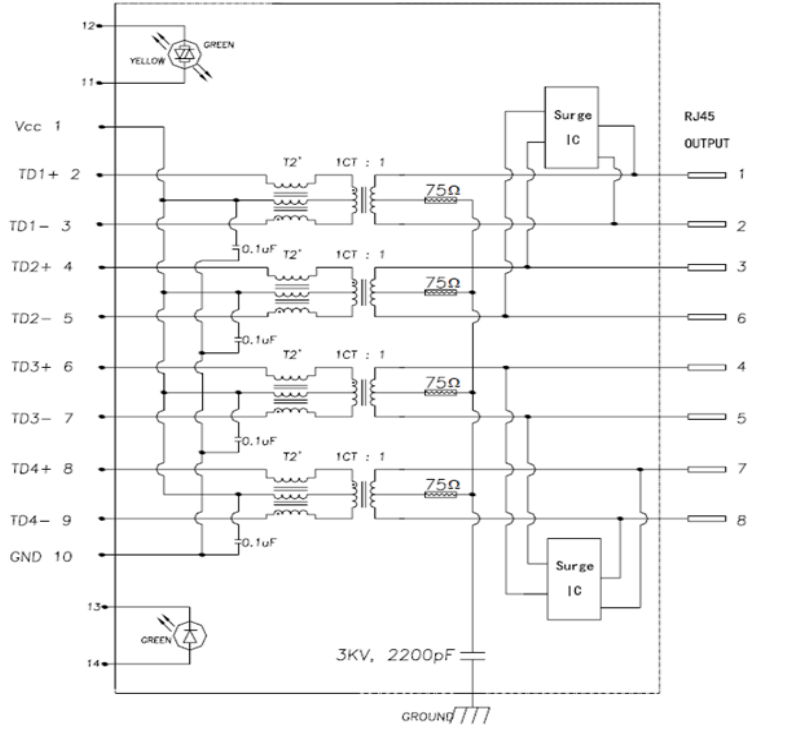
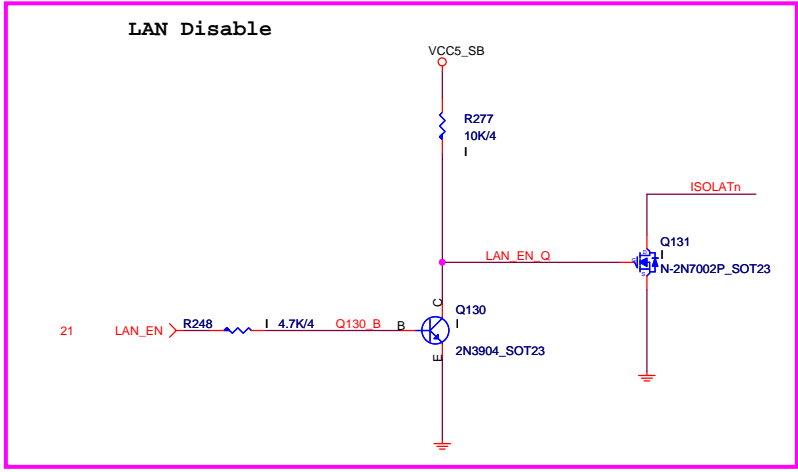




**B06-081610C-AJ0**



**N58-22F1471-F02**  
**AVL:N58-22F0181-U30**

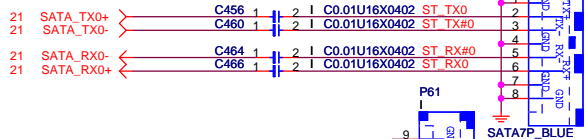


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
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<b>LAN AR8151</b>		
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### iSATA CONNECTOR

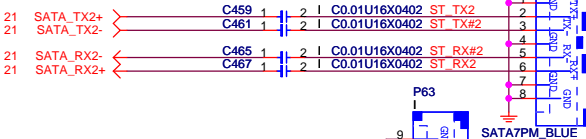
Multiple eSATA function

#### Dark Blue N5N-07M0651-H06

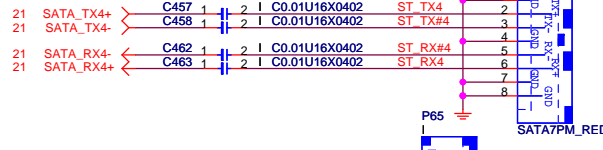


Layout: For Gen 3.0, trace length within 2.5"

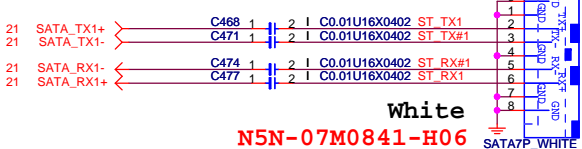
#### Light Blue N5N-07M0641-H06



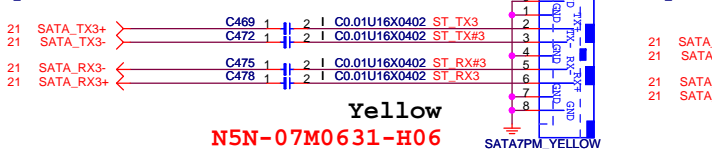
#### Red N5N-07M1991-H06



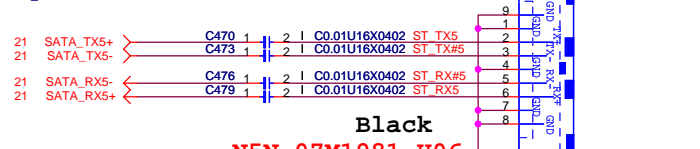
#### White N5N-07M0841-H06



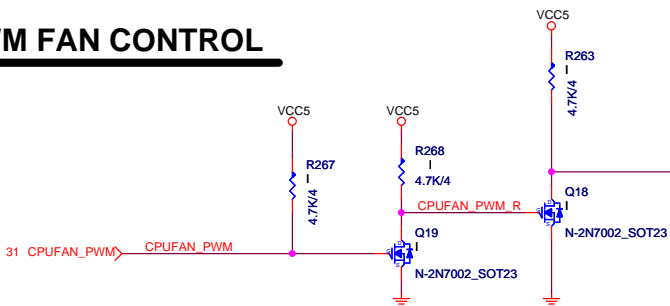
#### Yellow N5N-07M0631-H06



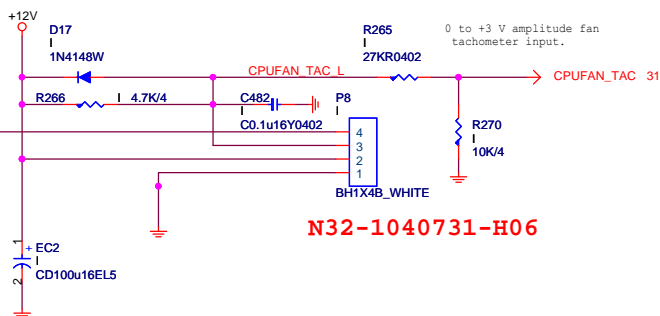
#### Black N5N-07M1981-H06



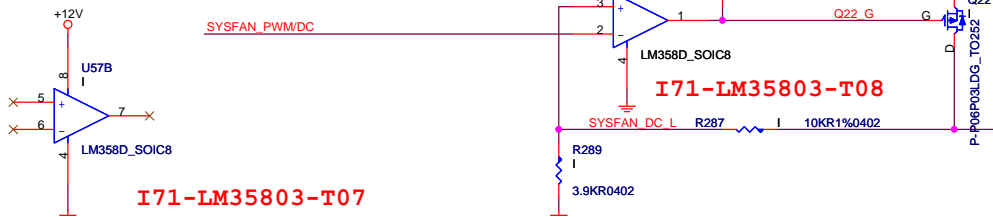
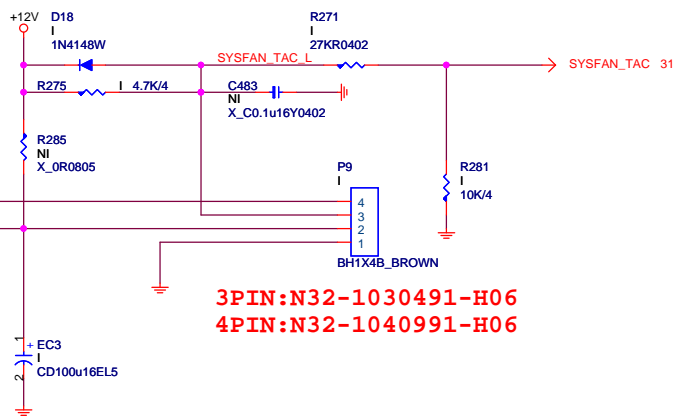
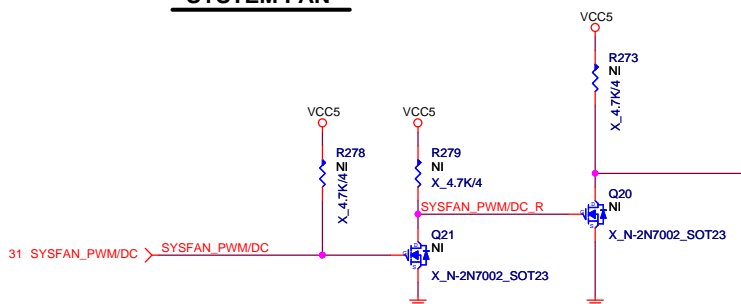
### PWM FAN CONTROL



### CPU FAN



### SYSTEM FAN



I71-LM35803-T07

I71-LM35803-T08

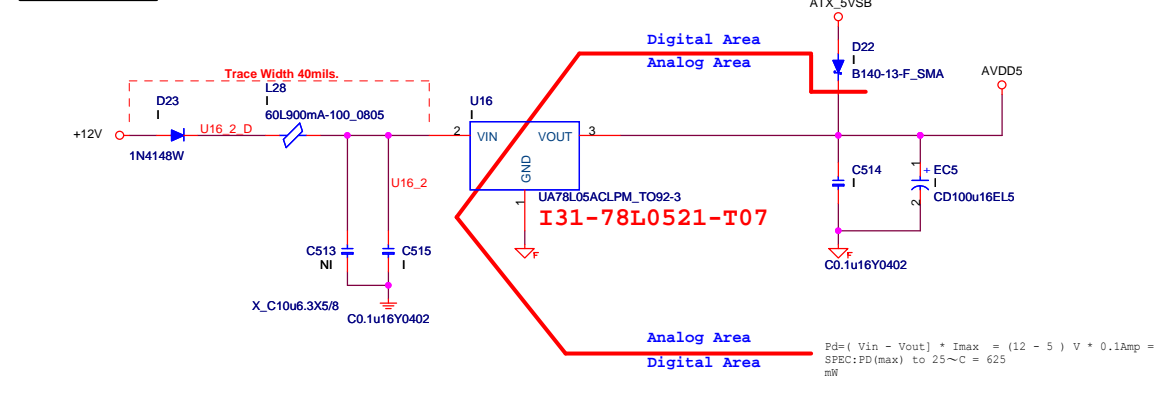
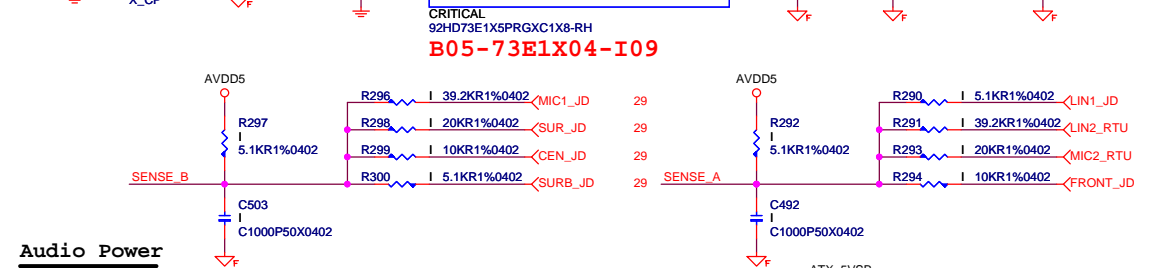
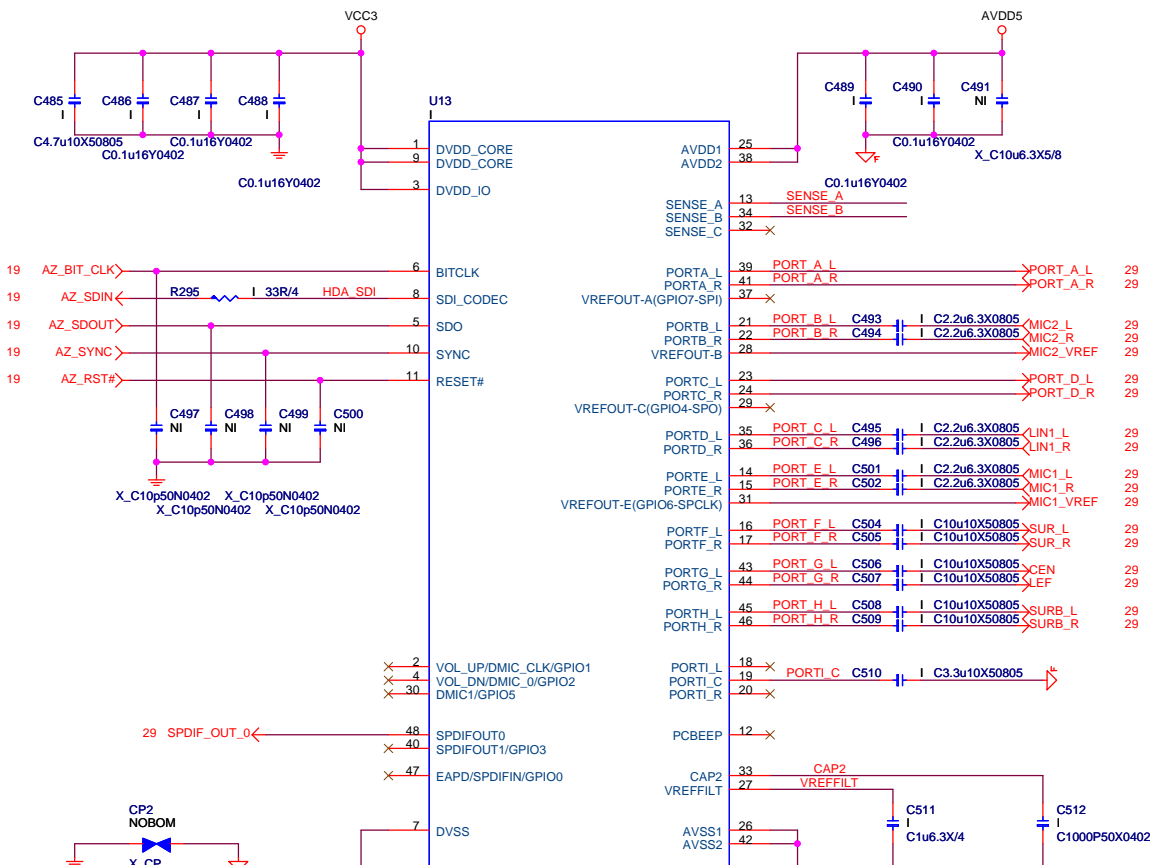
3PIN:N32-1030491-H06  
4PIN:N32-1040991-H06



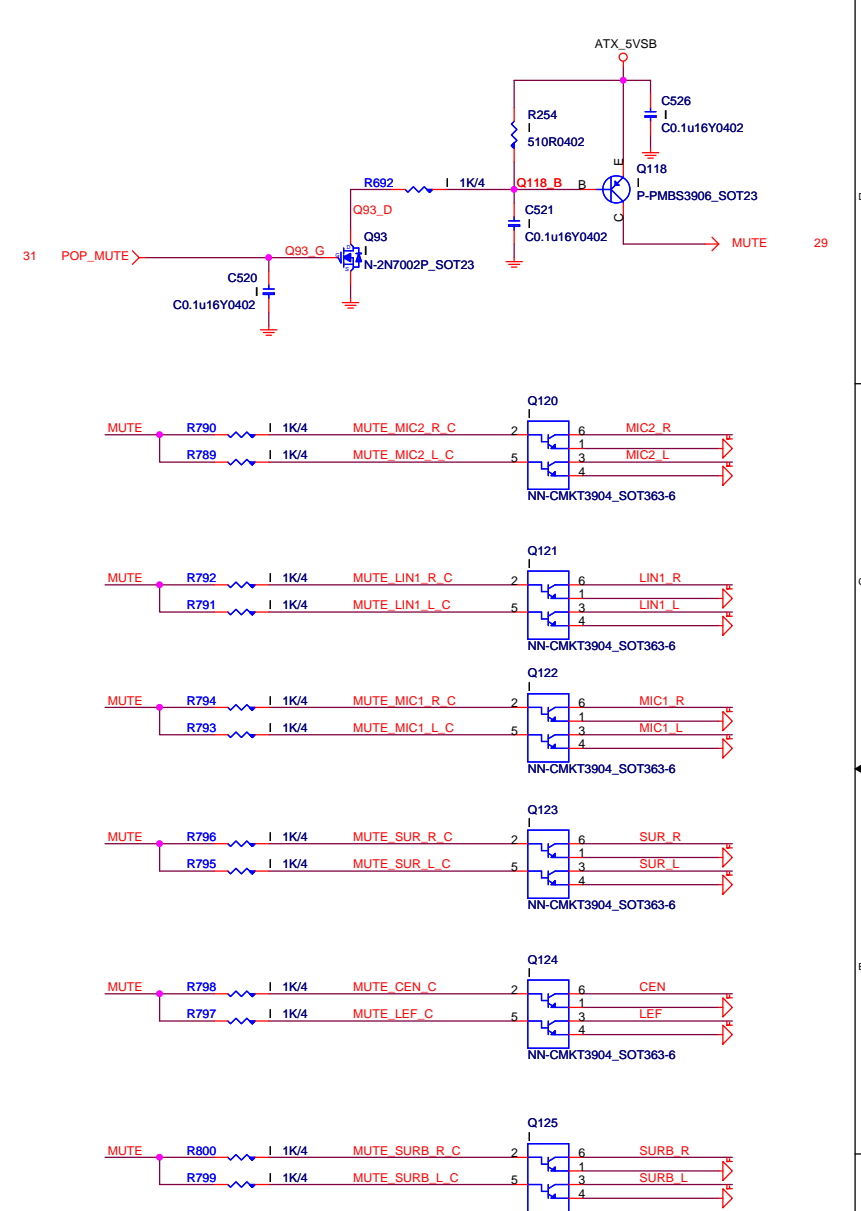
MICRO-STAR INT'L CO.,LTD

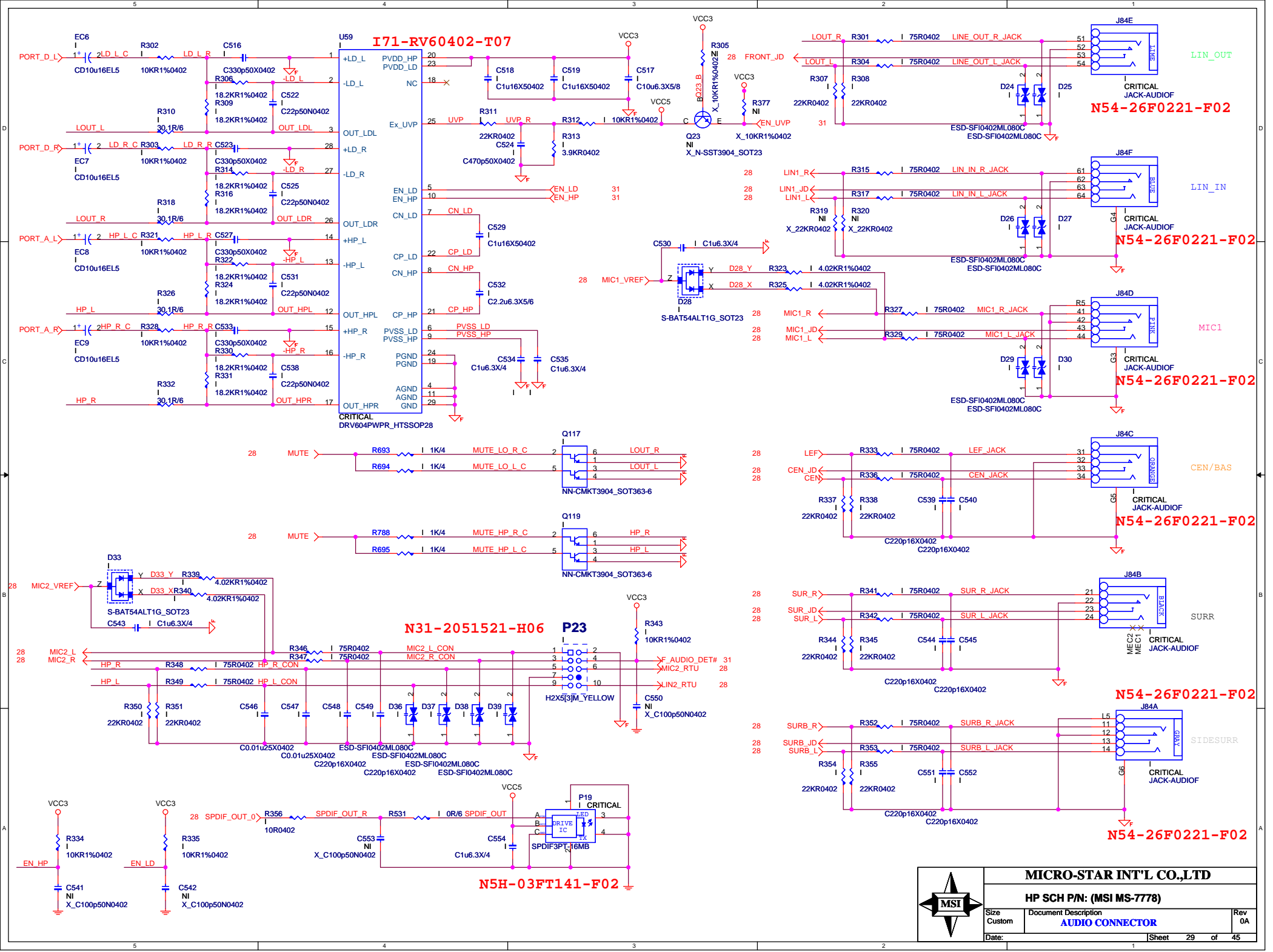
HP SCH P/N: (MSI MS-7778)

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SATA/FAN		
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$P_d = (V_{in} - V_{out}) \cdot I_{max} = (12 - 5) \cdot 0.1 \text{Amp} = 0.7 \text{ W}$   
 SFBP: PD(max) to 25~C = 625 mW





**I71-RV60402-T07**

**N31-2051521-H06 P23**

**N5H-03FT141-F02**

**N54-26F0221-F02**

**N54-26F0221-F02**

**N54-26F0221-F02**

**N54-26F0221-F02**

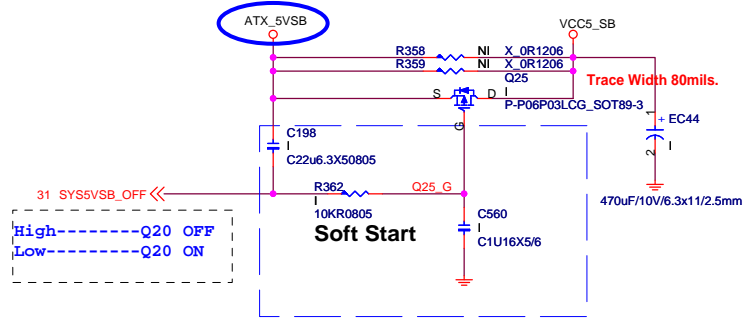
**N54-26F0221-F02**

**N54-26F0221-F02**



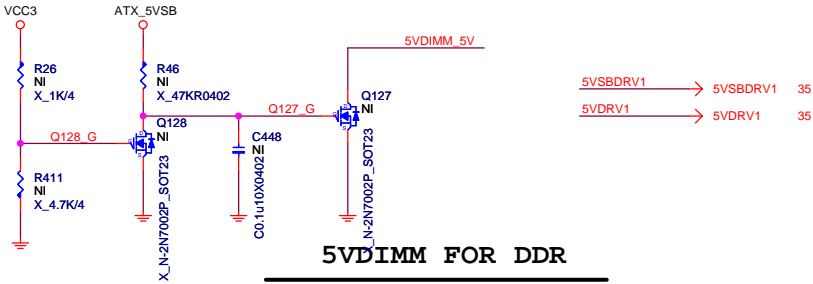
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>AUDIO CONNECTOR</b>	Rev 0A
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## VCC5 SB Power Switch

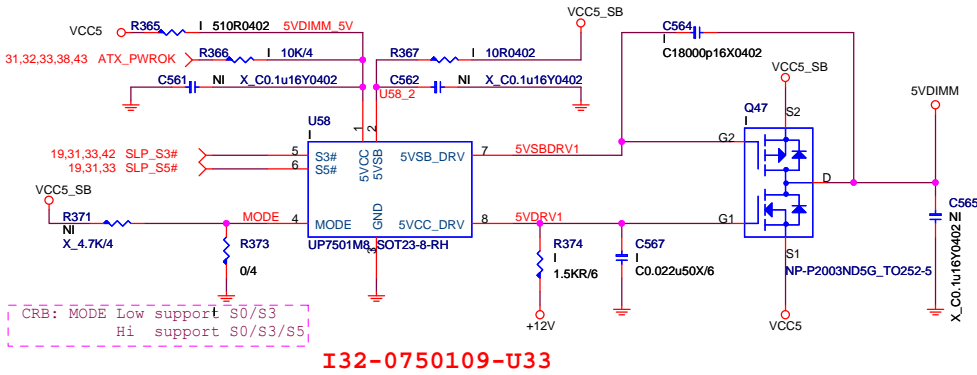


For special PSU sequence

High-----Q20 OFF  
Low-----Q20 ON

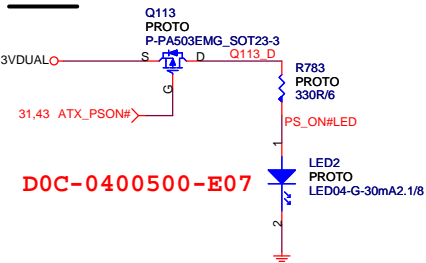


## 5VDIMM FOR DDR



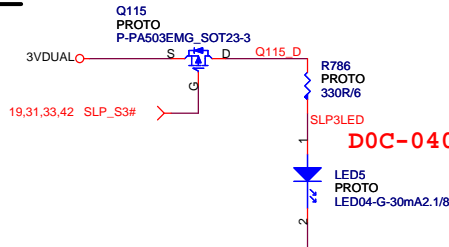
I32-0750109-U33

## PS\_ON#



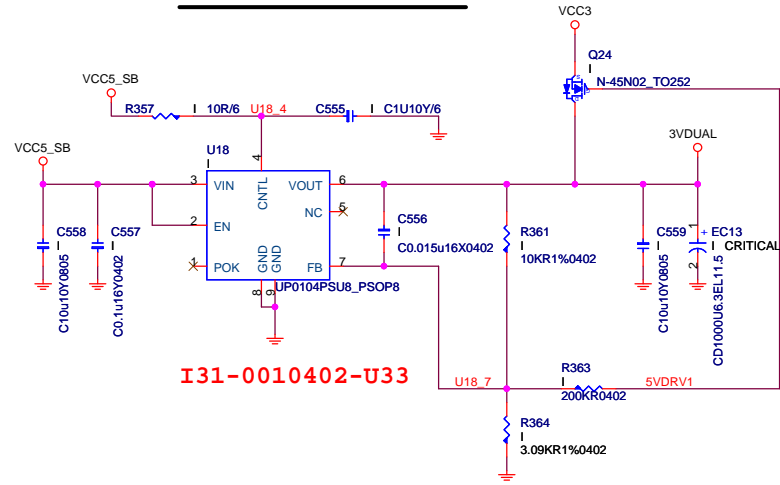
DOC-0400500-E07

## SLP\_S3#



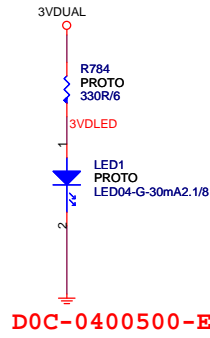
DOC-0400500-E07

## 3VDUAL POWER



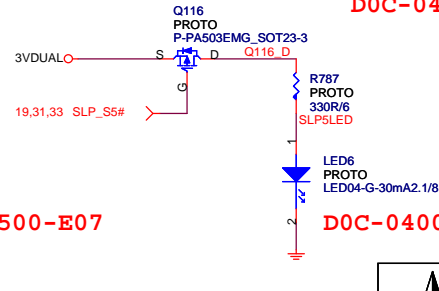
I31-0010402-U33

## 3VDUAL



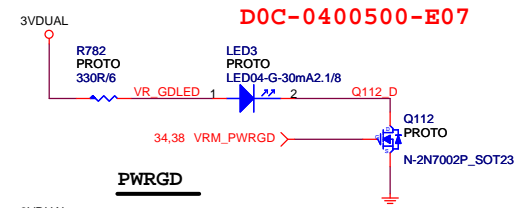
DOC-0400500-E07

## SLP\_S5#



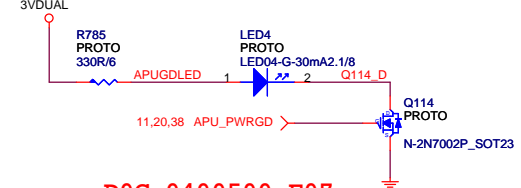
DOC-0400500-E07

## VRMPWRGD



DOC-0400500-E07

## PWRGD



DOC-0400500-E07



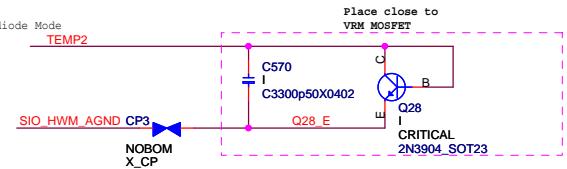
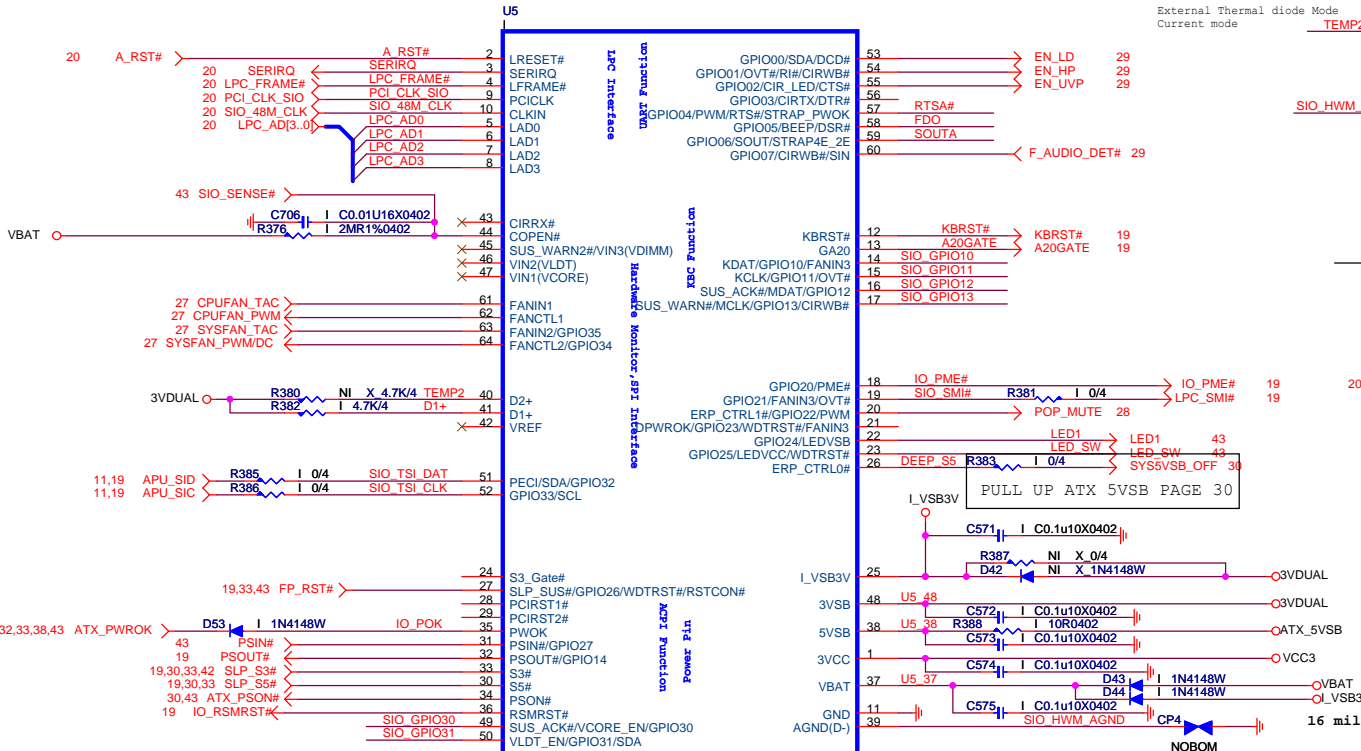
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

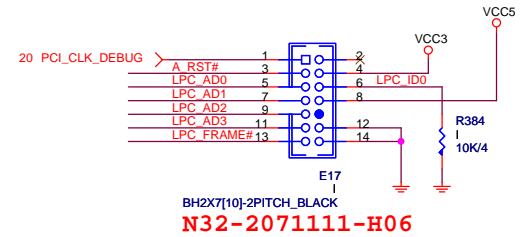
Size Custom	Document Description	Rev 0A
Date:	ACPI UPI & LED	Sheet 30 of 45

# F71808A

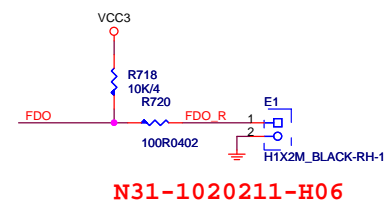
## TEMP SENSOR



## LPC Debug

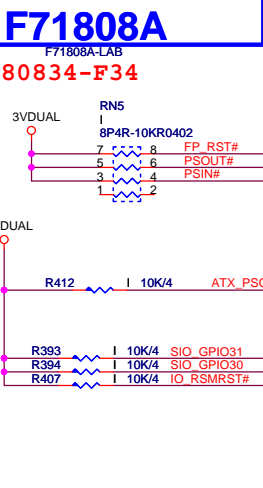
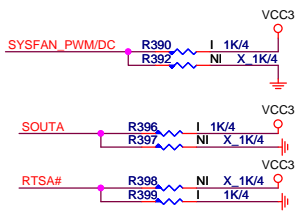


## Flash Descriptor Override Header



## LPC I/O STRAPPING RESISTOR

### POWER-ON TRIP



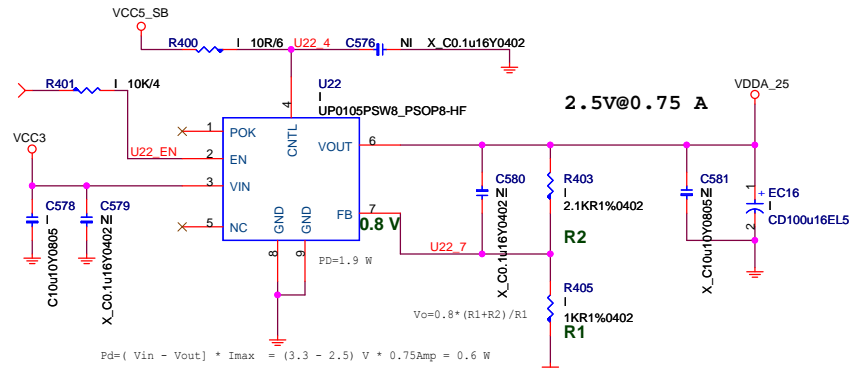
PIN	Function	NET Name	HI	LO
64	FANCTRL2	FANCTRL2	PWM FAN	LINEAR FAN
59	STRAP4E_2E	SOUTA	4E (DEFAULT)	2E
57	STRAP_PWOK	RTSA#	AMD (DEFAULT)	INTEL



**MICRO-STAR INT'L CO.,LTD**  
**HP SCH P/N: (MSI MS-7778)**  
 Size Custom Document Description **SUPER I/O F71808A** Rev 0A  
 Date: \_\_\_\_\_ Sheet 31 of 45

### CPU VDDA\_25 POWER

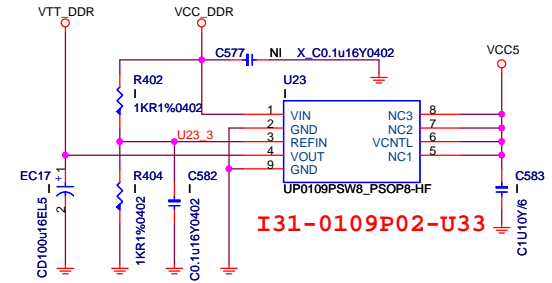
Layout:Route 50 mils AND 500 mils LONG  
(USE 2x25 mil TRACES TO EXIT BALL FIELD)



I31-0010502-U33

### VTT\_DDR POWER

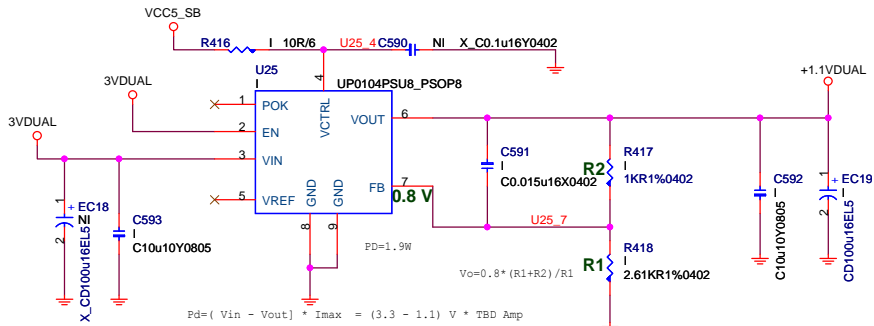
0.75V@2A



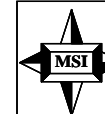
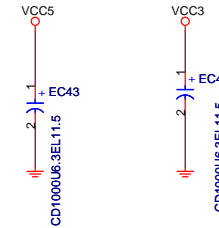
I31-0109P02-U33

### 1.1VDUAL POWER

1.V@1.3A----D3



I31-0010402-U33



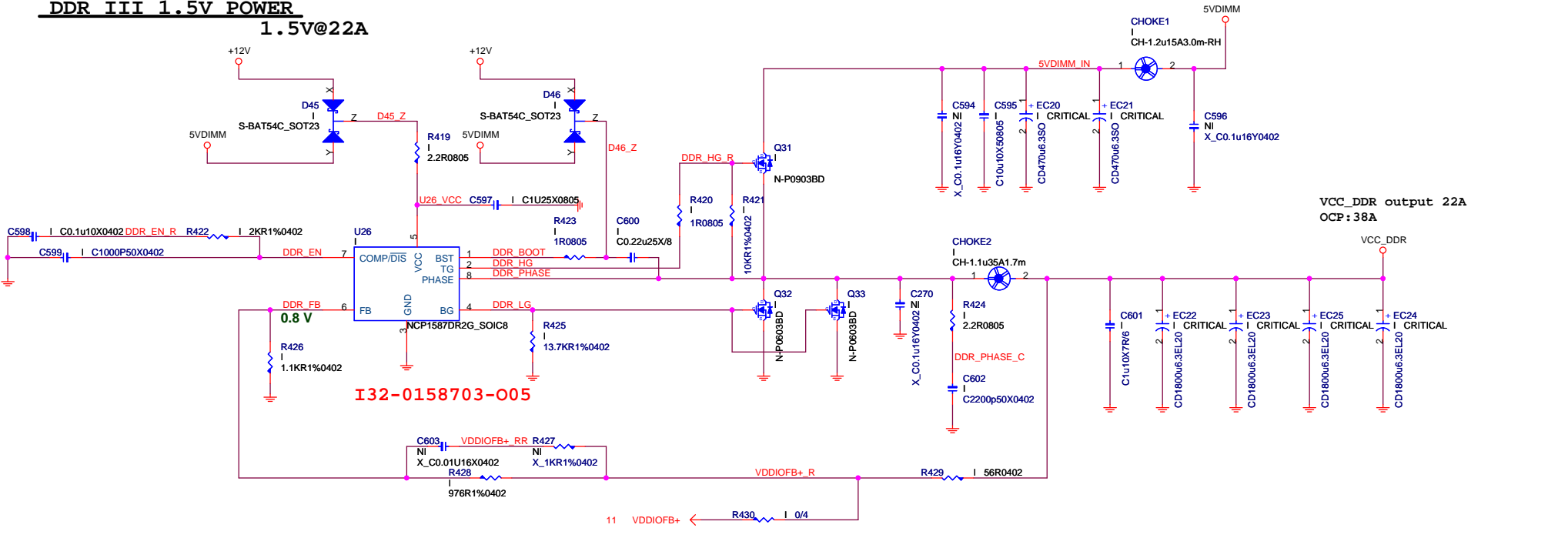
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

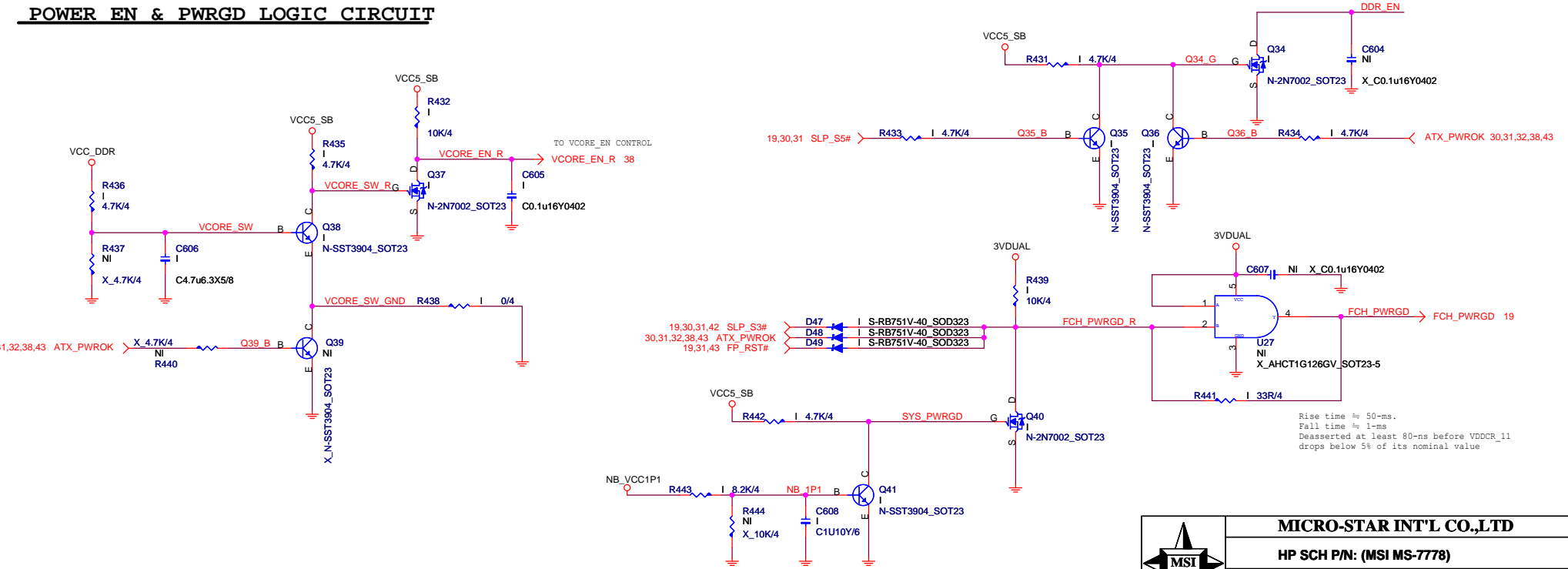
Size Custom	Document Description <b>SYS POWER</b>	Rev 0A
Date:		Sheet 32 of 45



**DDR III 1.5V POWER**  
**1.5V@22A**



**POWER EN & PWRGD LOGIC CIRCUIT**

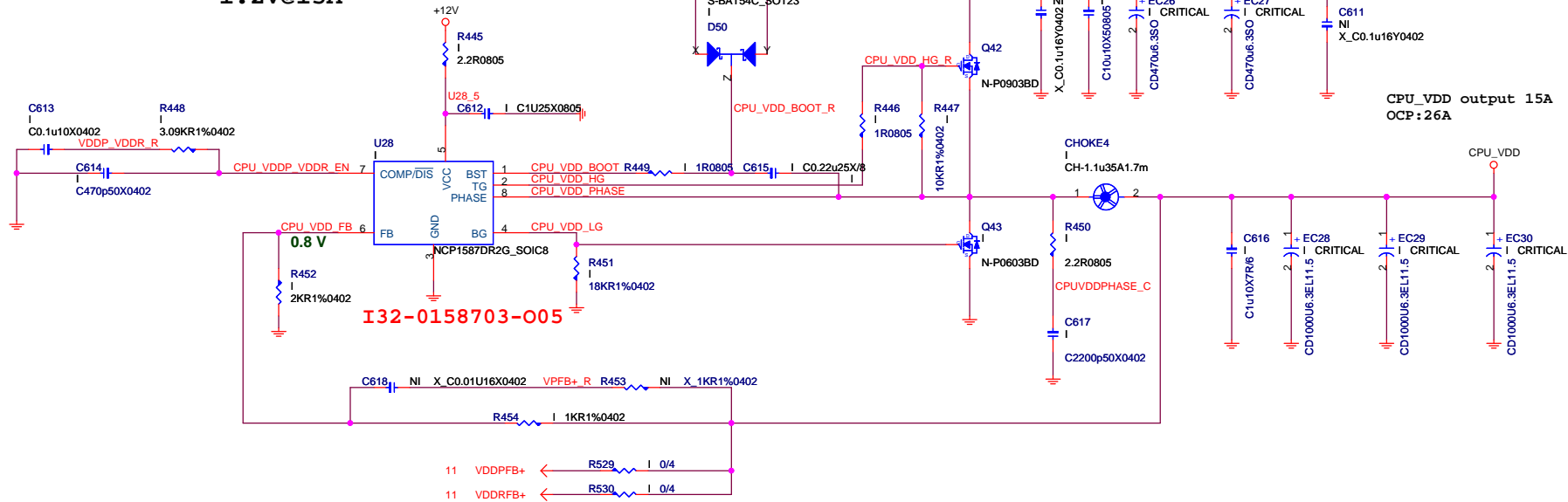


Rise time ≈ 50-ns.  
 Fall time ≈ 1-ns  
 Deasserted at least 80-ns before VDDCR\_11 drops below 5% of its nominal value

	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>HP SCH P/N: (MSI MS-7778)</b>	
	Size Custom	Document Description <b>DDR POWER</b>
Date:	Sheet 33 of 45	

# CPU VDD POWER

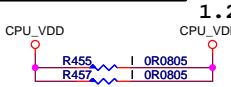
## 1.2V@15A



VDDP and VDDR support two separate power planes with single regulator

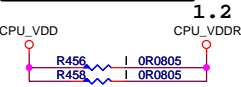
### CPU\_VDDP POWER

#### 1.2 V@5A



### CPU\_VDDR POWER

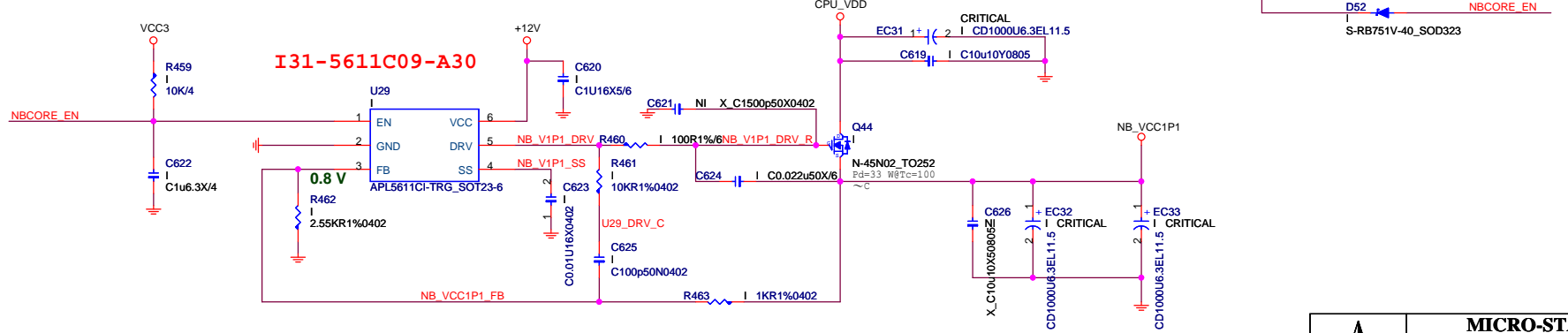
#### 1.2 V@5A



VDDP&VDDR IS COMBINED BY DEFAULT  
 VDDP\_FRMONLY FOR NORMAL OPERATION(VDDR/VDDP COMBINED MODE)  
 VDDR\_FWMIS FOR DEBUG/OC MODE (SEPERATE VDDR/VDDP)

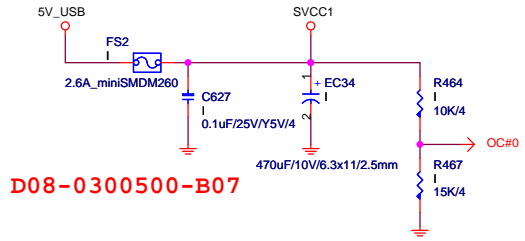
# NB VCC1P1 POWER

## 1.1V@5A



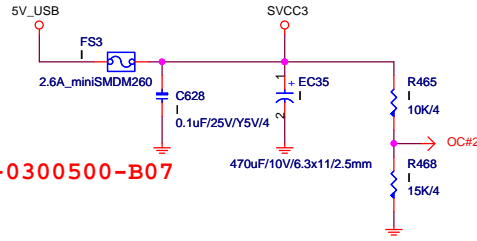
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description	Rev 0A
<b>FCH CORE</b>		
Date:		Sheet 34 of 45

USB POWER



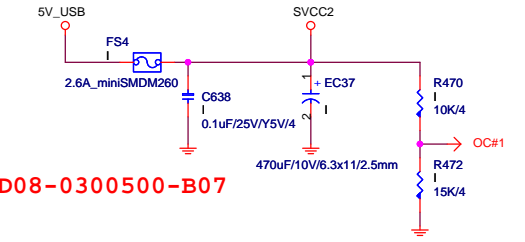
D08-0300500-B07

19,23



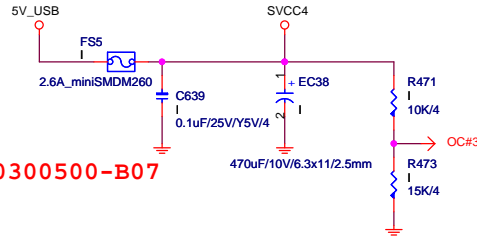
D08-0300500-B07

19,23



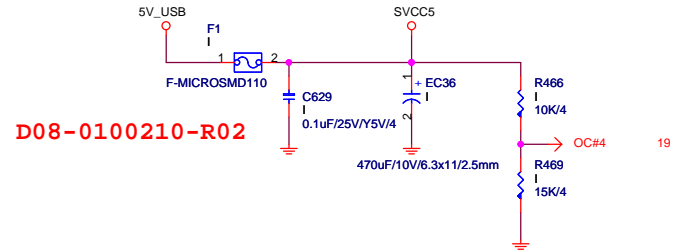
D08-0300500-B07

19,23



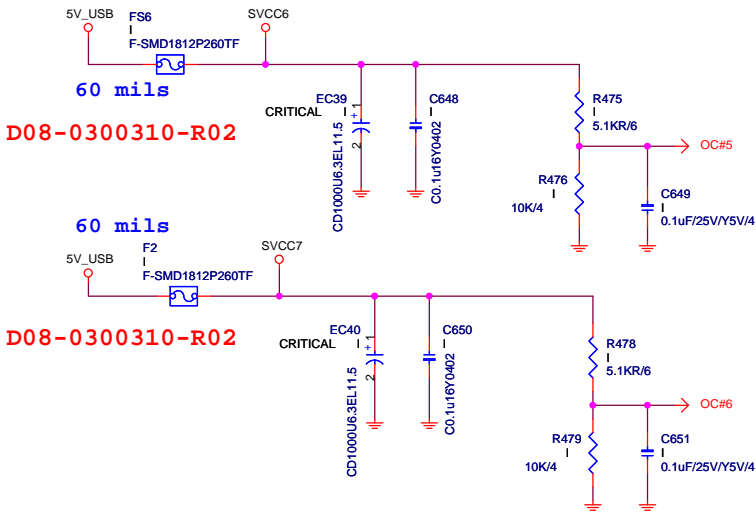
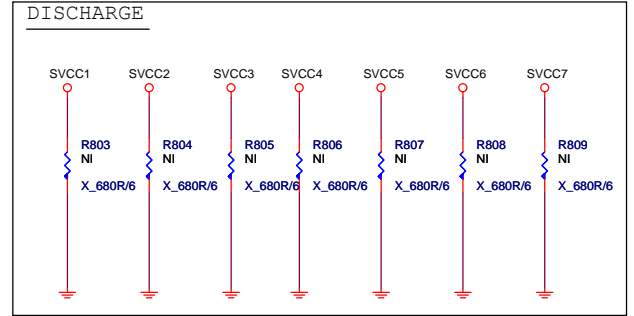
D08-0300500-B07

19,23



D08-0100210-R02

19

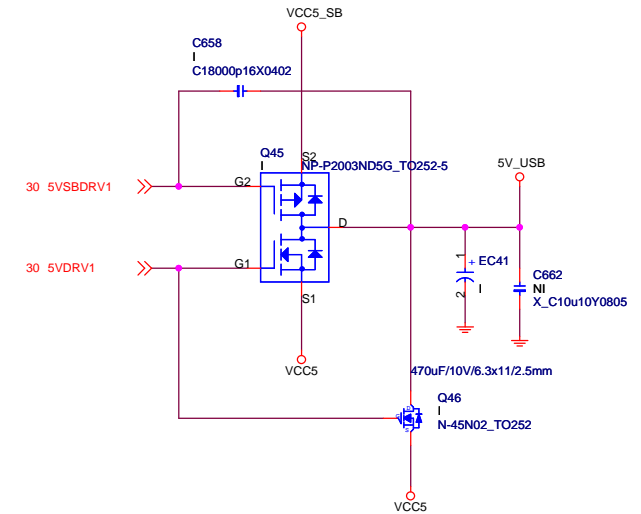


D08-0300310-R02

19

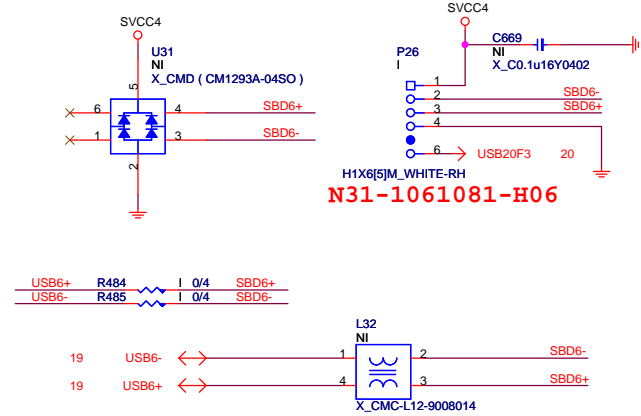
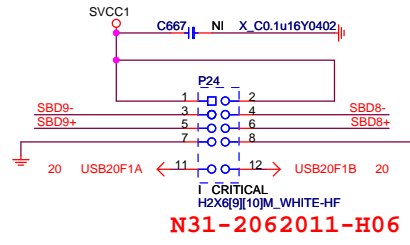
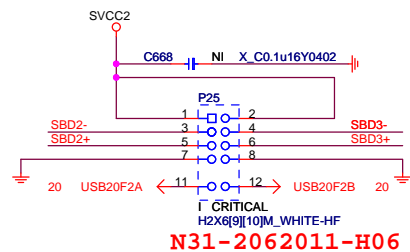
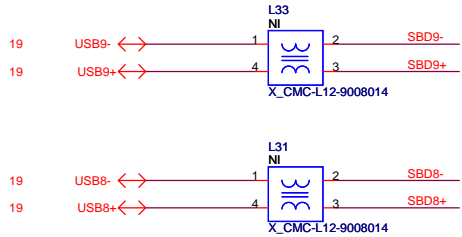
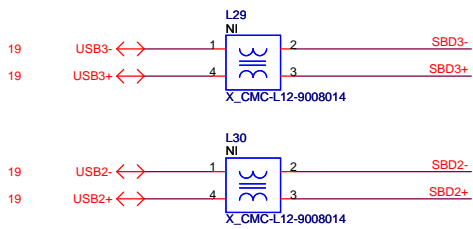
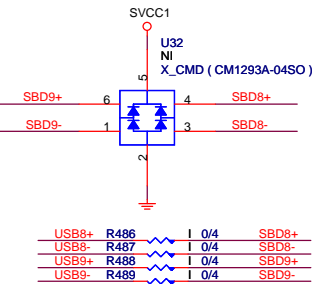
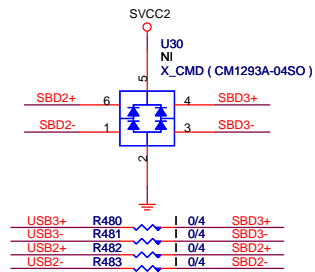
D08-0300310-R02

19



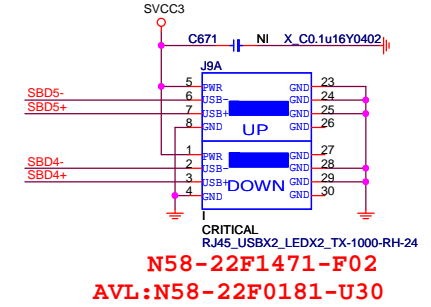
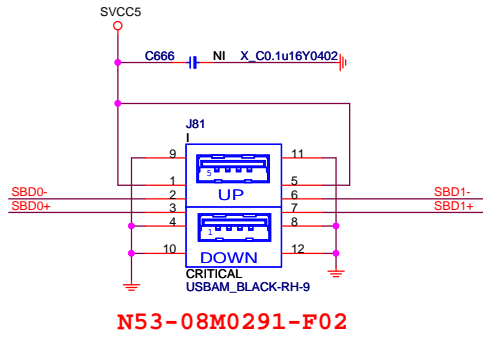
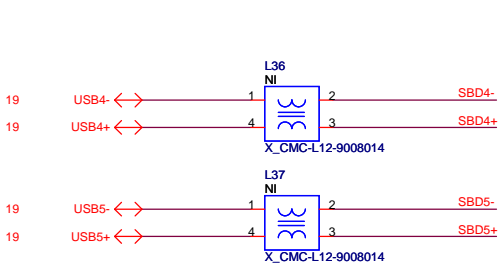
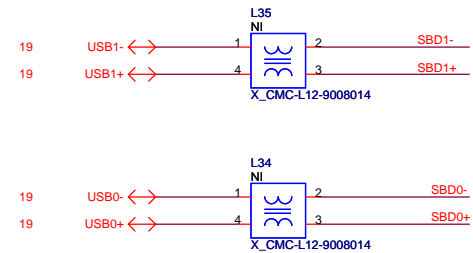
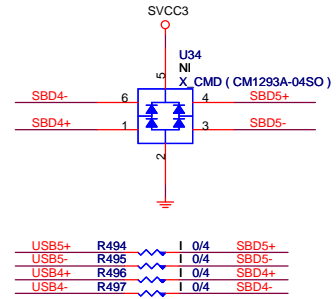
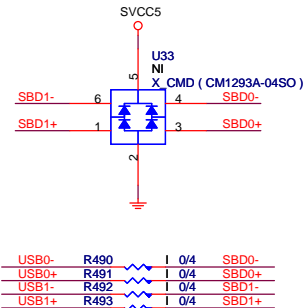
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>USB POWER</b>	Rev 0A
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# FRONT USB PIN HEADER



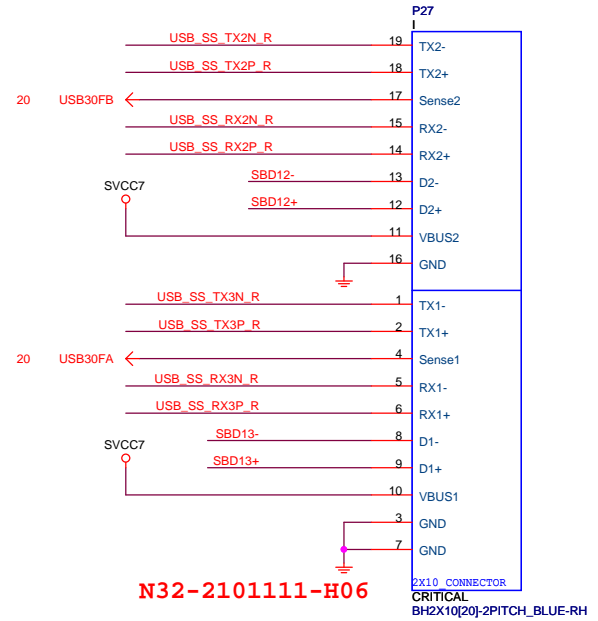
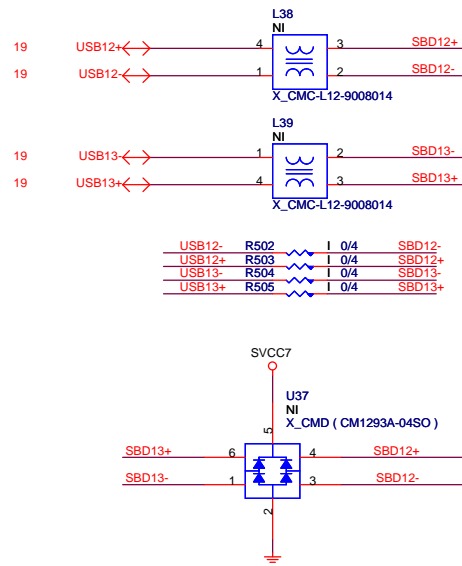
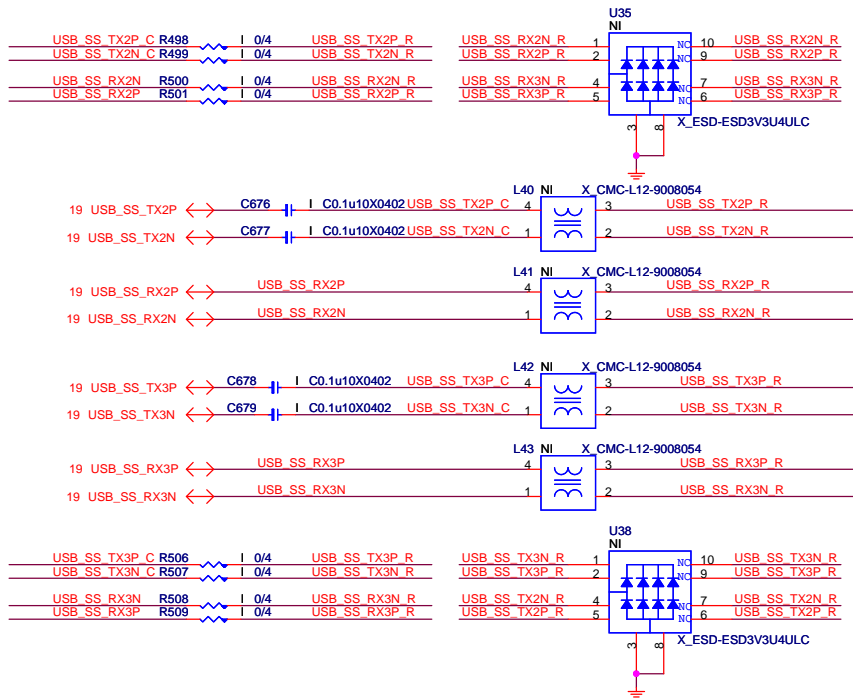
USB 2.0 trace length  
FRONT side within 6'';  
REAR side within 18''

# REAR PANEL USB 2.0 CONNECTOR

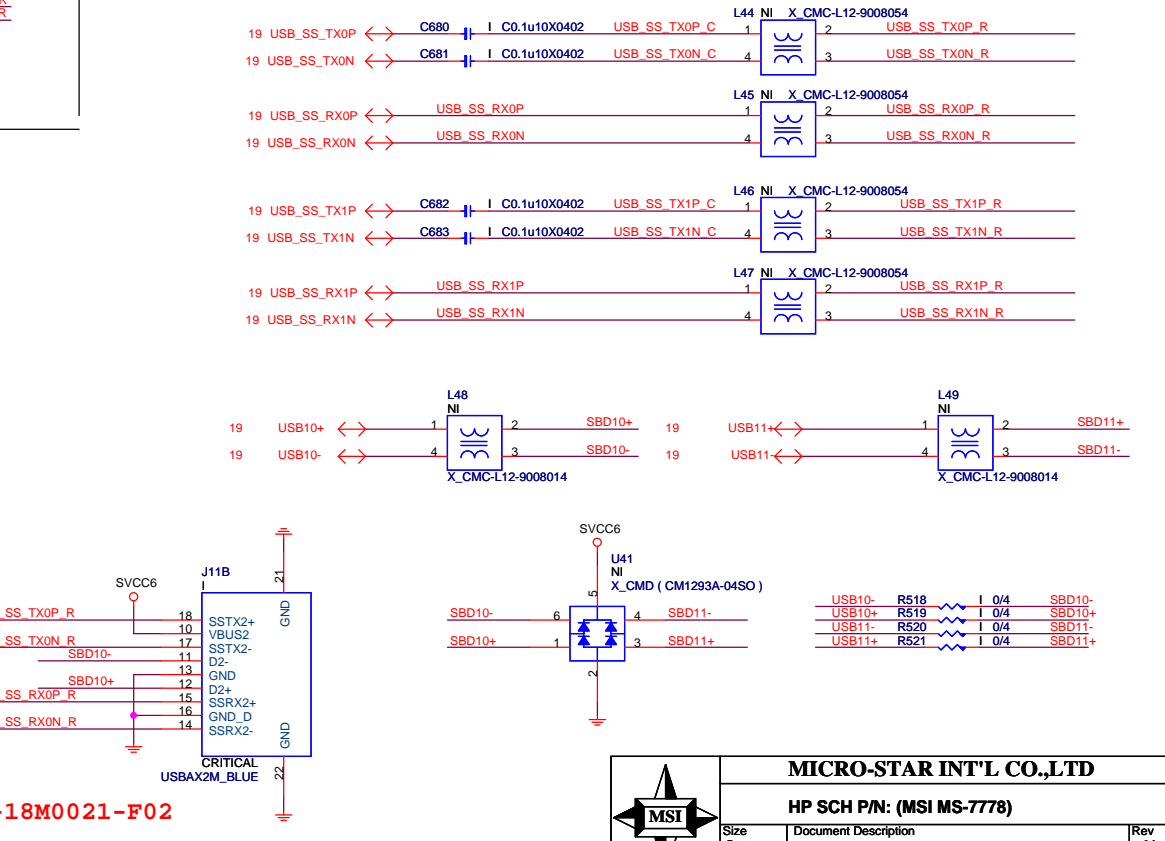
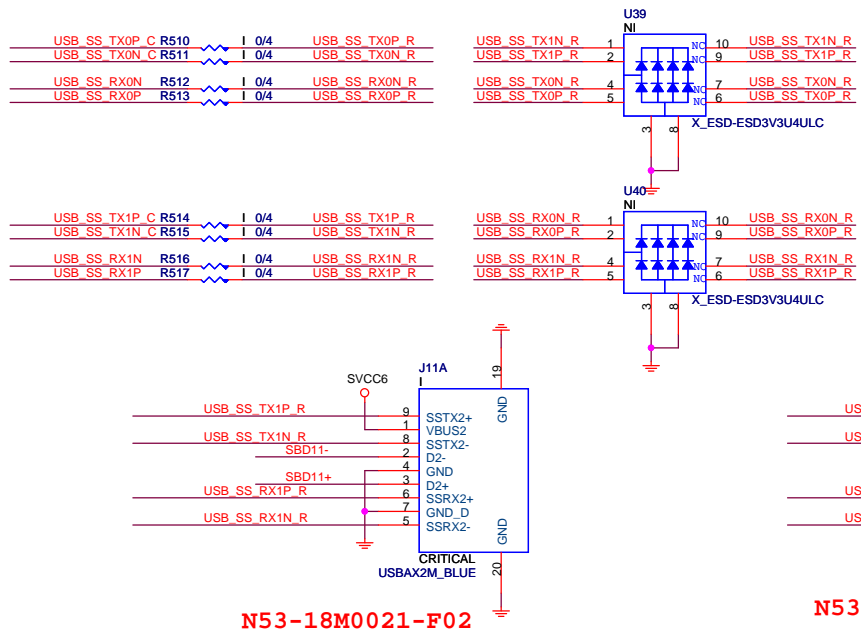


<b>MICRO-STAR INT'L CO.,LTD</b>		
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USB 3.0 trace length  
Front pin header within 3.5''



USB 3.0 trace length  
Rear connector within 8''



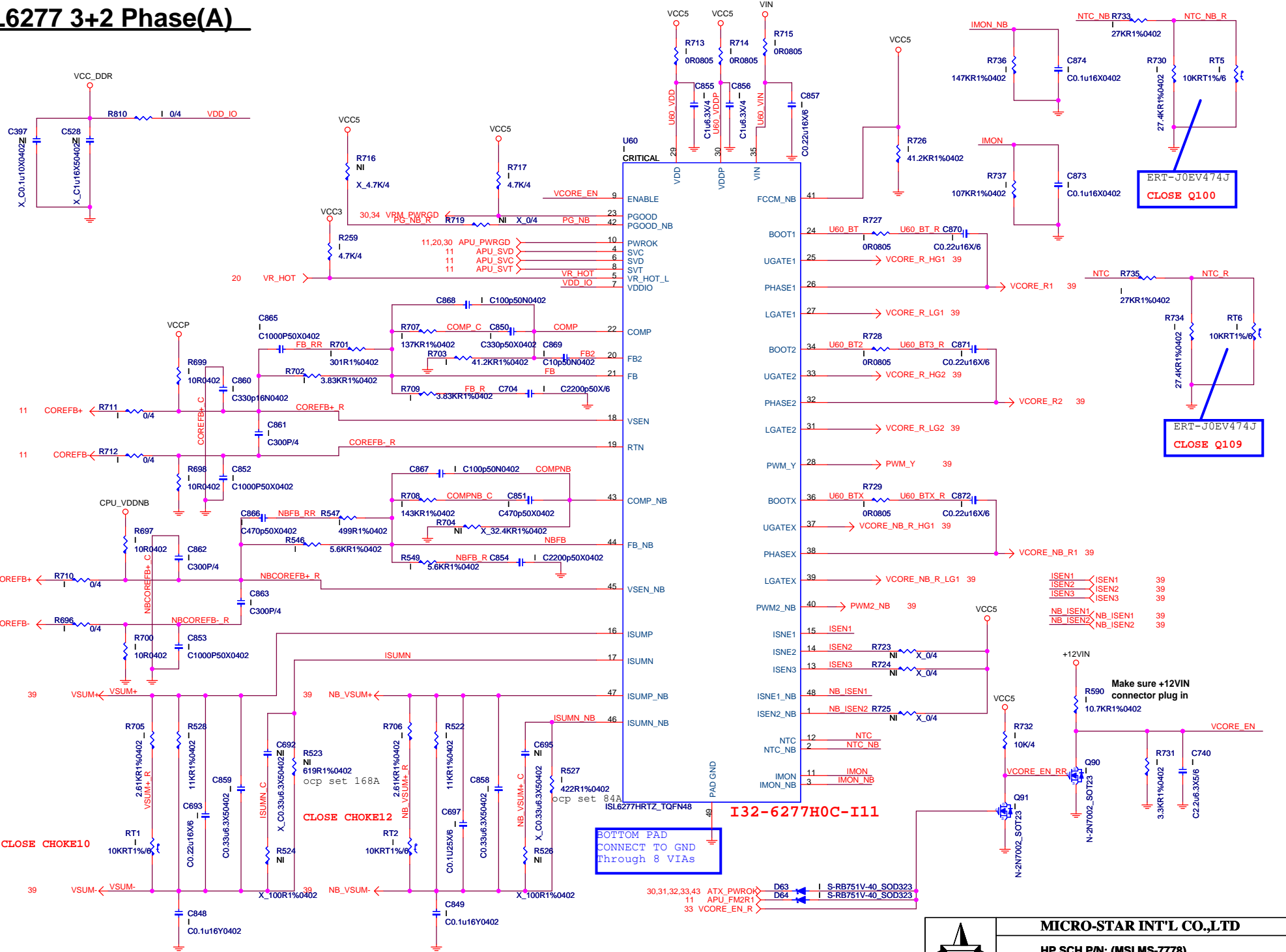
N53-18M0021-F02

N53-18M0021-F02



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description	Rev 0A
	<b>USB 3.0 CONN</b>	
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# ISL6277 3+2 Phase(A)



ERT-J0EV474J  
CLOSE Q100

ERT-J0EV474J  
CLOSE Q109

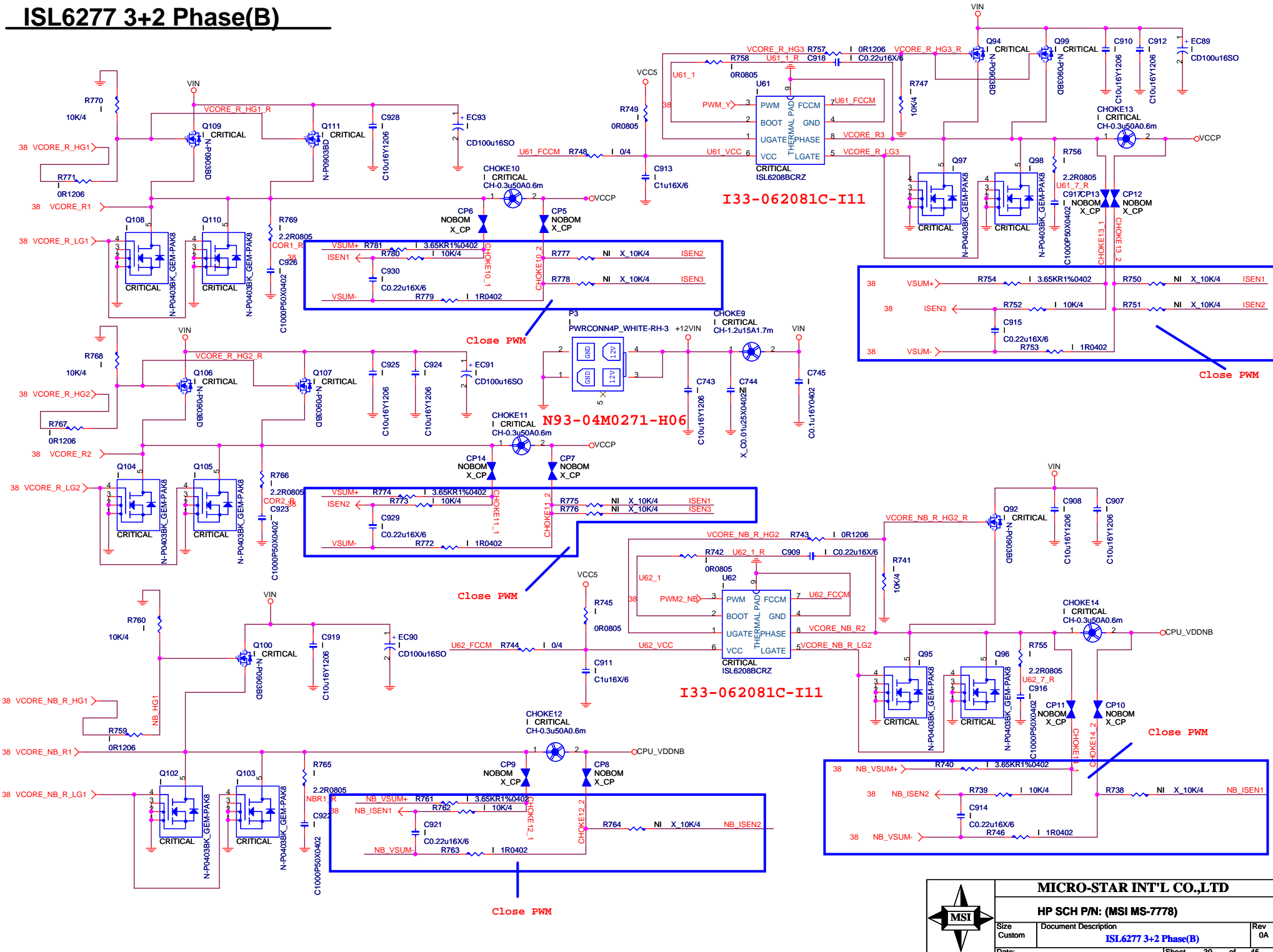
BOTTOM PAD  
CONNECT TO GND  
Through 8 VIAs

I32-6277H0C-I11



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>ISL6277 3+2 Phase(A)</b>	Rev 0A
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# ISL6277 3+2 Phase(B)



I33-062081C-I11

N93-04M0271-H06

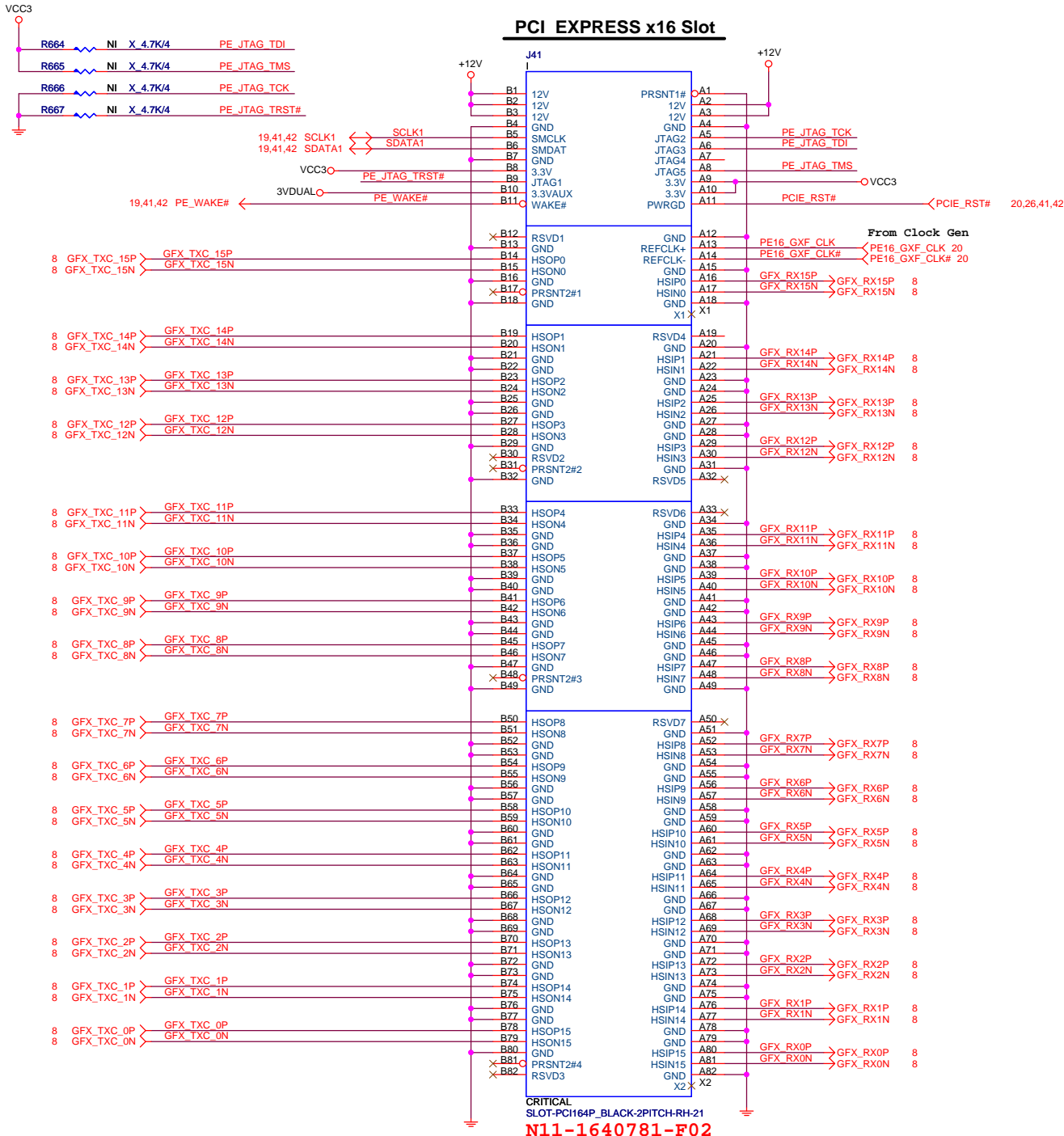
I33-062081C-I11



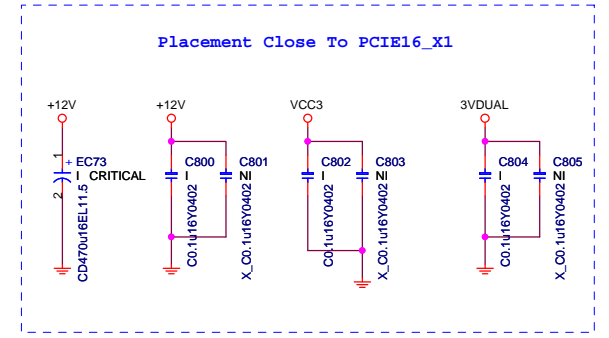
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>HP SCH P/N: (MSI MS-7778)</b>		
Size Custom	Document Description <b>ISL6277 3+2 Phase(B)</b>	Rev 0A
Date:	Sheet	39 of 45

PCI Express Slot x16

PCI EXPRESS x16 Slot



PCIE\_RST# C799 NI X\_C0.1u16Y0402



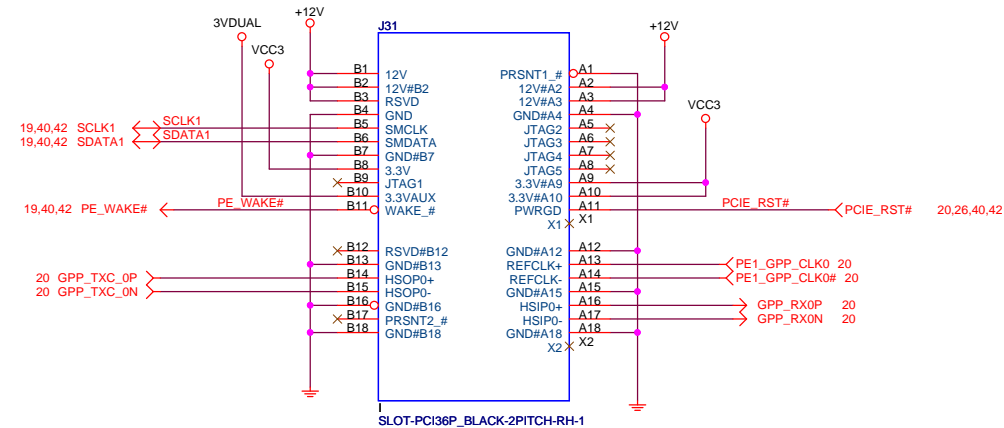
CRITICAL  
SLOT-PCI164P\_BLACK-2PITCH-RH-21  
**N11-1640781-F02**



MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: (MSI MS-7778)		
Size Custom	Document Description	Rev 0A
	<b>PCIE X16 SLOT</b>	
Date:		Sheet 40 of 45

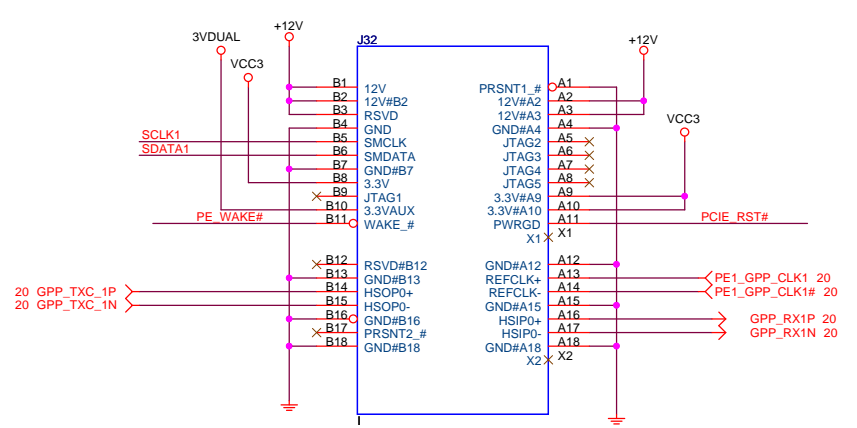


### PCI EXPRESS X1 Slot-1



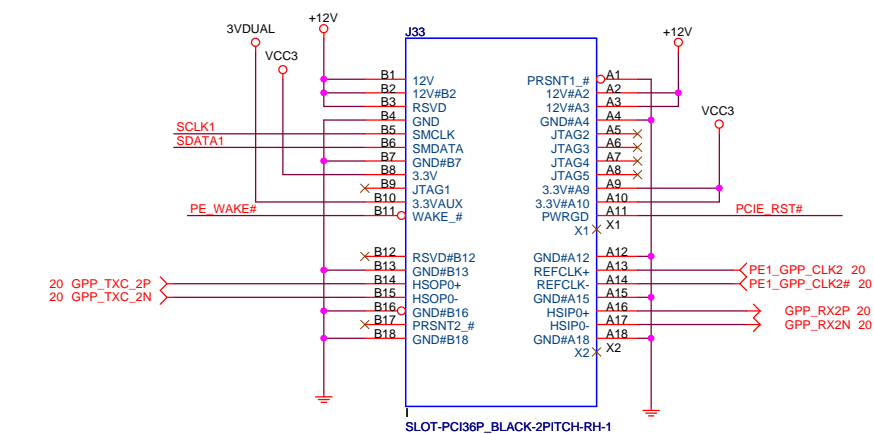
N11-0360251-F02

### PCI EXPRESS X1 Slot-2

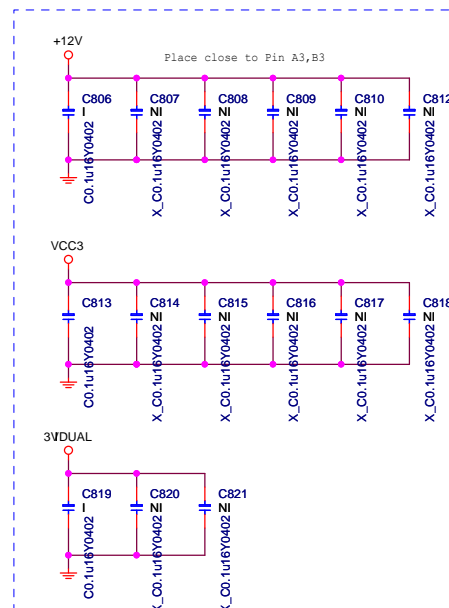


N11-0360251-F02

### PCI EXPRESS X1 Slot-3



N11-0360251-F02

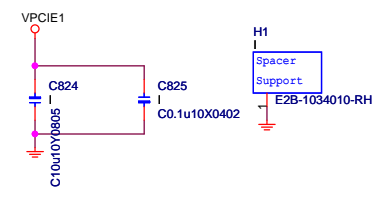
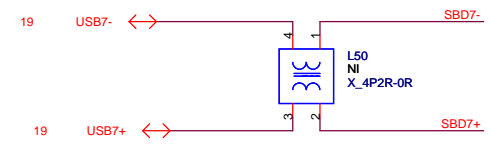
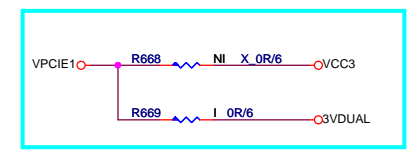
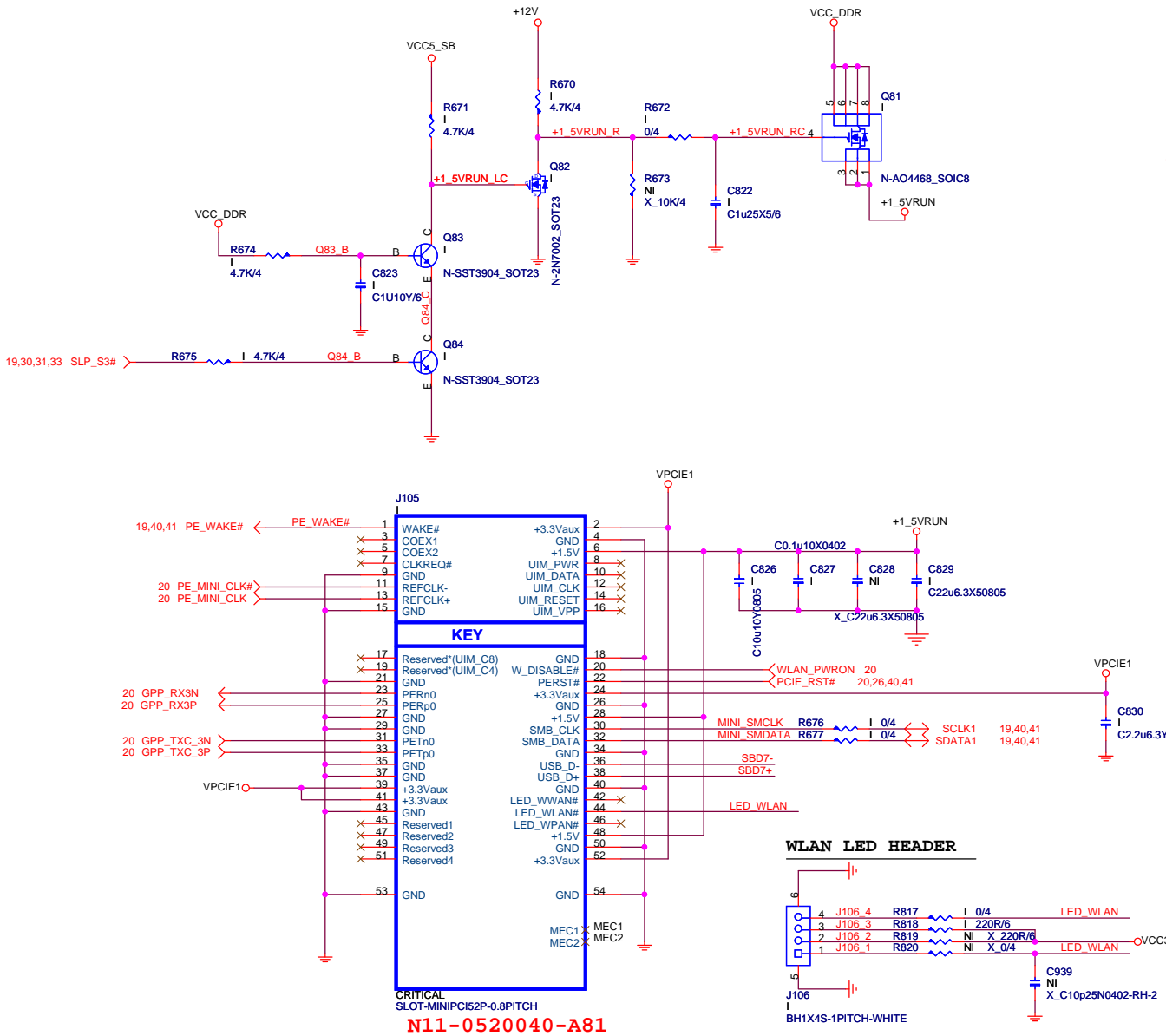


MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

Size Custom	Document Description <b>PCI E X1 SLOTS</b>	Rev 0A
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# Wireless LAN(Short Card)



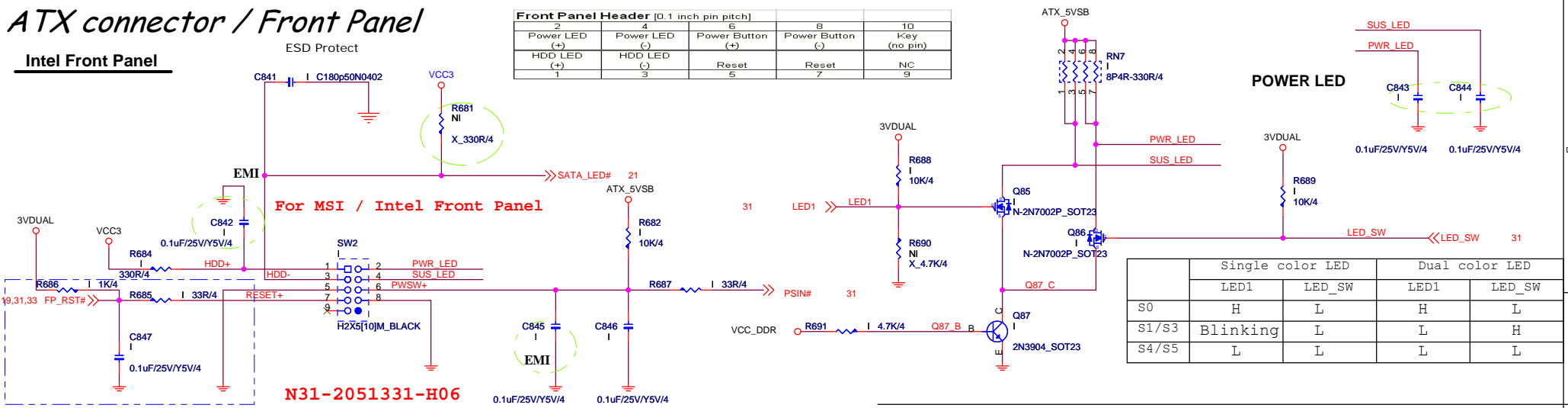
**N11-0520040-A81**

**N32-1040440-H06**

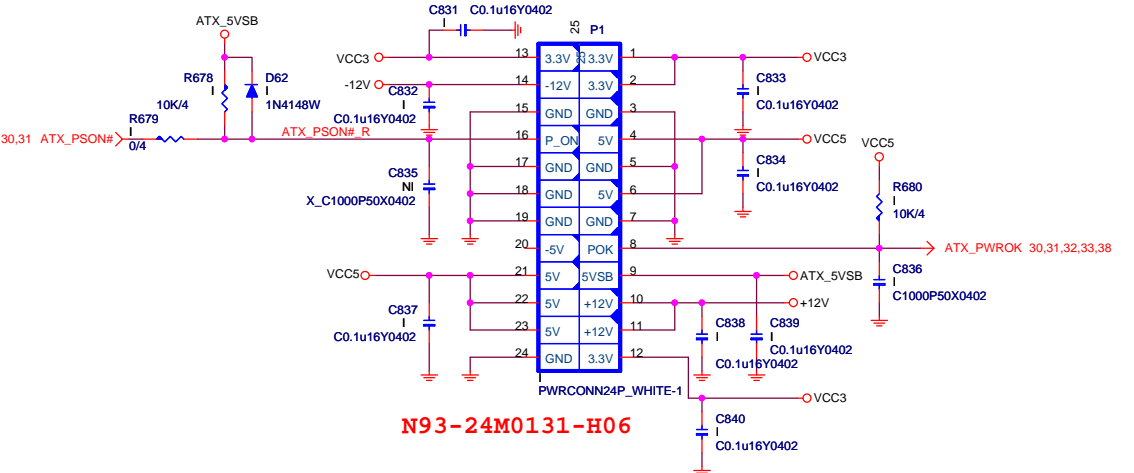
	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>HP SCH P/N: (MSI MS-7778)</b>	
	Size Custom	Document Description <b>PCIE X1 mini card</b>
Date:	Sheet 42 of 45	

# ATX connector / Front Panel

## Intel Front Panel



## ATX CONNECTOR

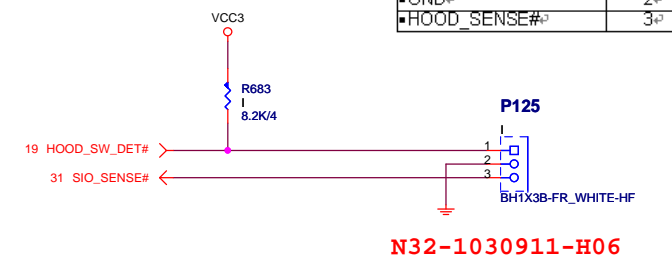


## HP Restricted Secret

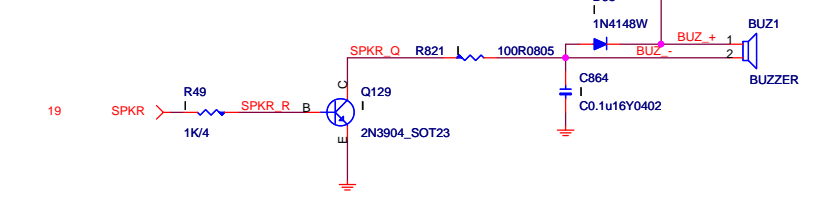
### HOOD SENSE

#### P125--HOOD-SENSE-HEADER-PIN-DESCRIPTION

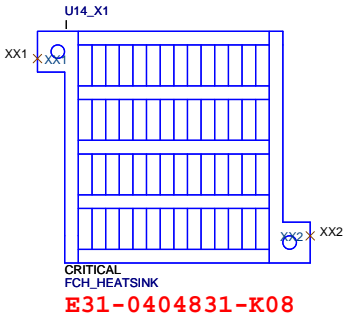
SIGNAL NAME	PIN #
HOOD_SW_DET#	1
GND	2
HOOD_SENSE#	3



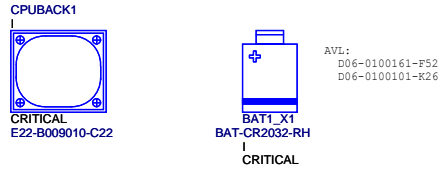
## BUZZER



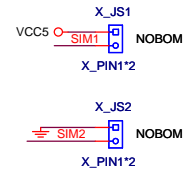
# HEAT SINK



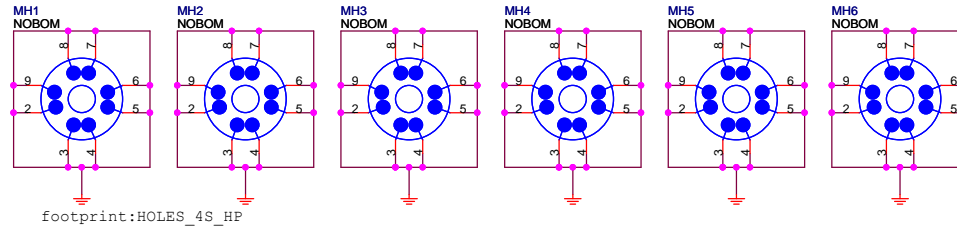
# MANUAL PART



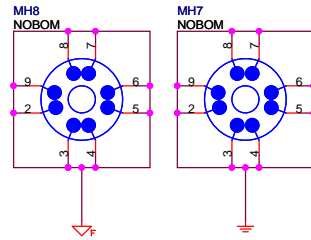
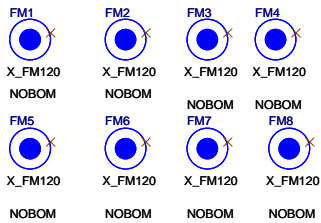
# Simulation



# Mounting Holes



# Optics Orientation Holes



MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

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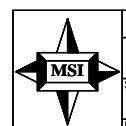
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