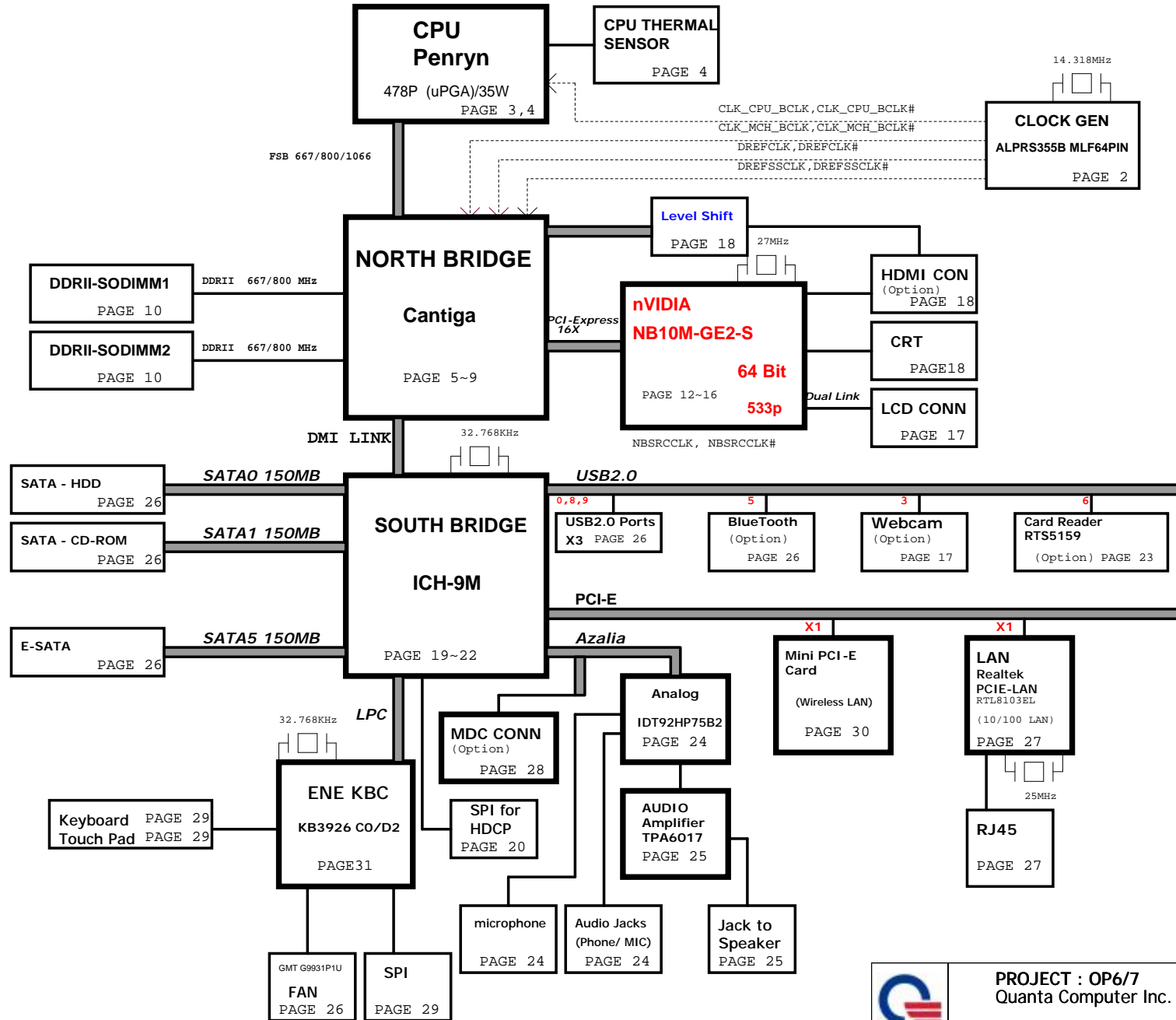



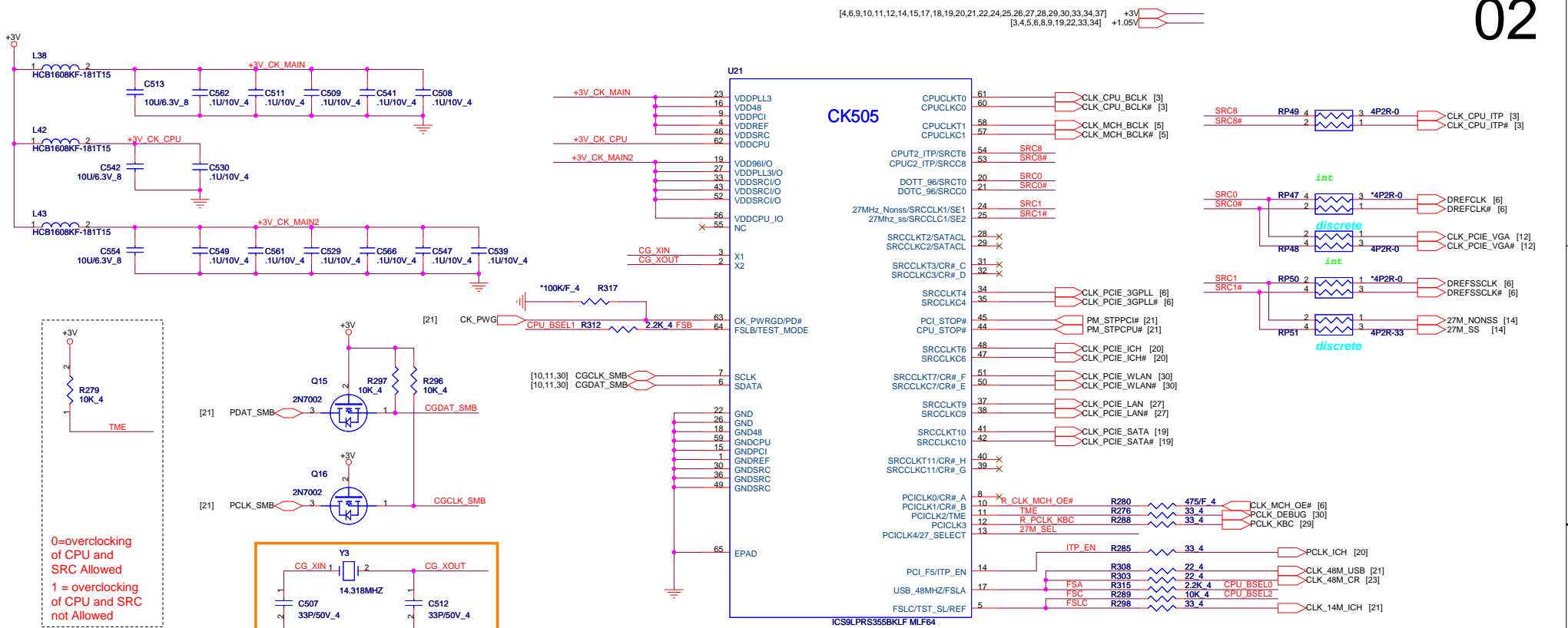
Tango/Ballet BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

- SYSTEM CHARGER (ISL6251AHAZ-T) PAGE 31
- SYSTEM POWER ISL6237IRZ-T PAGE 32
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 36
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 33
- CPU CORE ISL6266A PAGE 34



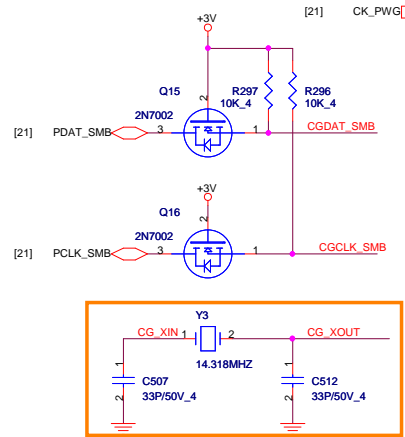
	PROJECT : OP6/7 Quanta Computer Inc.		Rev A
	Size Custom	Document Number Block Diagram	



0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC Not Allowed

0=UMA
1 = External VGA

Enable ITP CLK

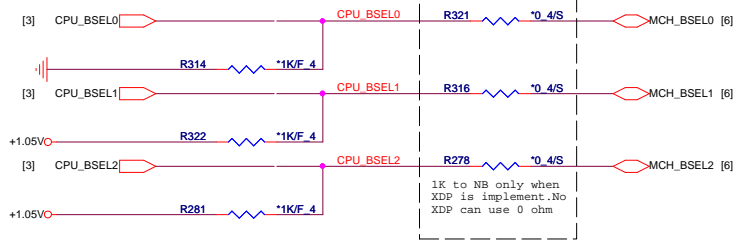


DB:Change from 27P to 33P(TXC suggestion)

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

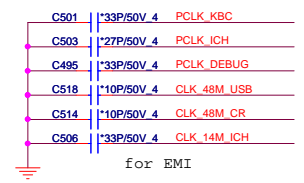
CK505 QFN64
 Siligo SLG8SP513VTR AL8SP513000
 Realtek RTM875N-606-VD-GR AL000875000

CPU Clock select



1K to NB only when XDP is implement.No XDP can use 0 ohm

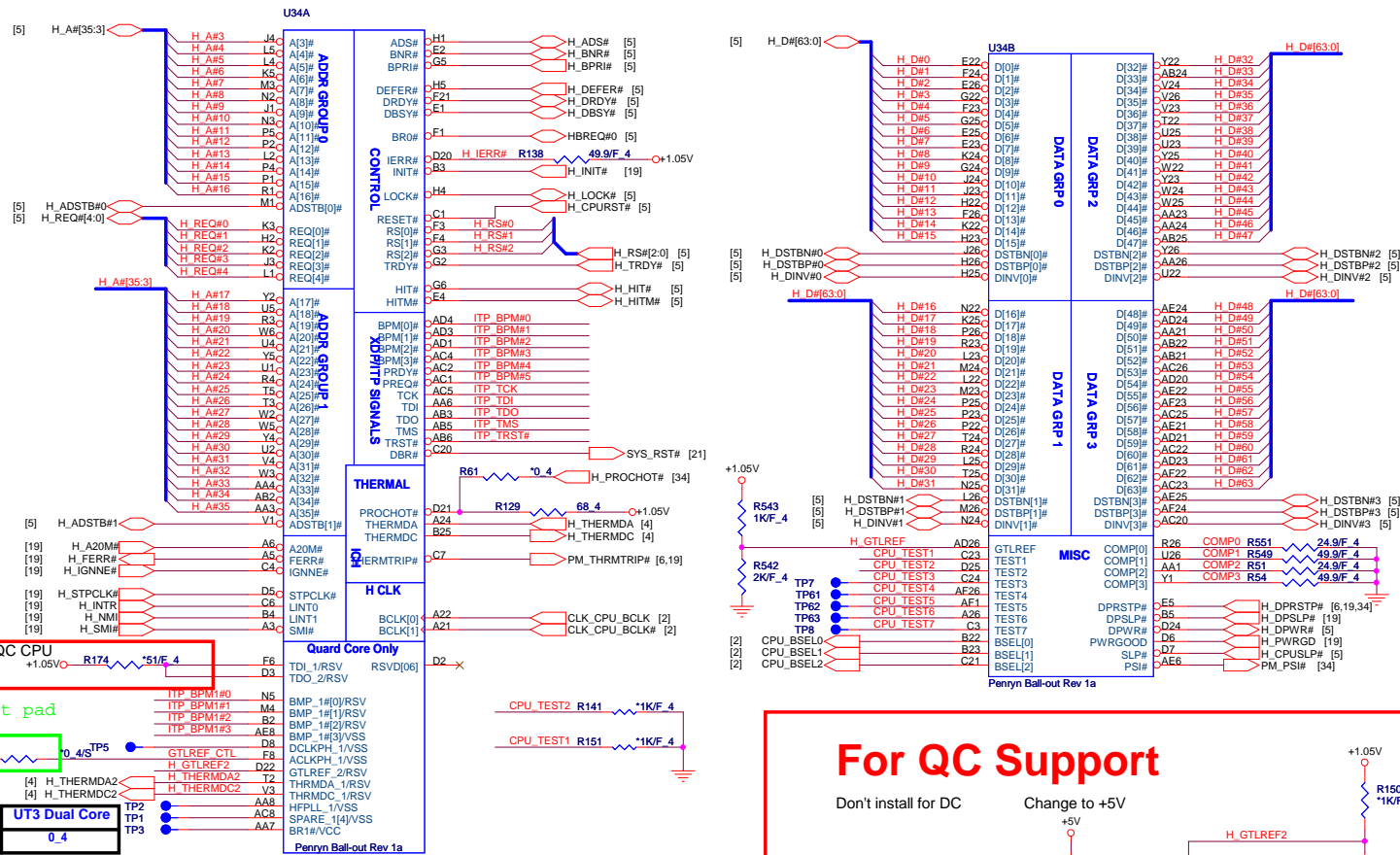
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



PROJECT : OP6/7
Quanta Computer Inc.

Size Custom	Document Number	Rev SI
Clock Generator		
Date: Tuesday, January 20, 2009	Sheet 2 of 37	

[2,4,5,6,8,9,19,22,33,34] +1.05V

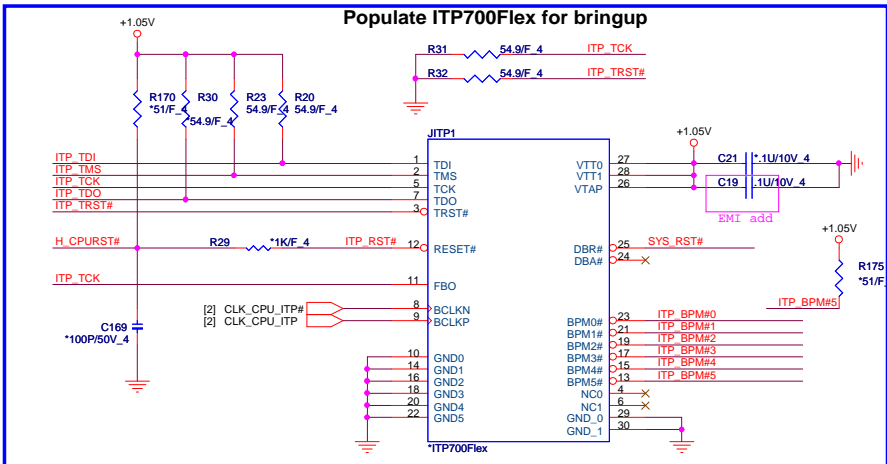
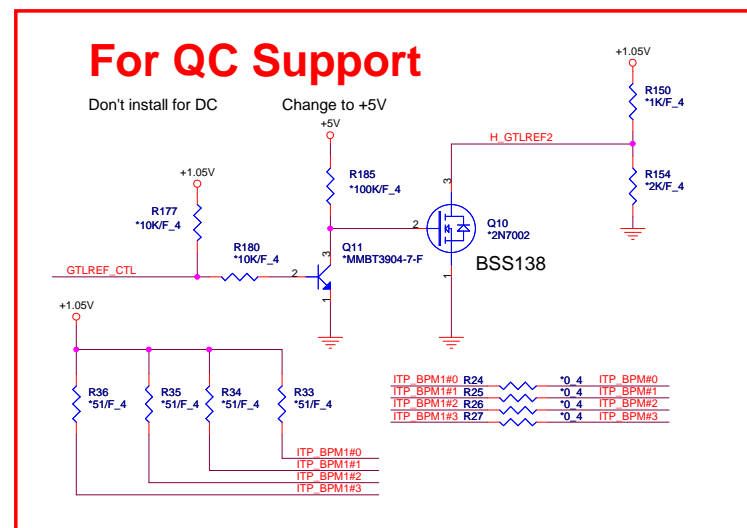



PV Stage: Change to short pad

For QC CPU
+1.05V \rightarrow R174 \rightarrow *51/F_4

R28 \rightarrow *0.4/TP5

CPU_TEST2 R141 \rightarrow *1K/F_4
CPU_TEST1 R151 \rightarrow *1K/F_4

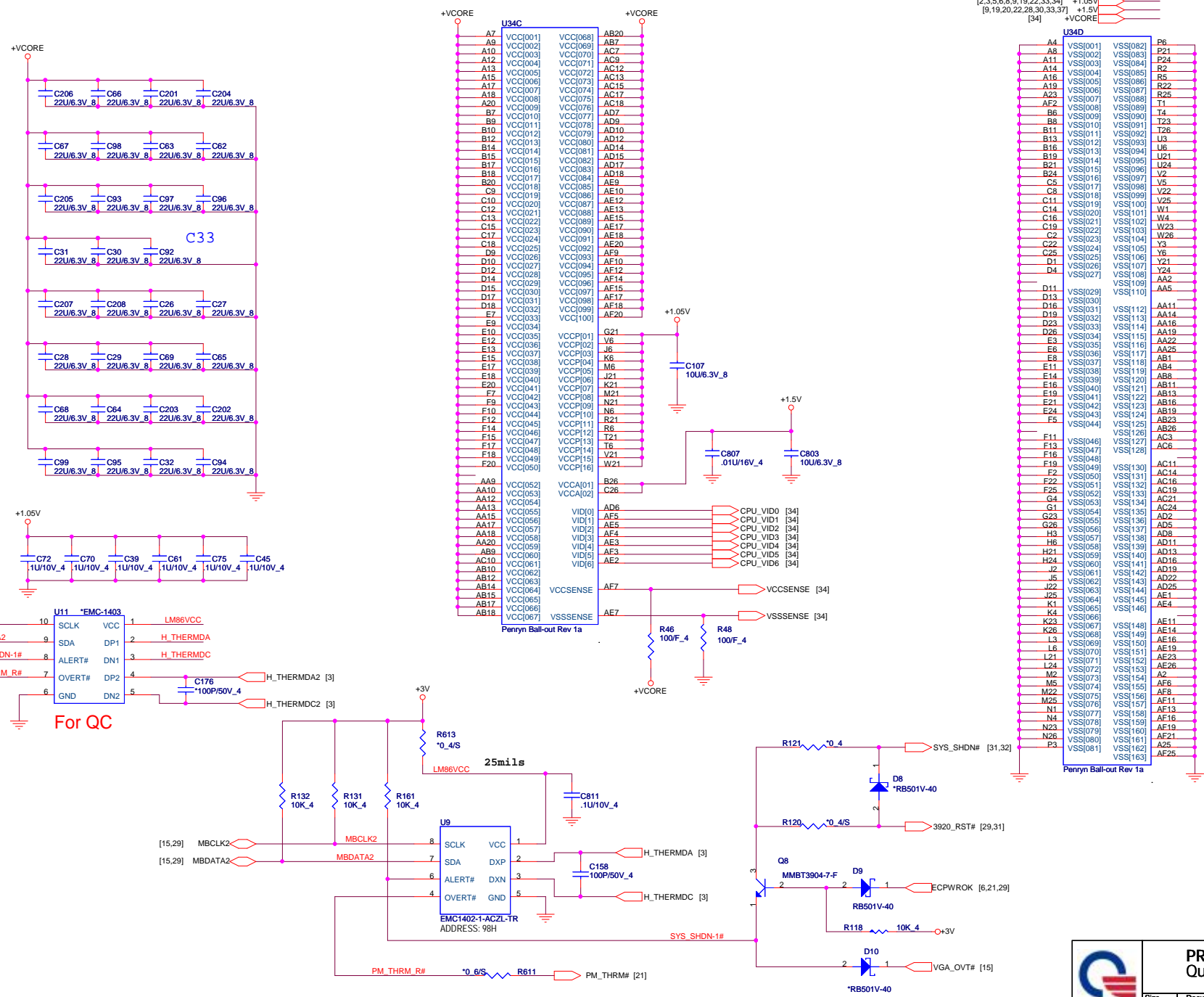


 PROJECT : OP6/7
Quanta Computer Inc.

Size Custom	Document Number Penryn 1/2	Rev SI
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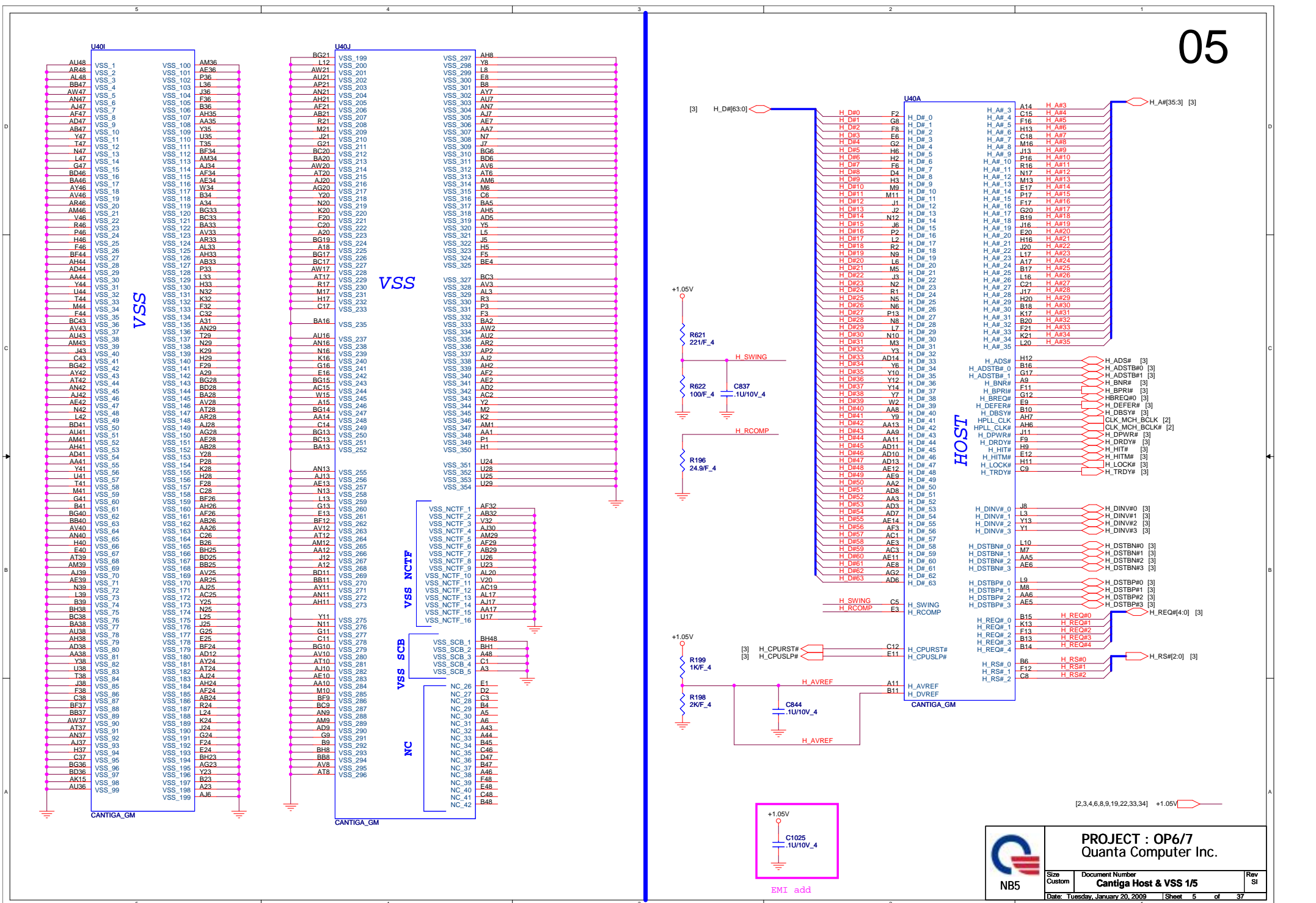
Date: Tuesday, January 20, 2009 | Sheet 3 of 37

[2,6,9,10,11,12,14,15,17,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37] +3V
[2,3,5,6,8,9,19,22,33,34] +1.05V
[9,19,20,22,28,30,33,37] +1.5V
[34] +VCCORE



PROJECT : OP6/7
Quanta Computer Inc.

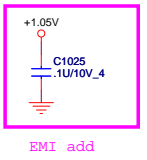
NB5	Size	Document Number	Rev
	Custom	Penryn & TH Monitor 2/2	SI
Date: Tuesday, January 20, 2009		Sheet 4 of 37	



PROJECT : OP6/7
Quanta Computer Inc.

Size Custom Document Number **Cantiga Host & VSS 1/5** Rev SI

Date: Tuesday, January 20, 2009 Sheet 5 of 37



[2,3,4,6,8,9,19,22,33,34] +1.05V

MCH_CFG_5 DMiX2 selection

Low: DMiX2
High: DMiX4 (Default)
MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved
MCH_CFG_6 ITPM Host Interface

Low: ITPM Host Interface enabled
High: ITPM Host Interface disabled (Default)
MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

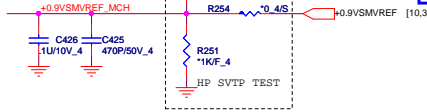
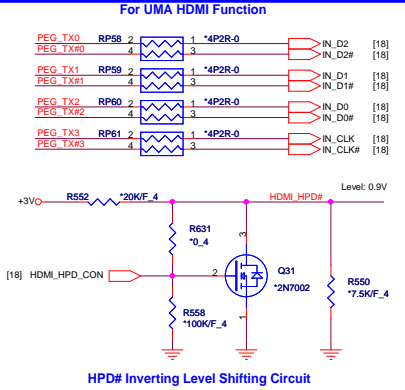
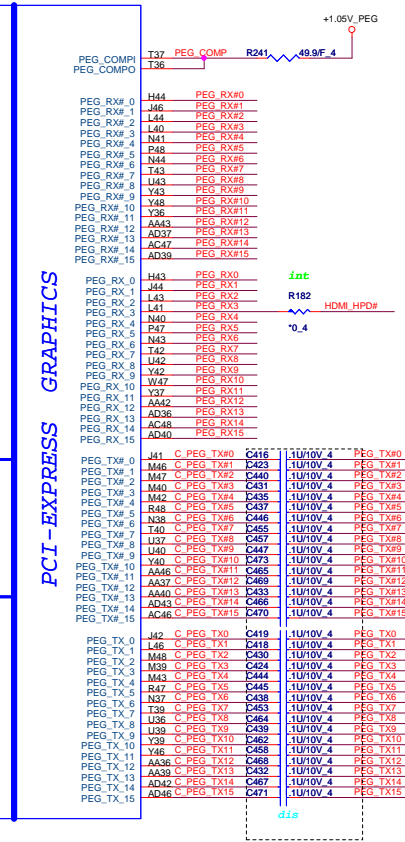
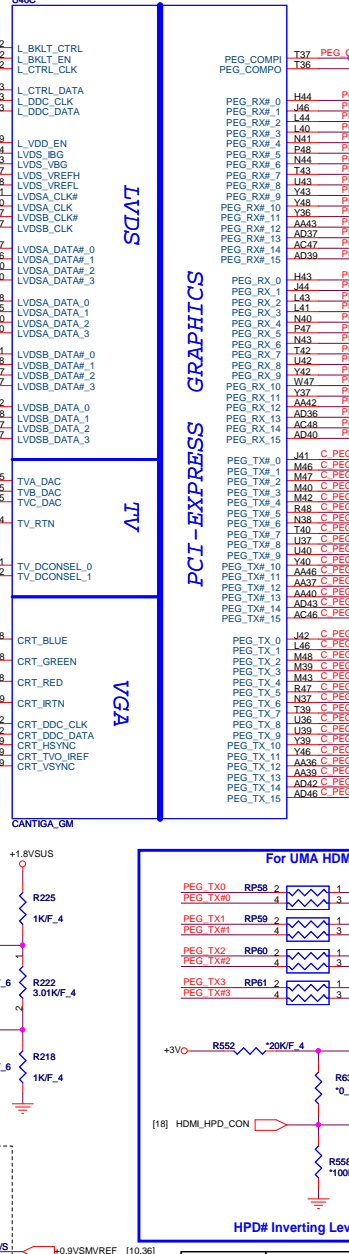
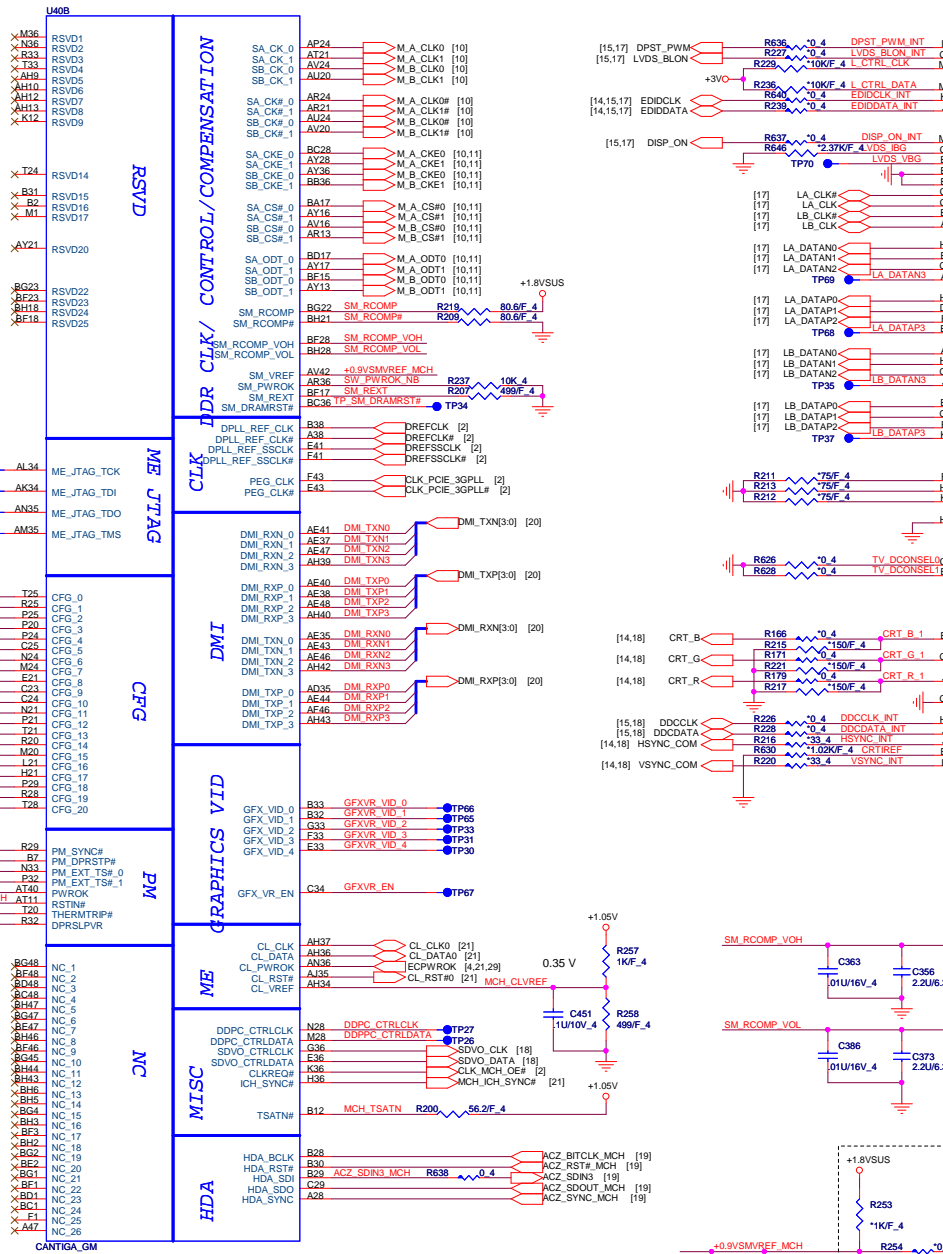
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration

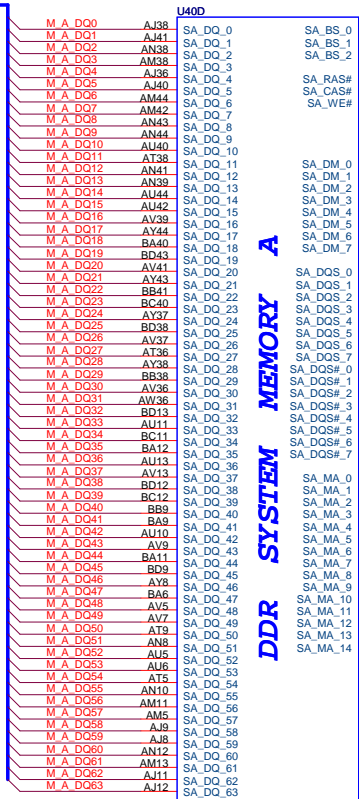
0	0	Reserved
0	1	XOR Mode enabled
1	0	All-Z Mode enabled
1	1	Normal operation (Default)

[2,4,9,10,11,12,14,15,17,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37] +3V
 [8,9,10,28,33,36] +1.8VSUS
 [2,3,4,5,8,9,19,22,33,34] +1.05V_PEG
 [2,3,4,5,8,9,19,22,33,34] +1.05V_PEG

PEG_TX#(15:0) → PEG_TX#(15:0) [12]
 PEG_TX15(0) → PEG_TX15(0) [12]
 PEG_RX#(15:0) → PEG_RX#(15:0) [12]
 PEG_RX15(0) → PEG_RX15(0) [12]

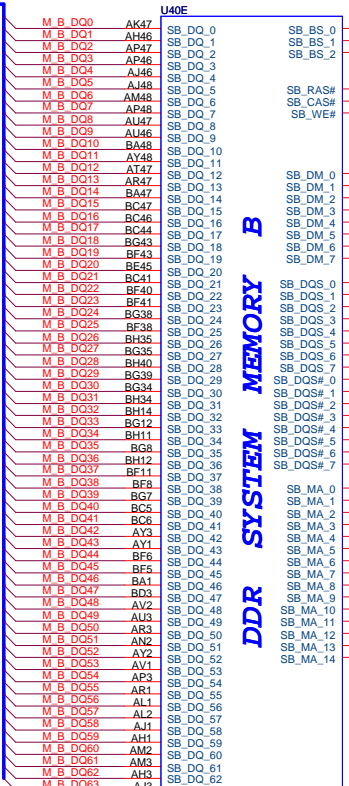


[10] M_A_DQ[63:0]



CANTIGA_GM

[10] M_B_DQ[63:0]



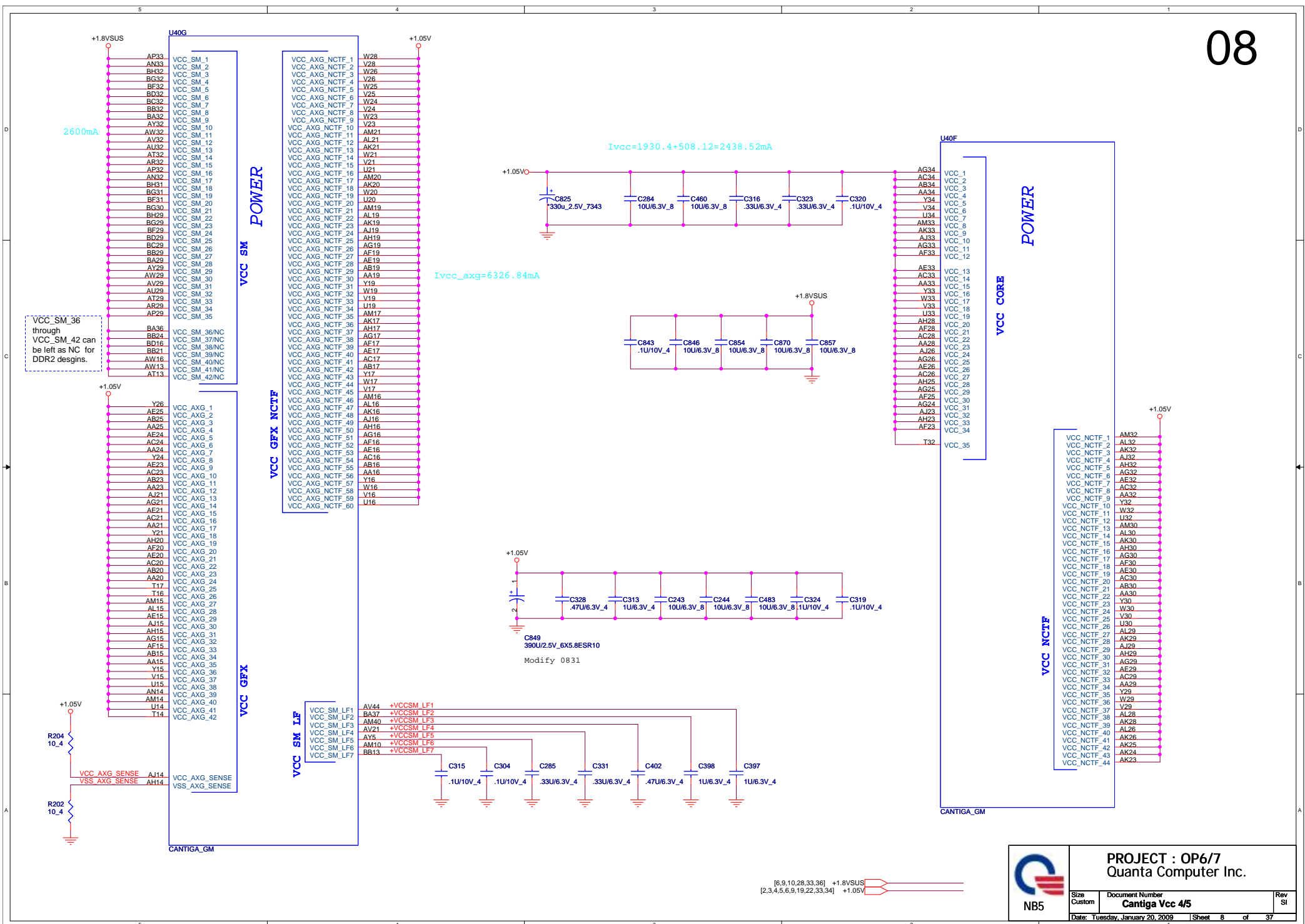
CANTIGA_GM

PROJECT : OP6/7
Quanta Computer Inc.

Size Custom Document Number
Cantiga DDR2 3/5

Date: Tuesday, January 20, 2009 Sheet 7 of 37

NB5 Rev SI



VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desigs.

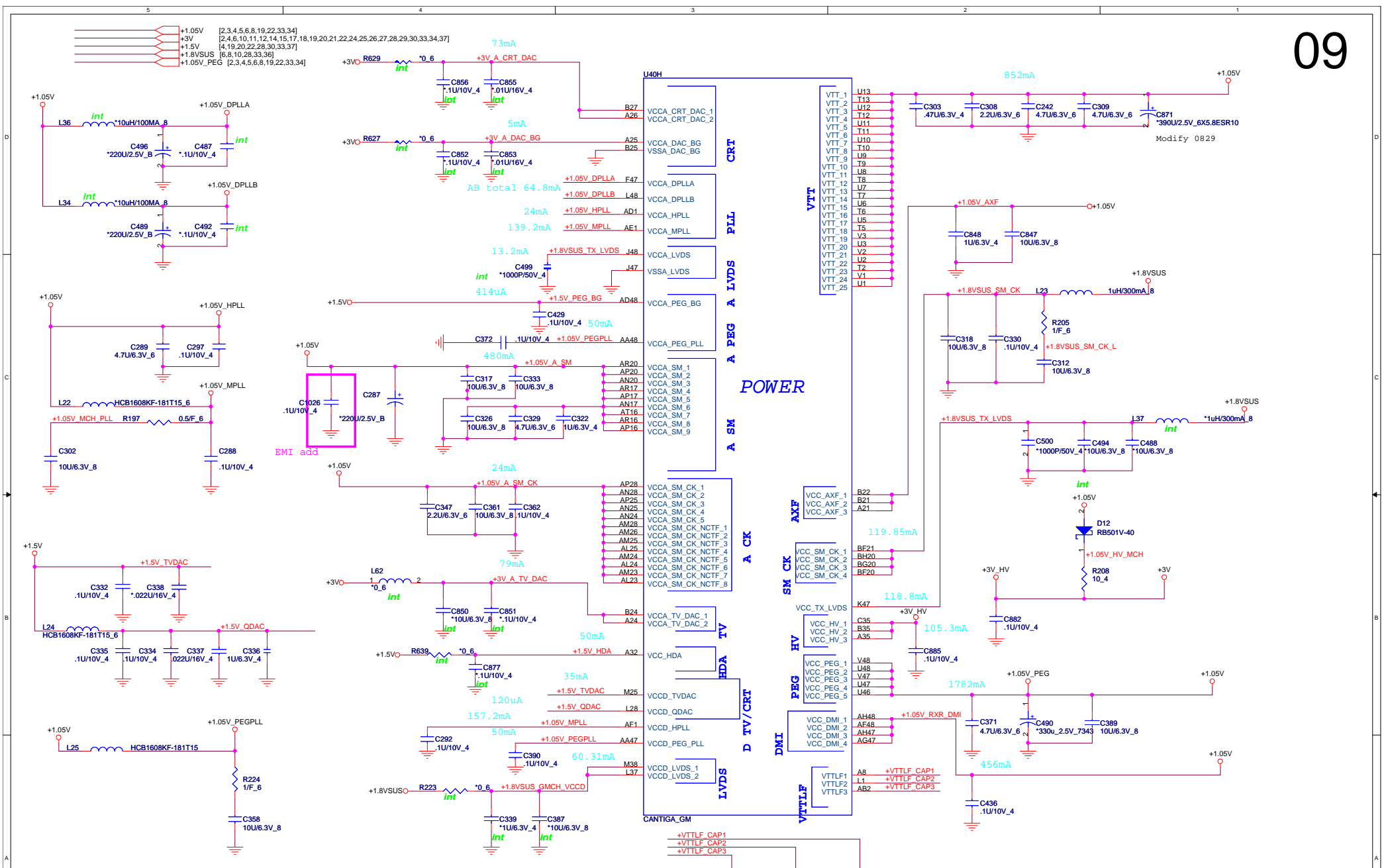
Ivcc=1930.4+508.12=2438.52mA

Ivcc_axg=6326.84mA


Modify 0831

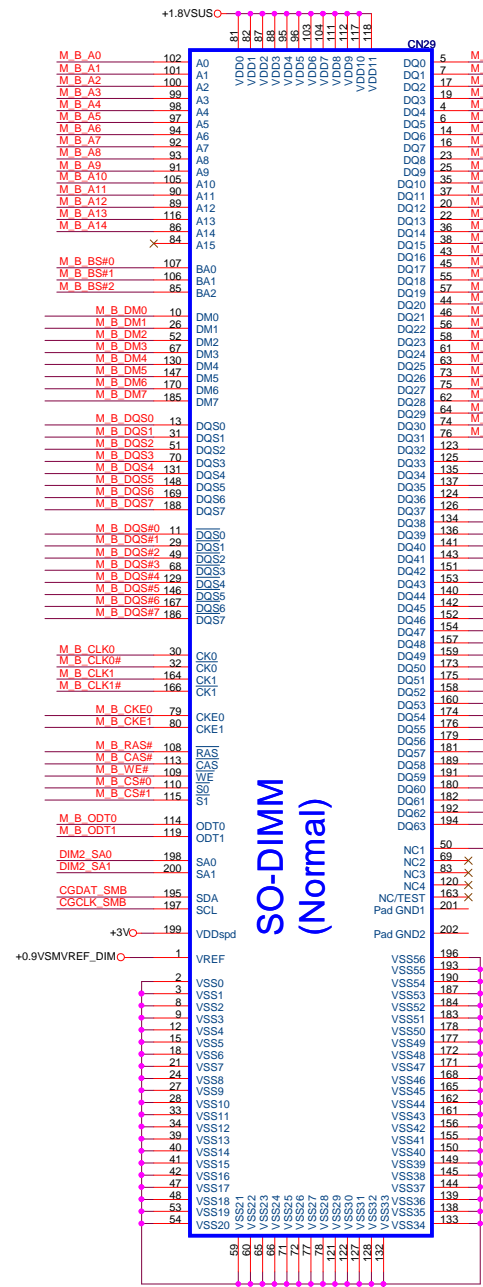


	PROJECT : OP6/7 Quanta Computer Inc.		
	Size Custom	Document Number Cantiga Vcc 4/5	Rev SI
	Date: Tuesday, January 20, 2009		Sheet 8 of 37



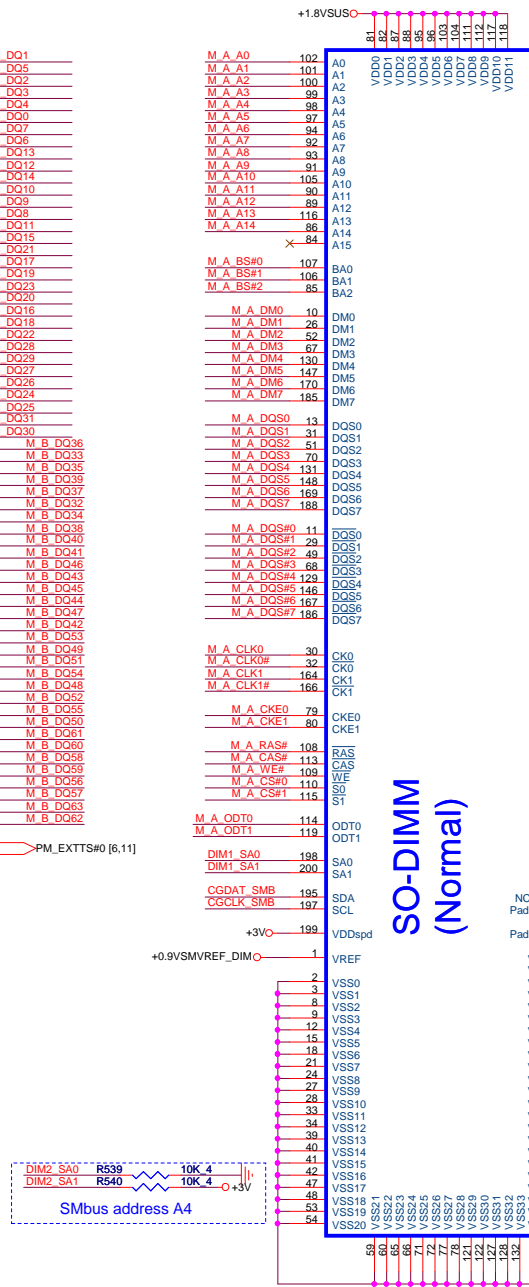
Modify to U40#AF1 power to +1.05V_MPLL as CRB change

	PROJECT : OP6/7 Quanta Computer Inc.		Rev SI
	Size Custom	Document Number Cantiga Power 5/5	Date: Tuesday, January 20, 2009 Sheet 9 of 37



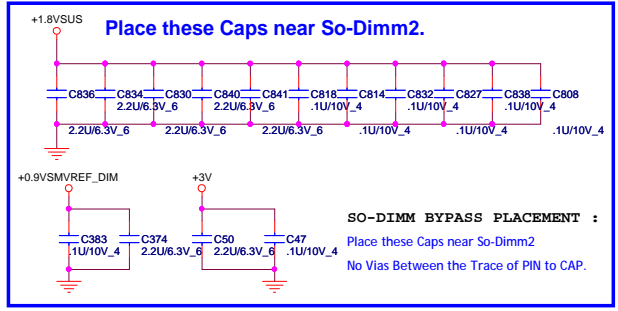
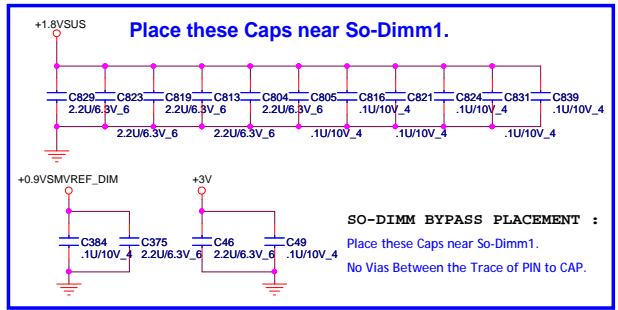
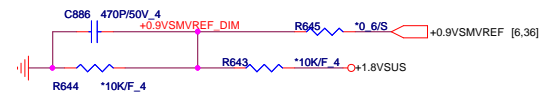
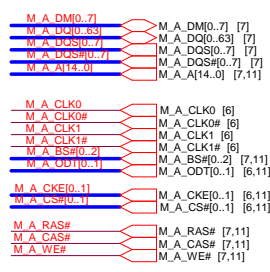
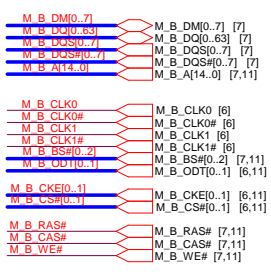
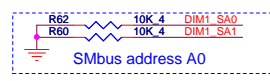
SO-DIMM (Normal)

H 9.2



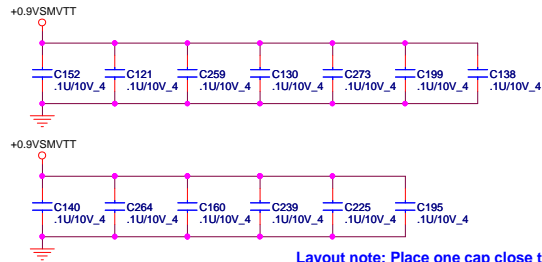
SO-DIMM (Normal)

H 5.2



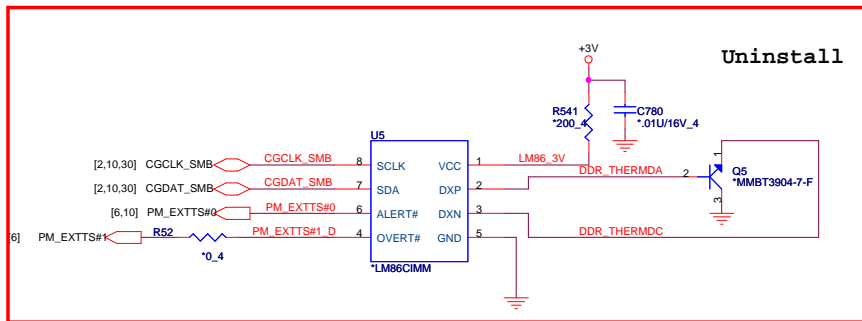
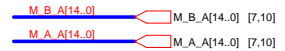
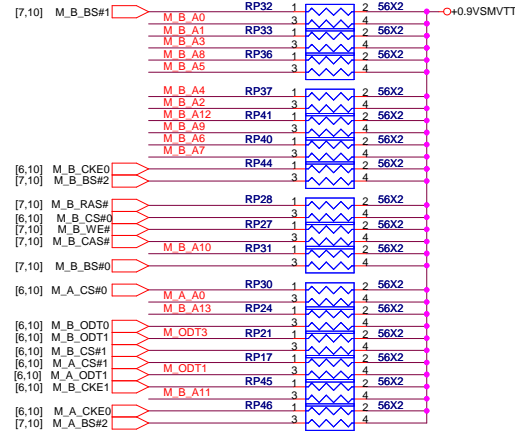
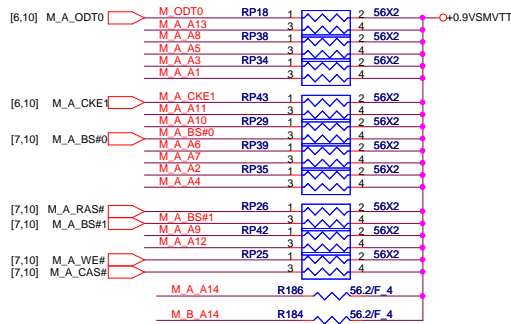
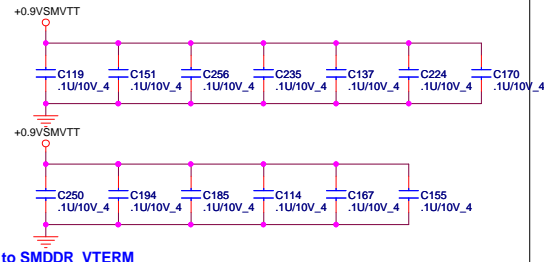
DDRII DUAL CHANNEL A,B.

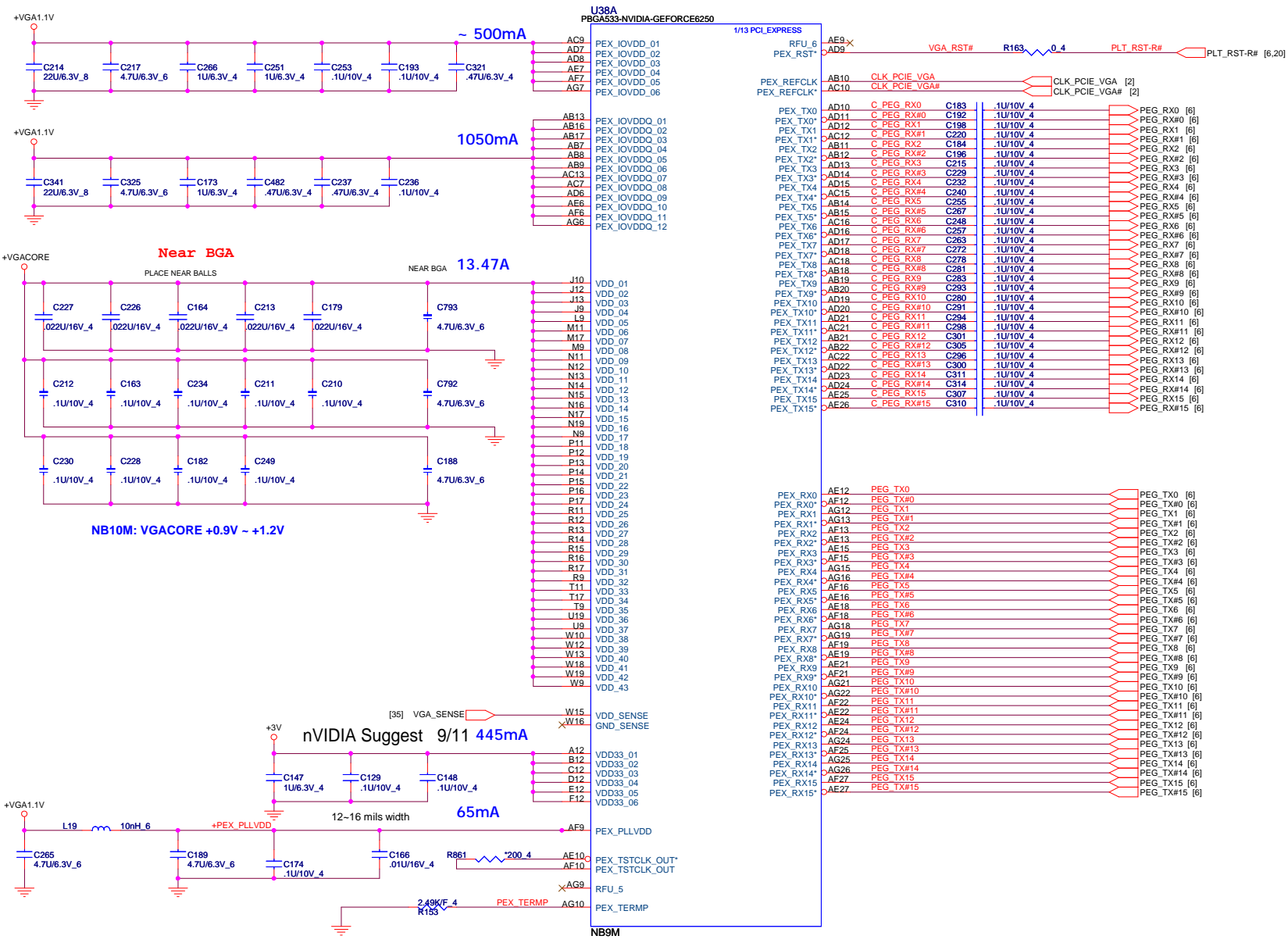
DDRII A CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII B CHANNEL





PROJECT : OP6/7
Quanta Computer Inc.

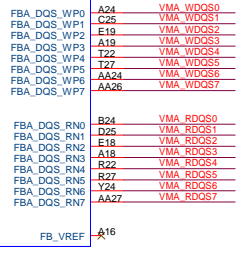
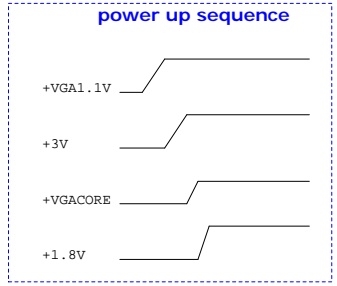
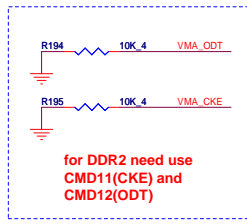
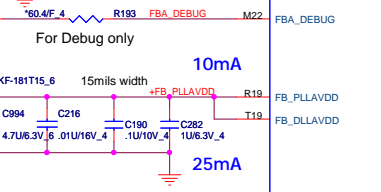
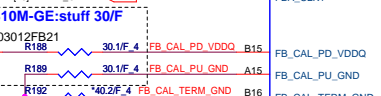
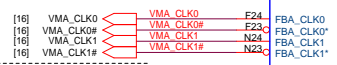
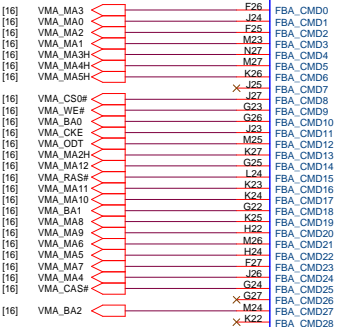
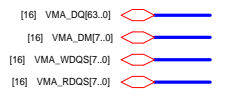
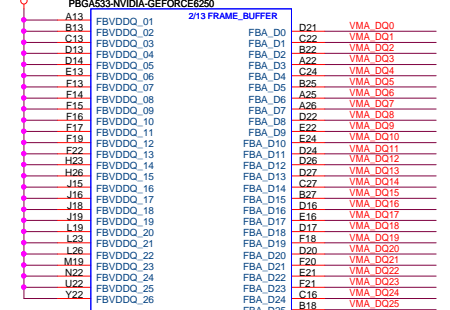
NB5

Size Custom Document Number **NV10M (PCIe I/F) 1/5** Rev DB

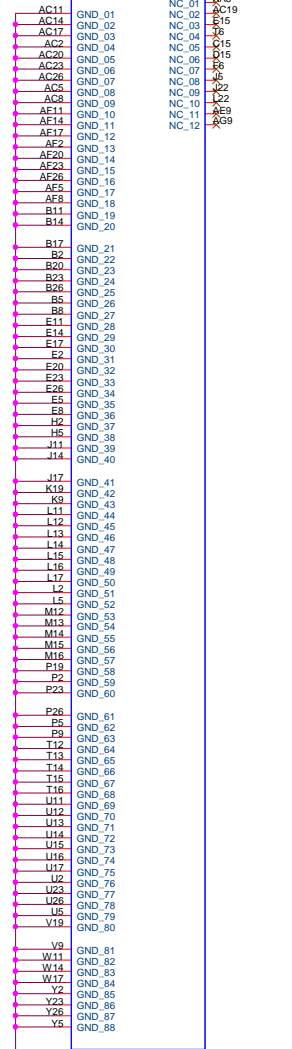
Date: Tuesday, January 20, 2009 | Sheet 12 of 37

U38B
PBG533-NVIDIA-GEFORCE6250

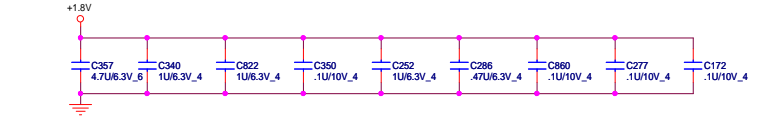
1.75A



U38J
PBG533-NVIDIA-GEFORCE6250

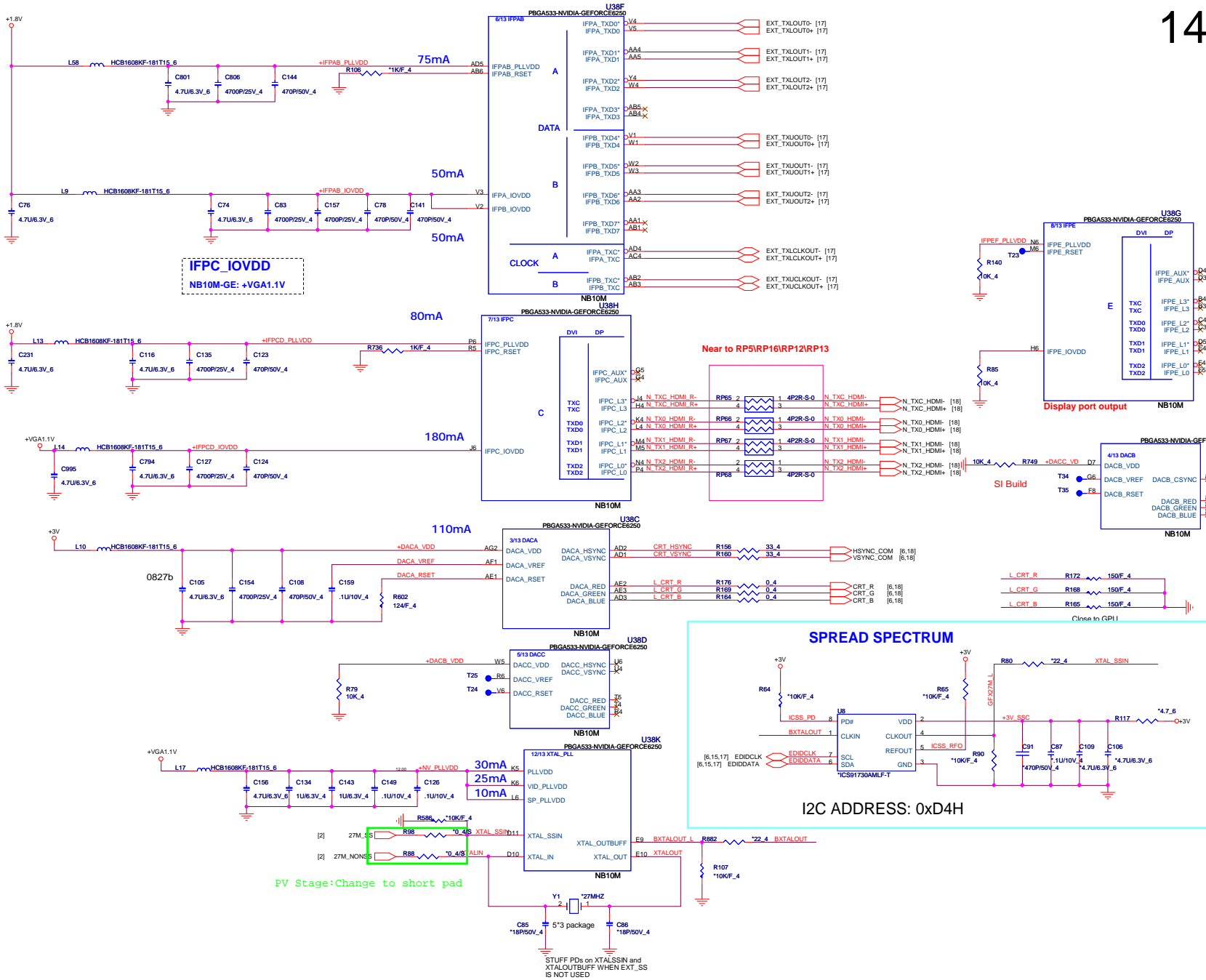


NB10M



PROJECT : OP6/7
Quanta Computer Inc.

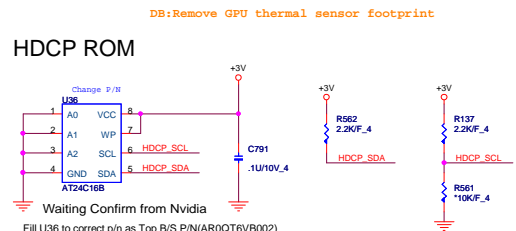
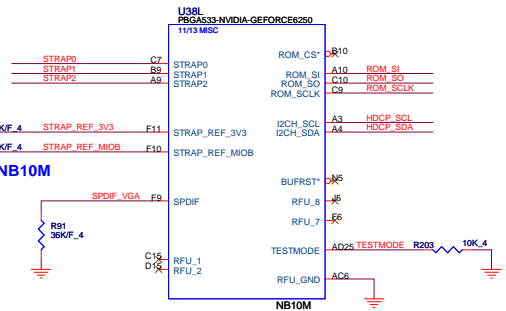
NB5	Size	Document Number	Rev
	Custom	NV10M (MEMORY IF) 2/5	DB
Date:	Tuesday, January 20, 2009	Sheet	13 of 37



Install it when not connected to Spread spectrum device

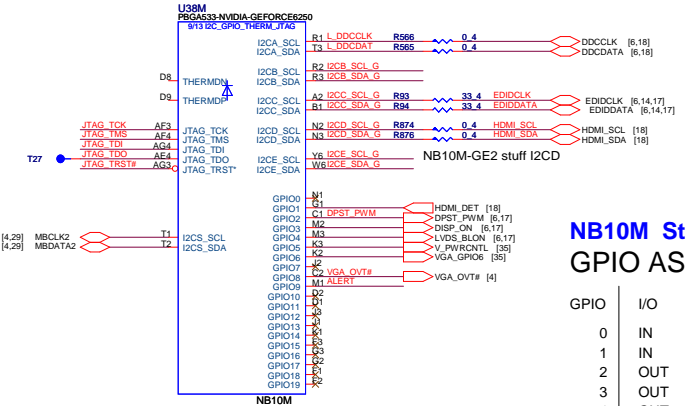
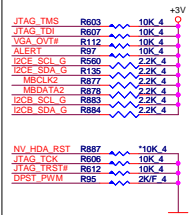
PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10M (DISPLAY) 3/5	D6
Date: Tuesday, January 20, 2009	Sheet 14 of 37	



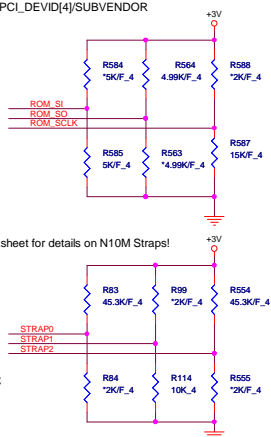
DHCP ROM	
HDCP_SCL	Low: Crypto ROM
	Hi: I2C ROM

Waiting Confirm from Nvidia
Fill U36 to correct p/in as Top B/S P/N(AR0QT6VB002)



NB10M Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



RAM ID: **ROM_SI R585**
64M*16 HYN **0000 PD 5K**
 SAM **0001 PD 10K**
 QIM **0010 PD 15K**

PCI_DEVID: **STRAP2 R554**
 NB10M-GE2 0x6EF **8 1111 PU 45K**

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

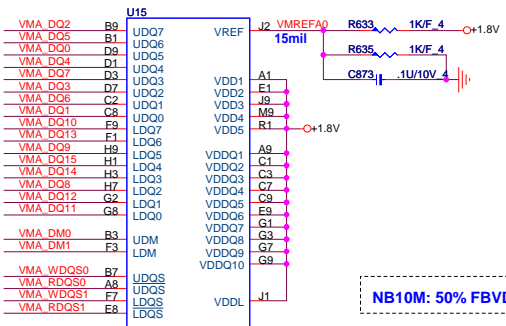
	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[0]

NB10M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 64Mx16x4, 64bit, 512MB	Hynix H5PS1G63EFR-20L
0001	DDR2 64Mx16x4, 64bit, 512MB	Samsung K4N1G164QG-HC20
0010	DDR2 64Mx16x4, 64bit, 512MB	Qimonda HY618T1G161C2P-20

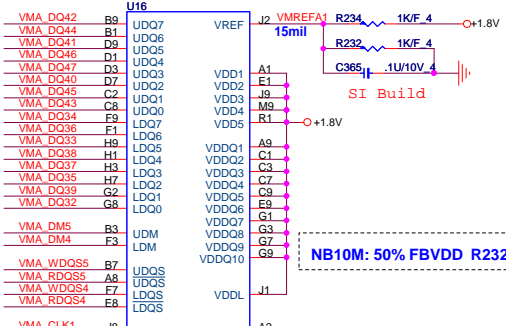
PROJECT : OP6/7
 Quanta Computer Inc.

Size	Document Number	Rev
C	NV10M (GPIO & STRAPS) 4/5	DB
Date: Tuesday, January 20, 2009 Sheet 15 of 37		



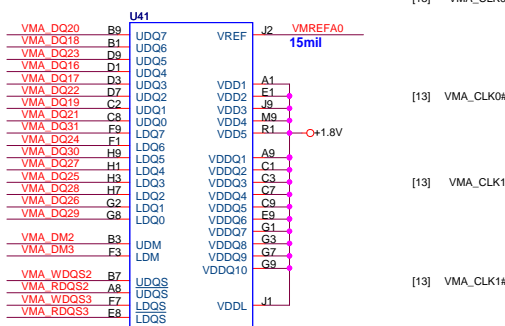
NB10M: 50% FBVDD R232 (1K)

Hynix HY5PS1G1631CFR-25 64Mx16
Samsung K4N1G164QQ-HC25 64Mx16

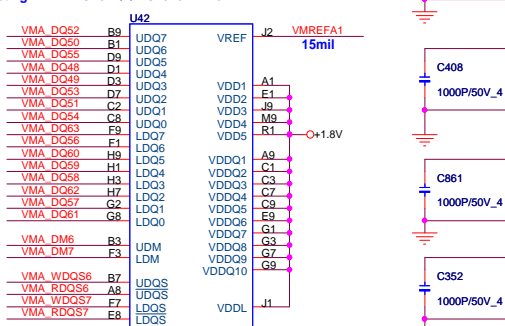


NB10M: 50% FBVDD R232 (1K)

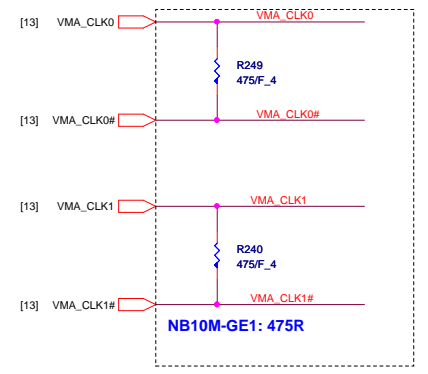
Hynix HY5PS1G1631CFR-25 64Mx16
Samsung K4N1G164QQ-HC25 64Mx16



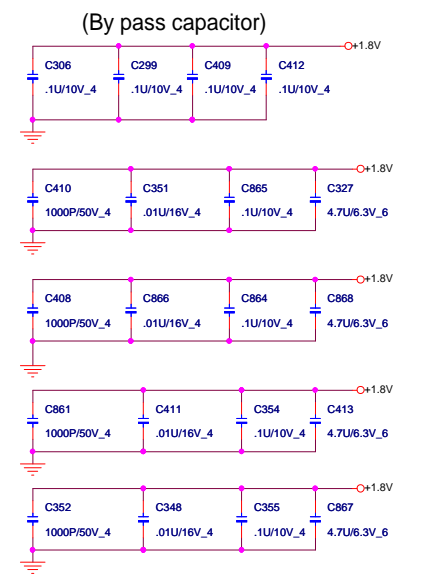
Hynix HY5PS1G1631CFR-25 64Mx16
Samsung K4N1G164QQ-HC25 64Mx16



Hynix HY5PS1G1631CFR-25 64Mx16
Samsung K4N1G164QQ-HC25 64Mx16



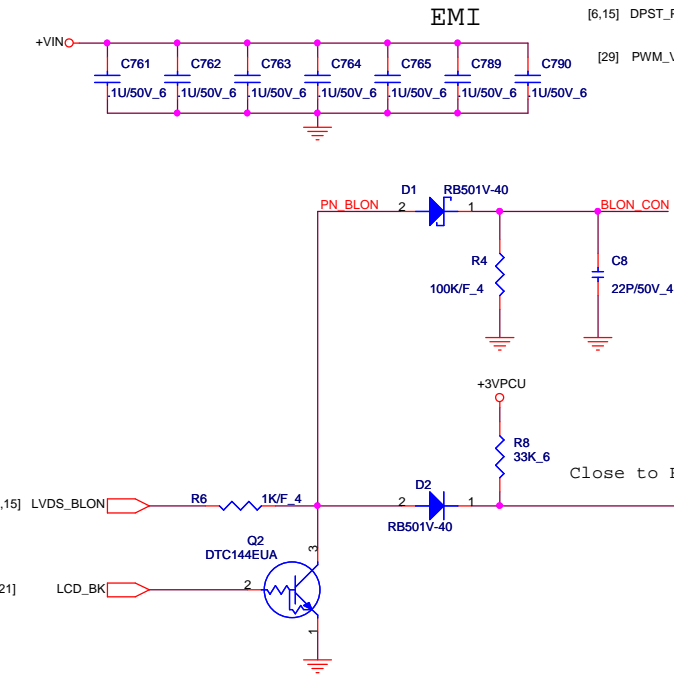
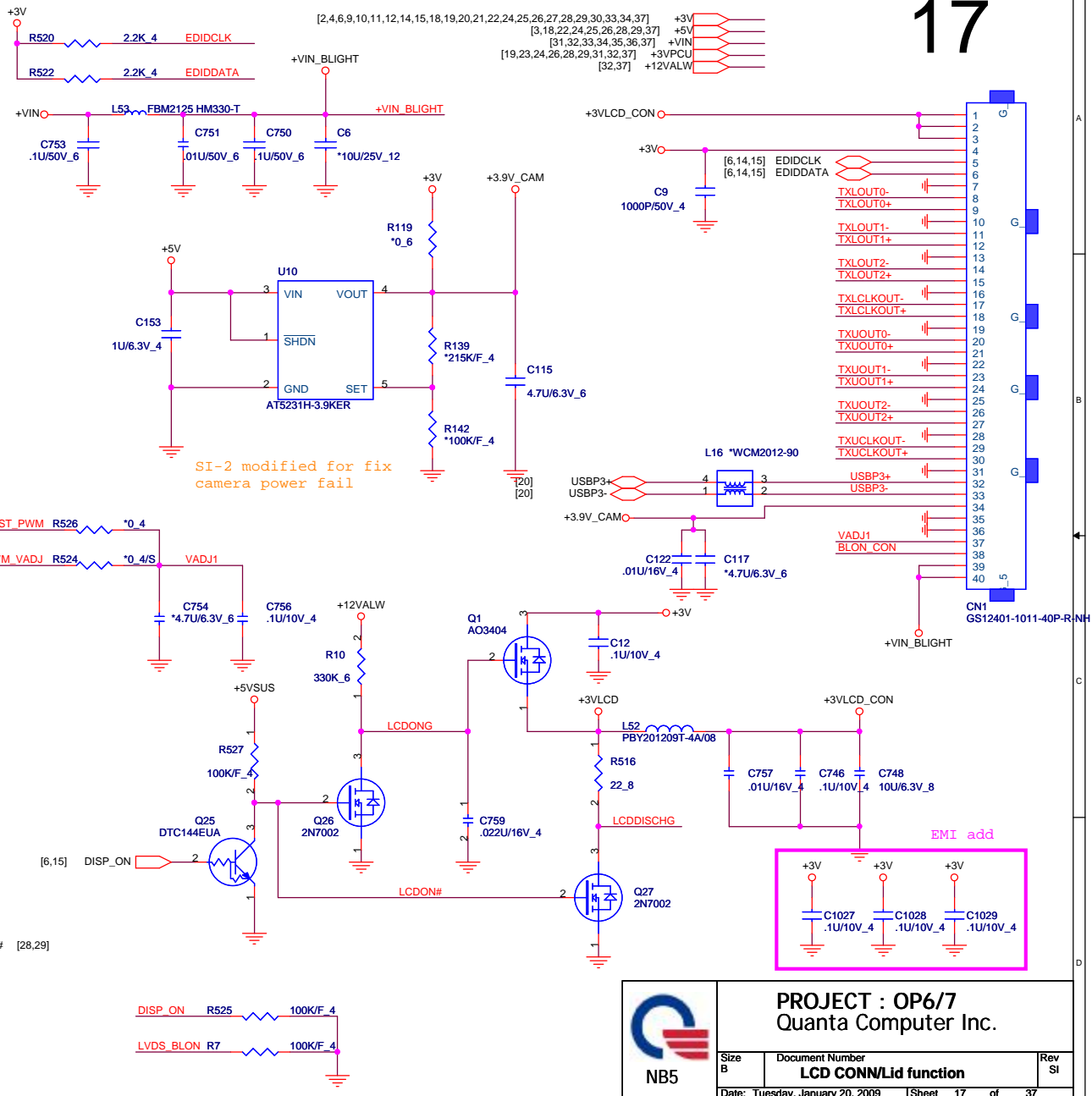
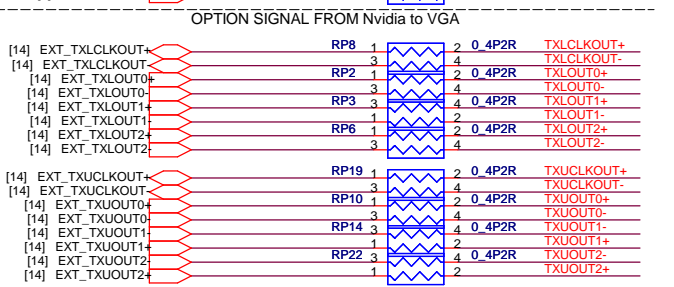
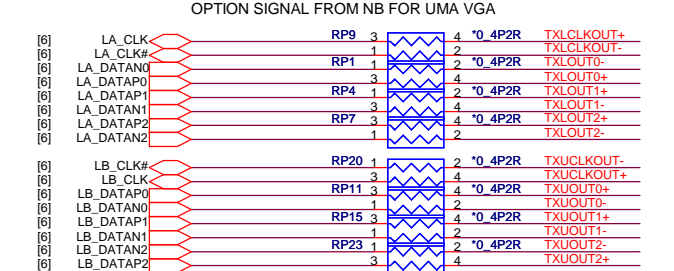
CS14752FB11 RES CHIP 475 1/16W +1% (0402)



- [13] VMA_DQ[63..0]
 - [13] VMA_DM[7..0]
 - [13] VMA_WDSQ[7..0]
- 256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01

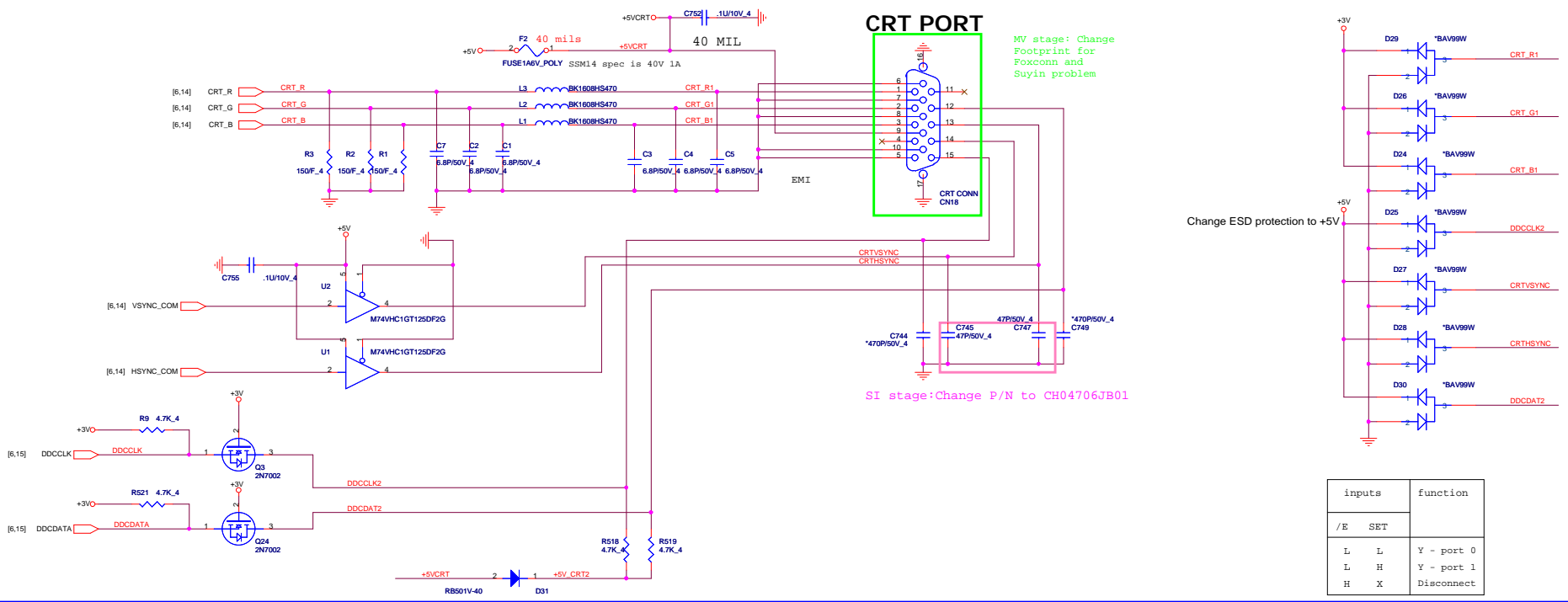


1. If LCD connector near GPU, then place these series Resistors near GPU
 2. If LCD connector near N/B, then place these series Resistors near N/B

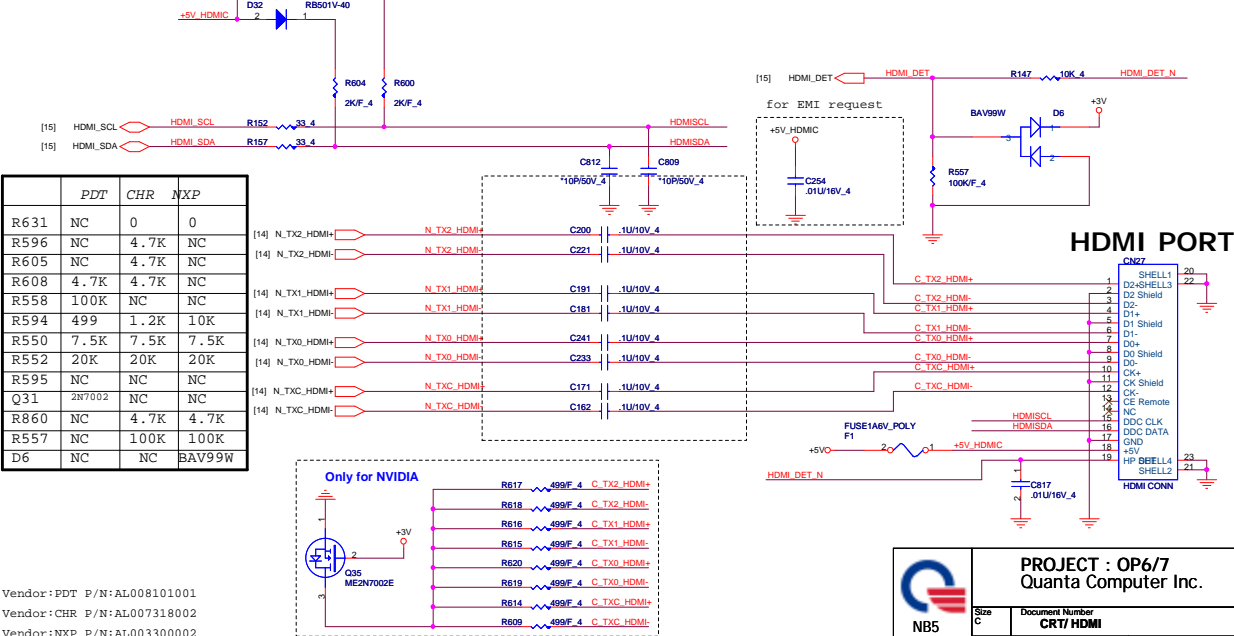
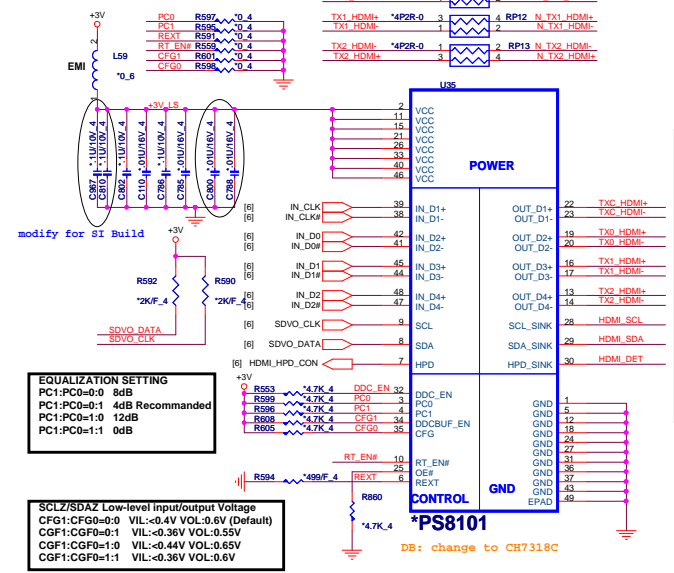


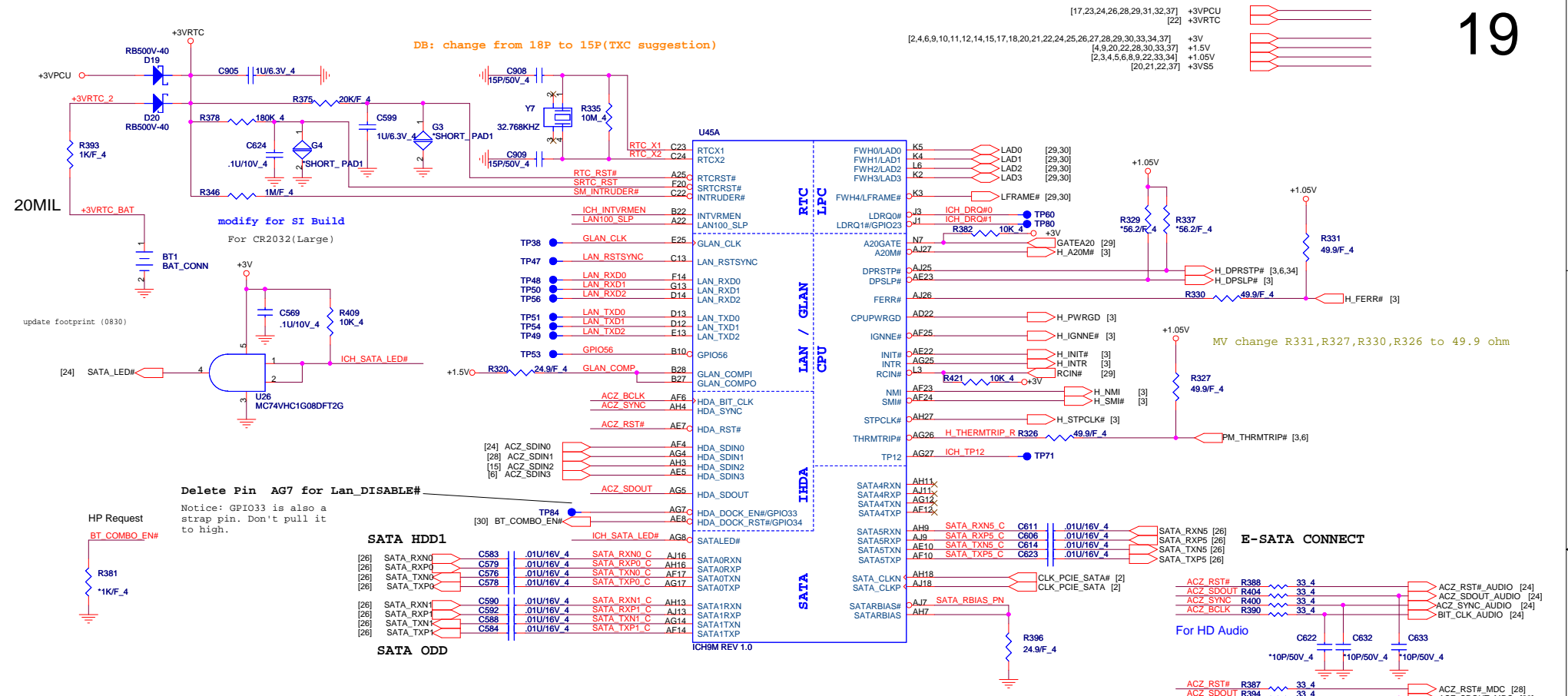
PROJECT : OP6/7
Quanta Computer Inc.

Size B	Document Number LCD CONN/Lid function	Rev SI
Date: Tuesday, January 20, 2009 Sheet 17 of 37		



For UMA HDMI function





Delete Pin AG7 for Lan_DISABLE#
 Notice: GPIO33 is also a strap pin. Don't pull it to high.

SATA HDD1

[26] SATA_RXN0	C583	.01U/16V_4	SATA_RXN0_C	AJ16
[26] SATA_RXP0	C579	.01U/16V_4	SATA_RXP0_C	AH16
[26] SATA_TXN0	C576	.01U/16V_4	SATA_TXN0_C	AF17
[26] SATA_TXP0	C578	.01U/16V_4	SATA_TXP0_C	AG17
[26] SATA_RXN1	C590	.01U/16V_4	SATA_RXN1_C	AH13
[26] SATA_RXP1	C592	.01U/16V_4	SATA_RXP1_C	AJ13
[26] SATA_TXN1	C588	.01U/16V_4	SATA_TXN1_C	AG14
[26] SATA_TXP1	C584	.01U/16V_4	SATA_TXP1_C	AF14

SATA ODD

[24] ACZ_SDIN0	AF4
[28] ACZ_SDIN1	AH4
[15] ACZ_SDIN2	AH3
[6] ACZ_SDIN3	AE5
[30] BT_COMBO_EN#	TP84

SB Strap

ICH9-M Internal VR Enable strap
 (Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

NTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

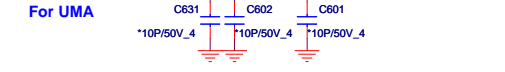
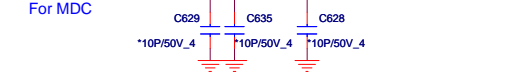
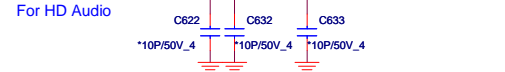
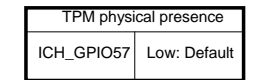
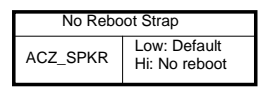
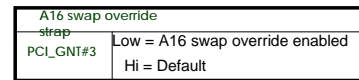
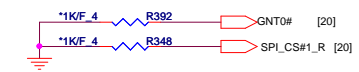
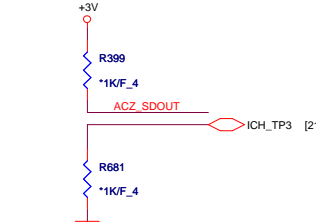
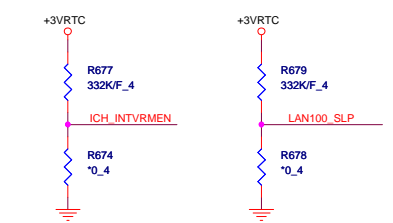
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS

SPI	0	1
PCI	1	0
LPC	1	1

(default)



PROJECT : OP6/7
Quanta Computer Inc.

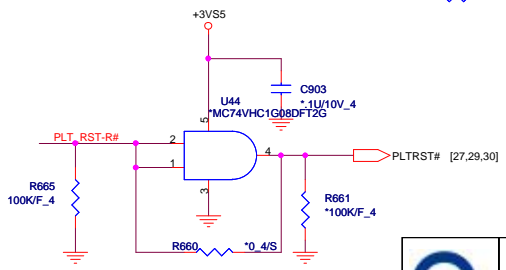
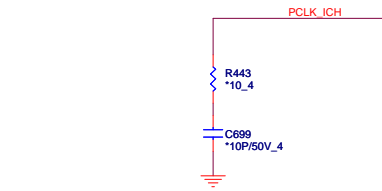
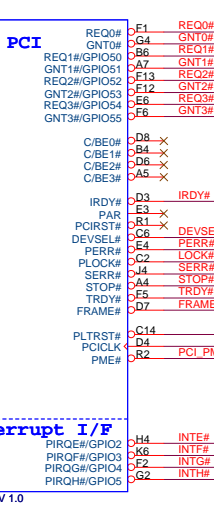
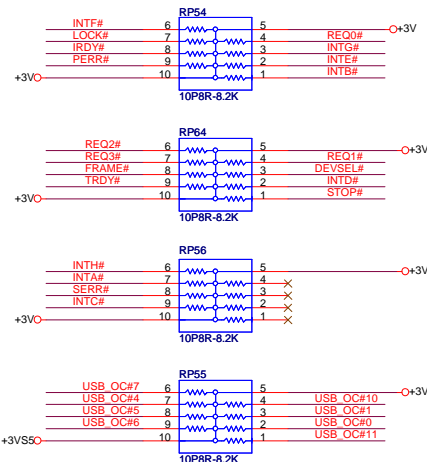
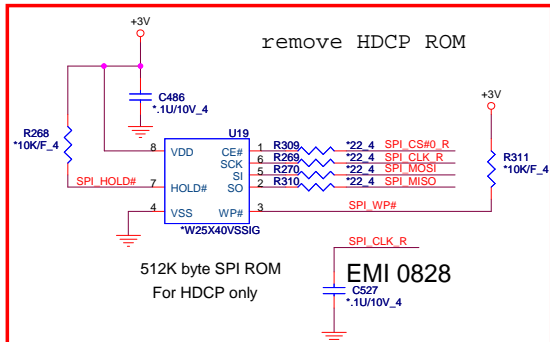
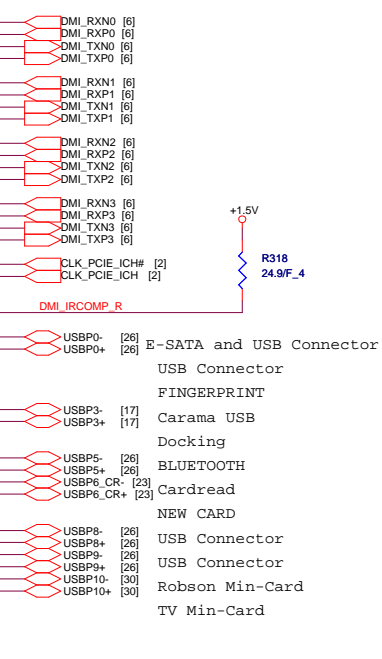
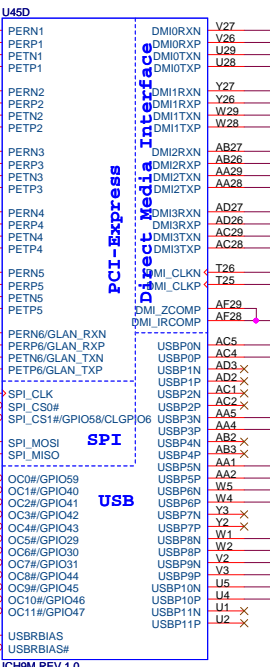
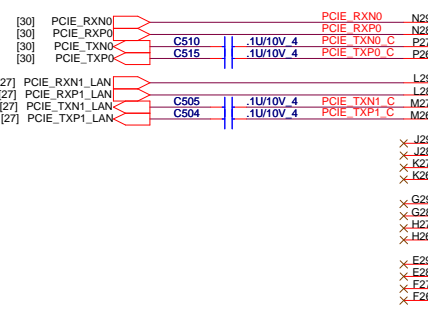
Size Custom Document Number
ICH9-M Host 1/4

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[4,9,19,22,28,30,33,37] +1.5V
[2,4,6,9,10,11,12,14,15,17,18,19,21,22,24,25,26,27,28,29,30,33,34,37] +3V
[21,23,26,30,33,34,35,37] +3VSUS

MINI CARD PCI-E(WLAN)

PCI-E-LAN



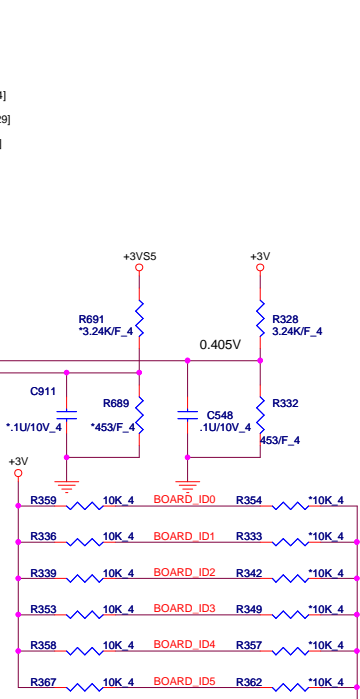
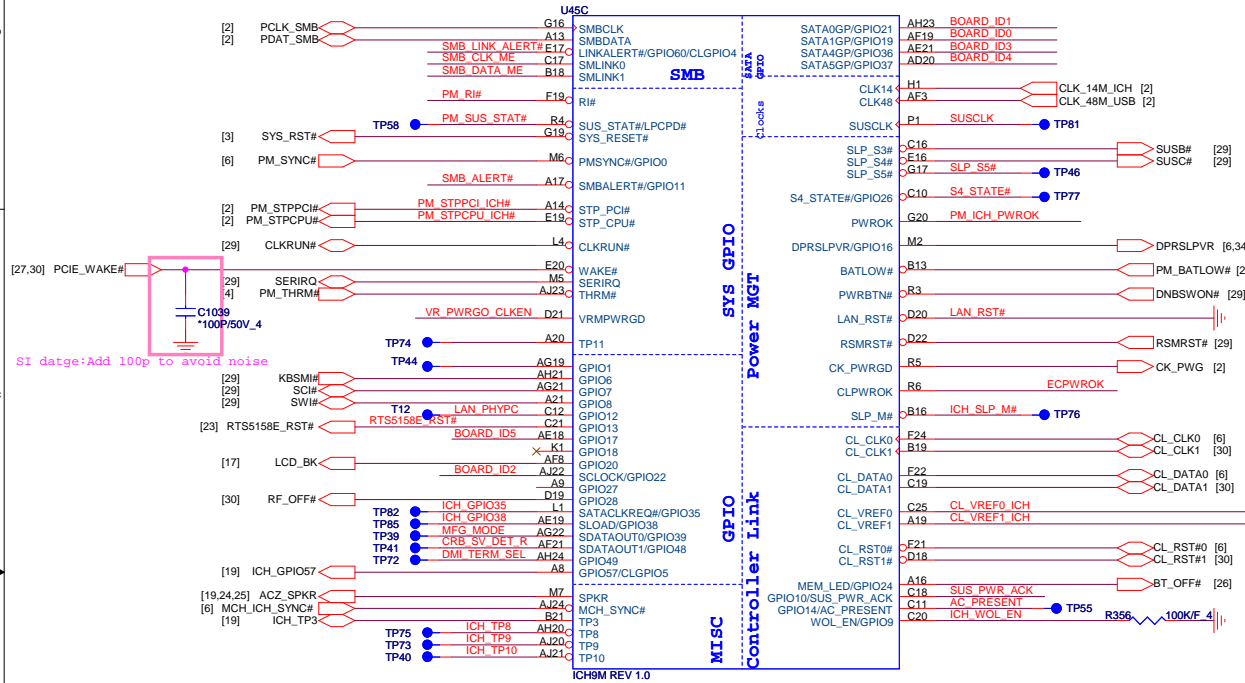
PROJECT : OP6/7
Quanta Computer Inc.

NB5

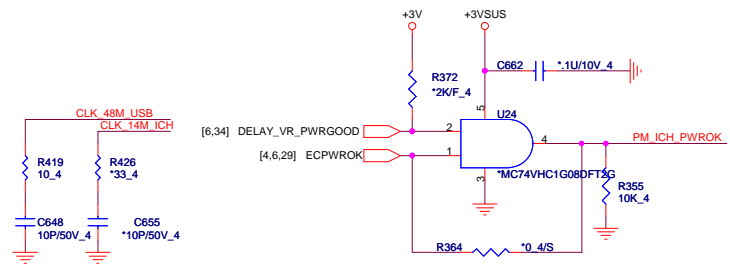
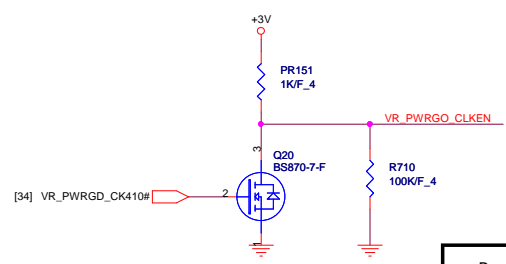
Size Custom Document Number ICH9-M PCI-E 2/4 Rev SI

Date: Tuesday, January 20, 2009 Sheet 20 of 37

[2,4,6,9,10,11,12,14,15,17,18,19,20,22,24,25,26,27,28,29,30,33,34,37] +1.5V
[19,20,22,37] +3V
[23,26,30,33,34,35,37] +3VSUS

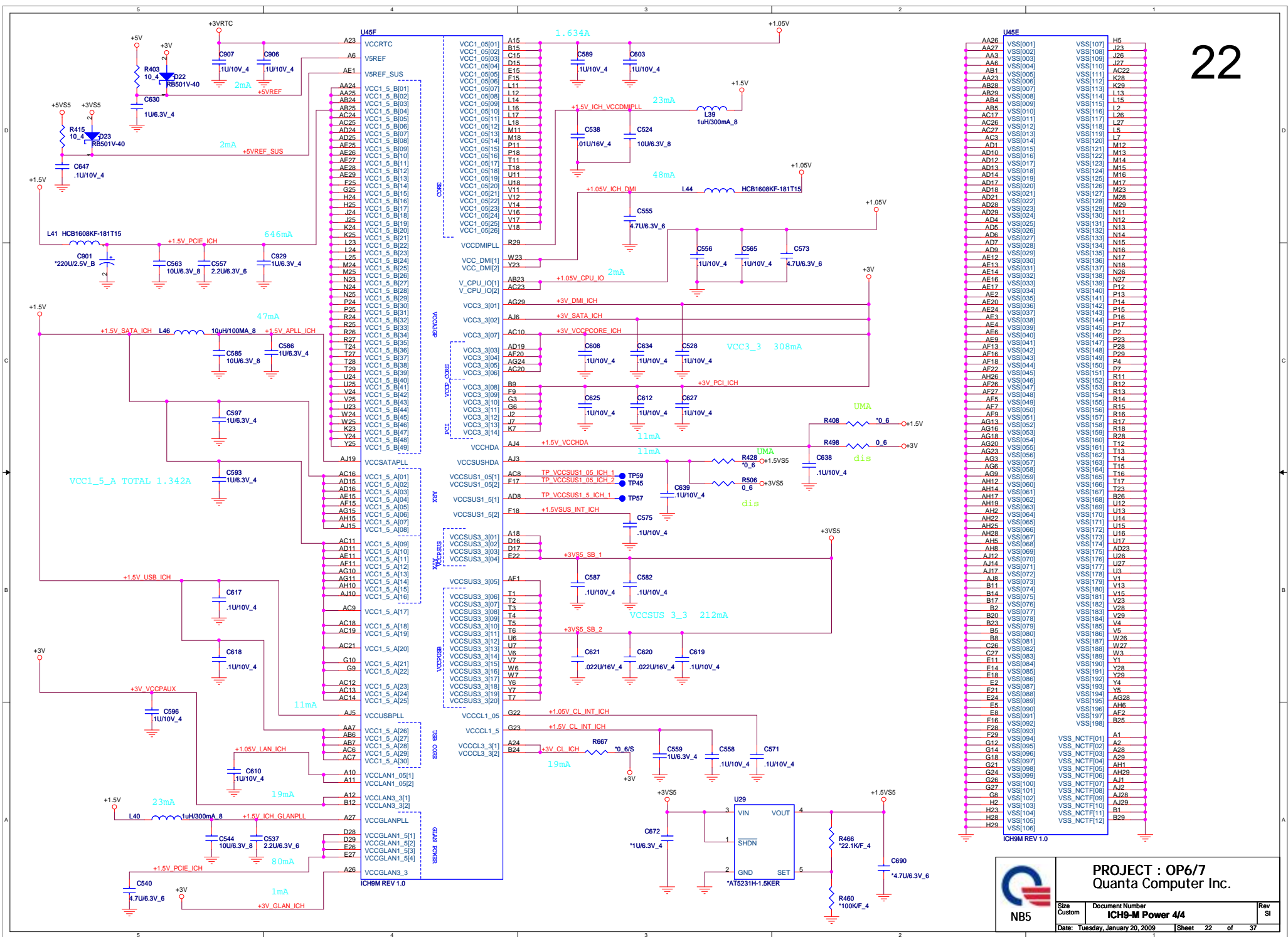


Delete R361,G2 as Bios_Rec can be cover by Bios



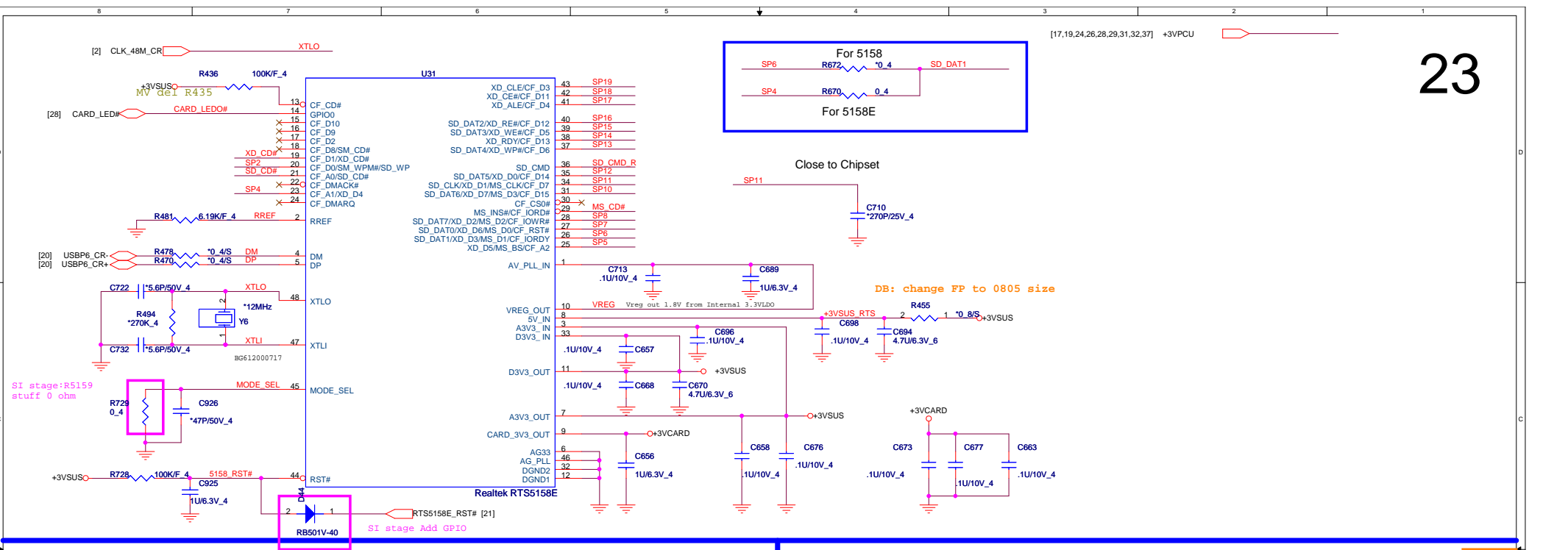
	Board ID	ID0 GPIO19	ID1 GPIO21	ID2 GPIO22	ID3 GPIO36	ID4 GPIO37	ID5 GPIO17
UMA/DIS		0=UMA 1=Dis.					
CardReader			0=No Sup 1=Support				
HDMI				0=No Sup 1=Support			
Bluetooth							
Camera							
Modem							

NB5
 PROJECT : OP6/7
 Quanta Computer Inc.
 Document Number
ICH9-M GPIO 3/4
 Rev SI
 Date: Tuesday, January 20, 2009 | Sheet 21 of 37

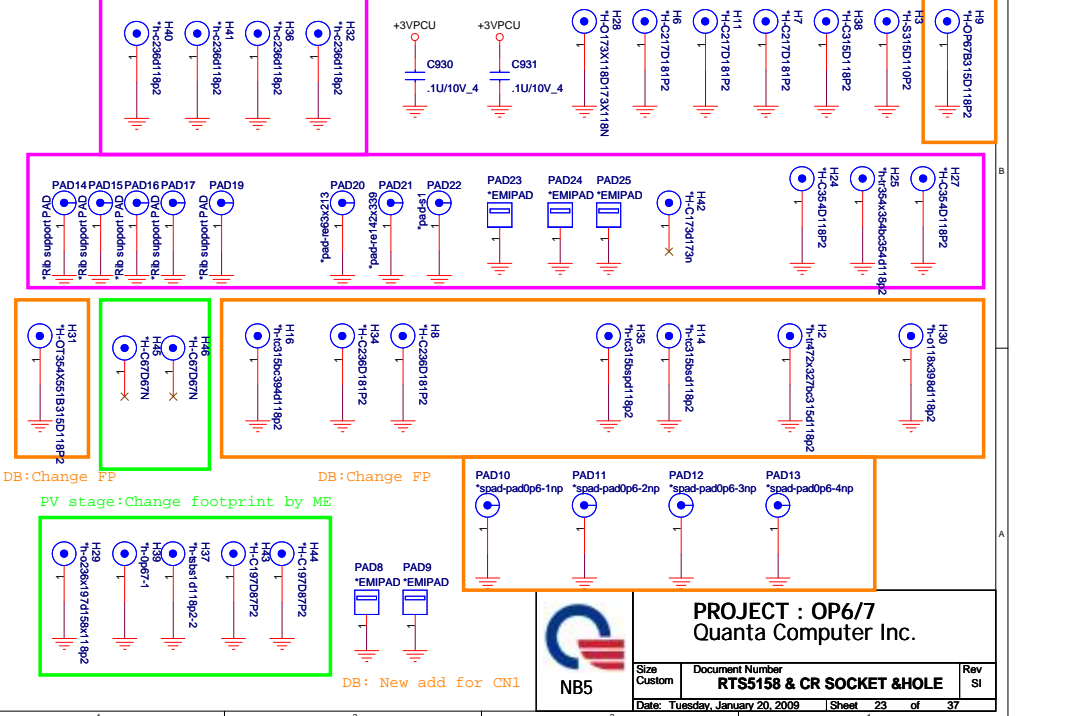
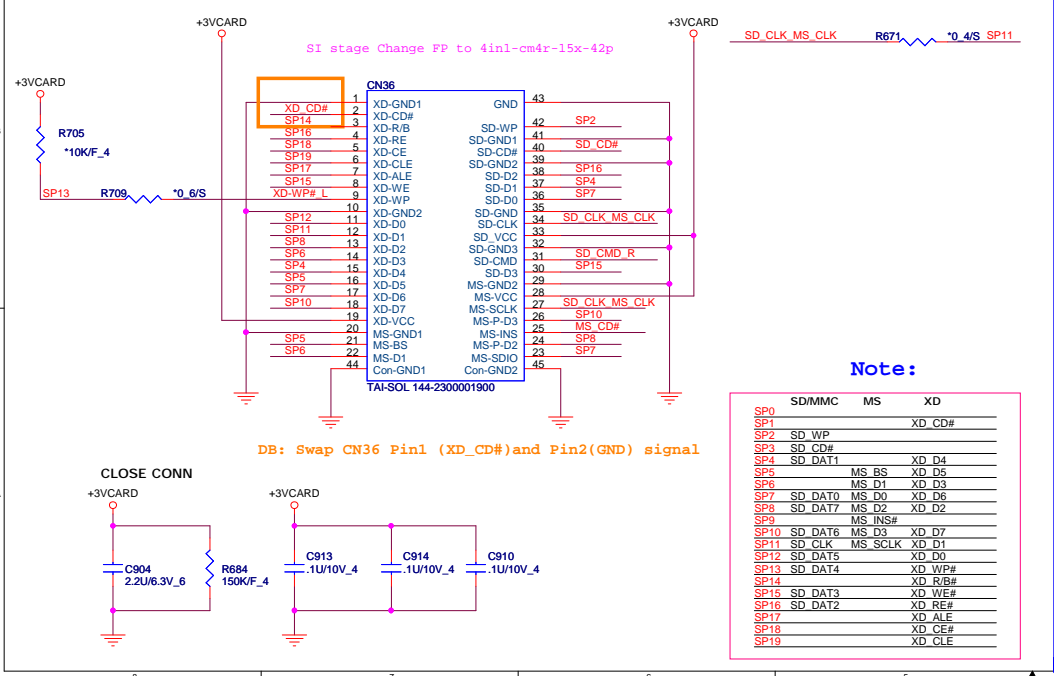


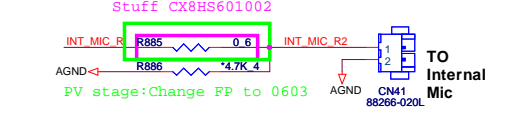
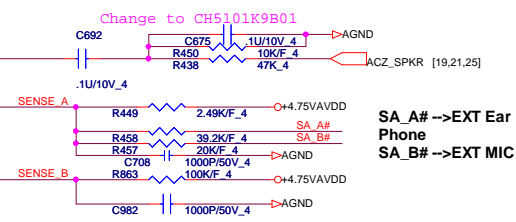
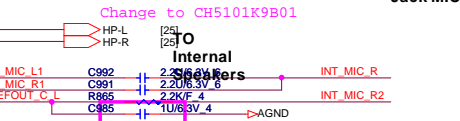
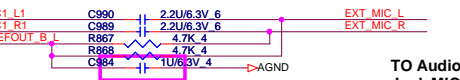
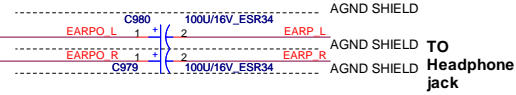
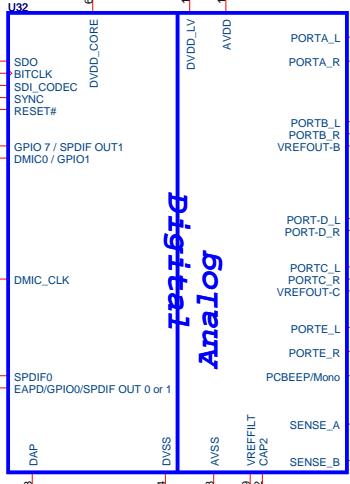
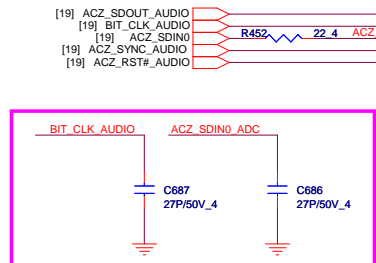
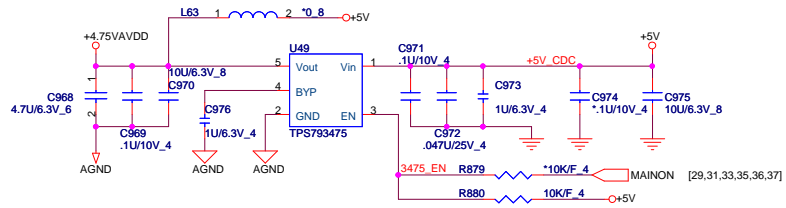
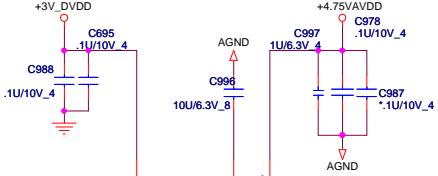
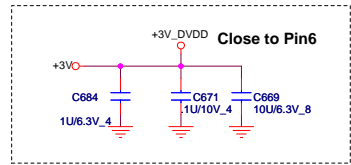
PROJECT : OP6/7
Quanta Computer Inc.

Size Custom	Document Number ICH9-M Power 4/4	Rev SI
Date: Tuesday, January 20, 2009 Sheet 22 of 37		

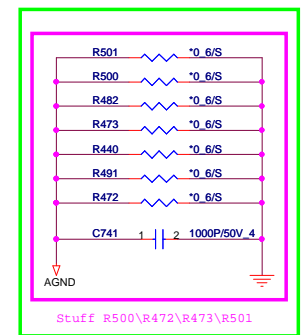


4 IN1 CARD READER XD, /SD, MS/MSP

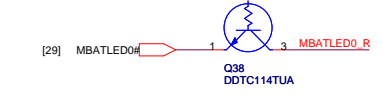
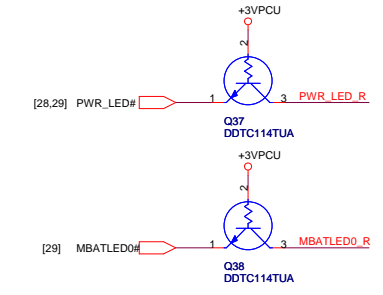
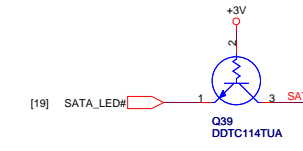
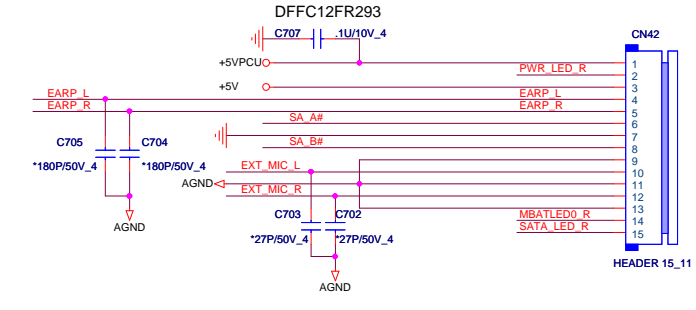




PV Stage: Change to short pad



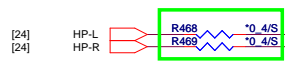
AUDIO/B CON.



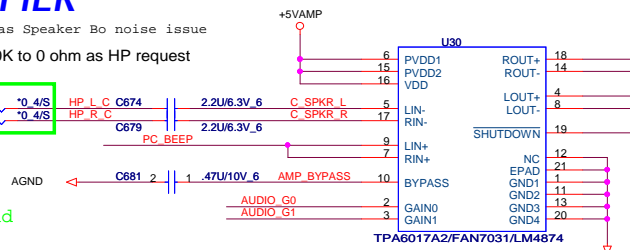
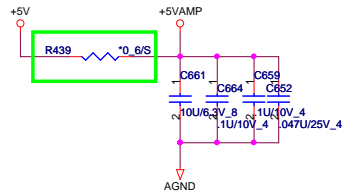
AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue

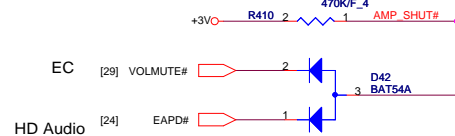
Change R468,R469 from 20K to 0 ohm as HP request



EV Stage: Change to short pad



Change R410 from 100K to 470K(CS44702FB13)



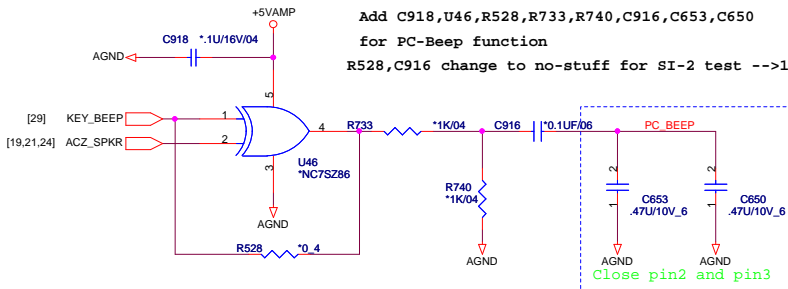
- AL001431K04
- AL6017A2K12
- APA2031 ,AL002031K00

6017A2 Gain Table

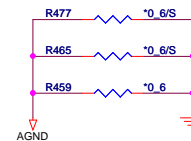
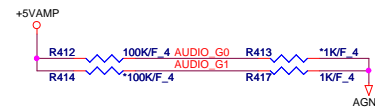
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

Add C918,U46,R528,R733,R740,C916,C653,C650 for PC-BEEP function

R528,C916 change to no-stuff for SI-2 test -->12/6



close pin2 and pin3



$$V_{rms} = V_{pp} / 2 \sqrt{2}$$

$$Power = (V_{rms})^2 / R$$

QT6 speaker -- 3.2ohm / 2W

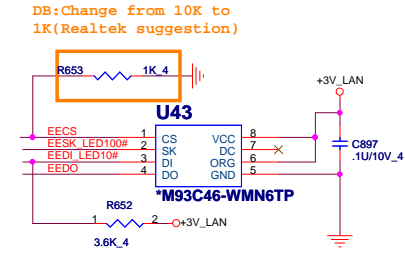
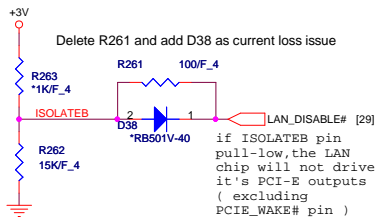
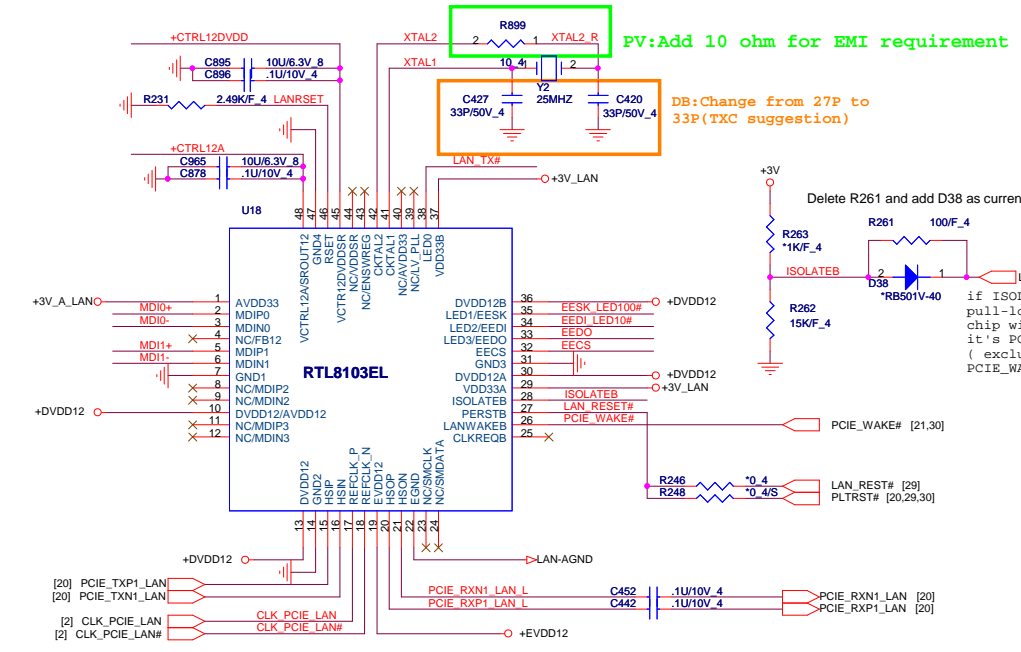
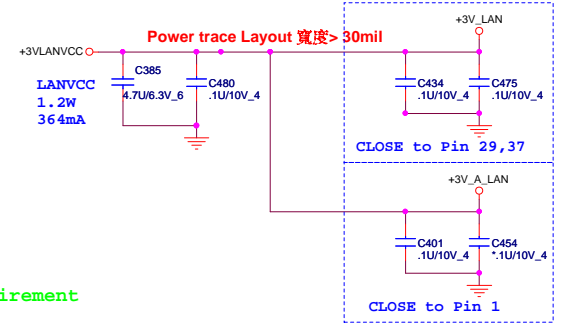
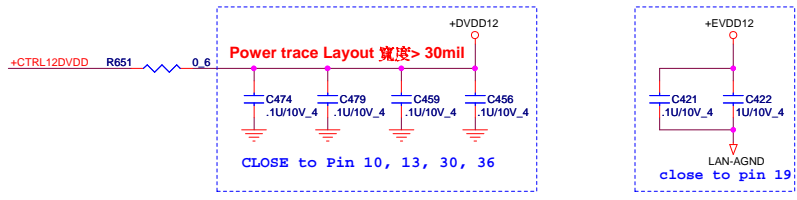
INT. SPEAKER

Change P/N to CX8HS601002 for EMI

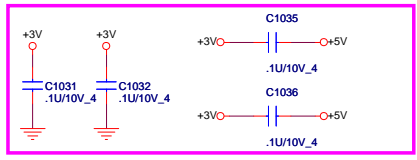
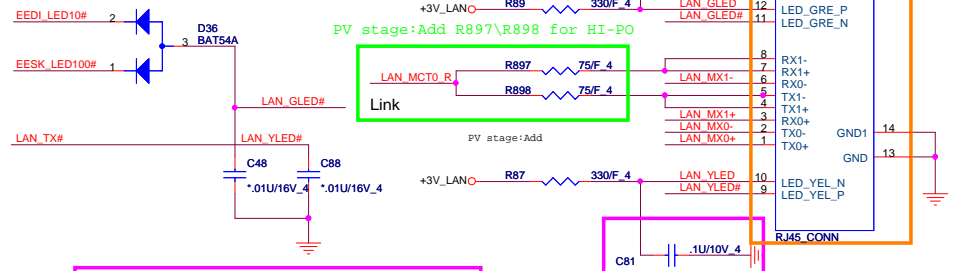
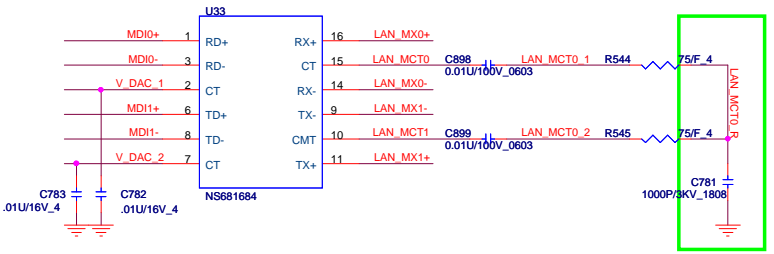


PROJECT : OP6/7
Quanta Computer Inc.

Size Custom	Document Number	Rev SI
	AMP_TPA6047A4/Accelerometer	
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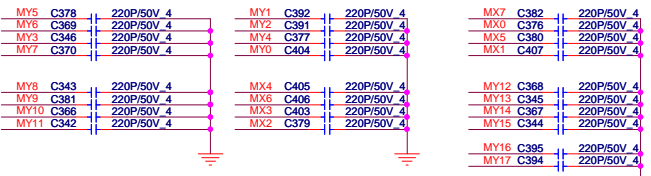
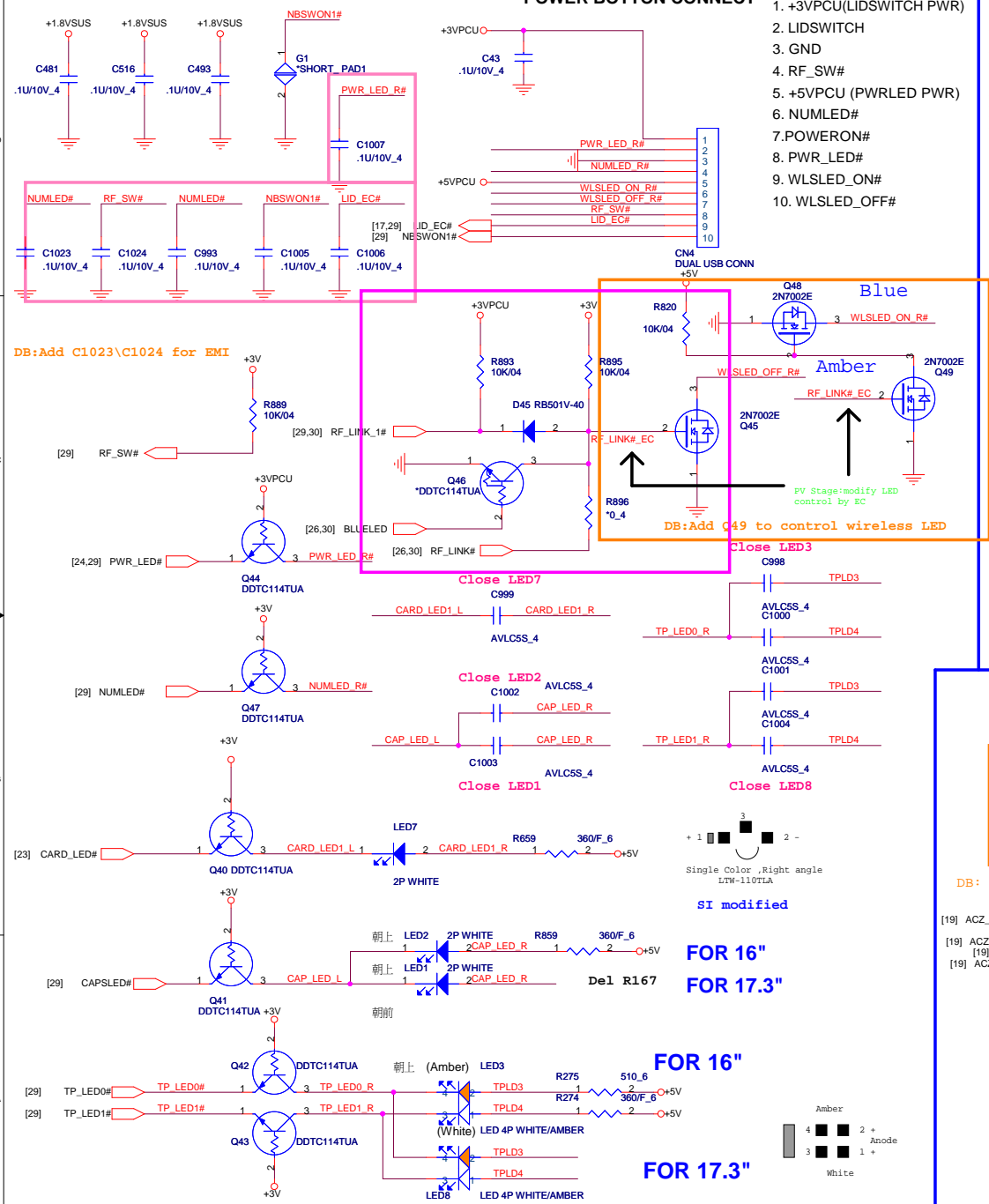


LAN_Transformer

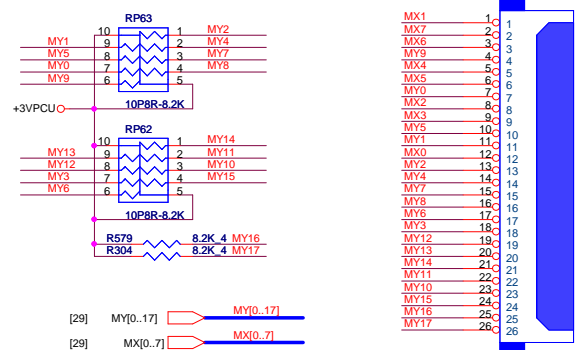


POWER BOTTON CONNECT

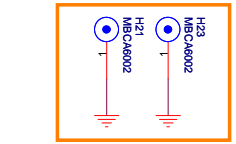
- 1.+3VPCU(LIDSWITCH PWR)
2. LIDSWITCH
3. GND
4. RF_SW#
- 5.+5VPCU (PWRLD PWR)
6. NUMLED#
- 7.POWERON#
8. PWR_LED#
9. WLSLED_ON#
10. WLSLED_OFF#



KEYBOARD PULL-UP

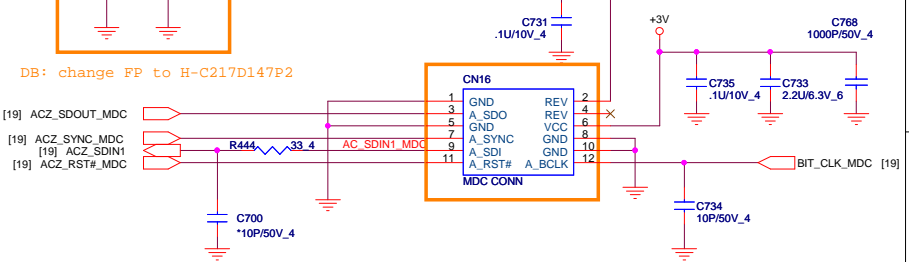


GB1RF260-1253-8F
Footprint: "gblrf260-1253-7f-26p-1"



DB: change FP to H-C217D147P2

MDC

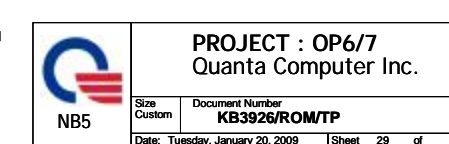
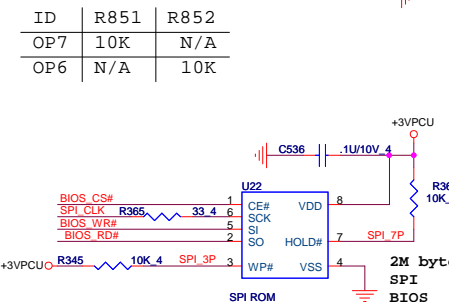
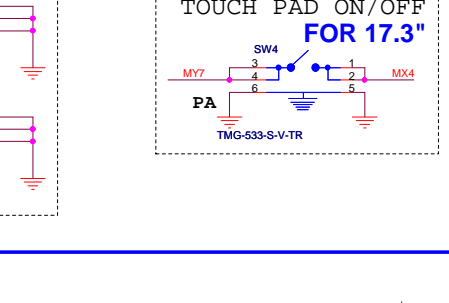
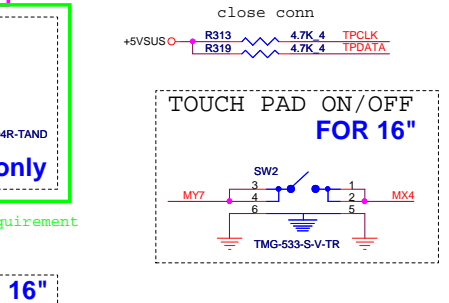
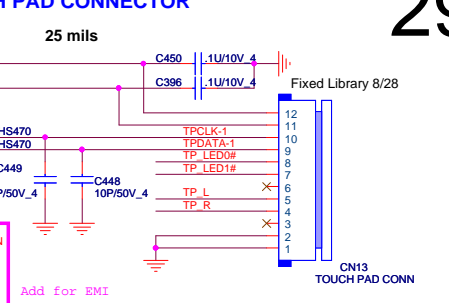
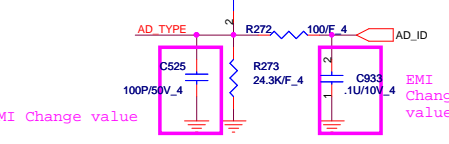
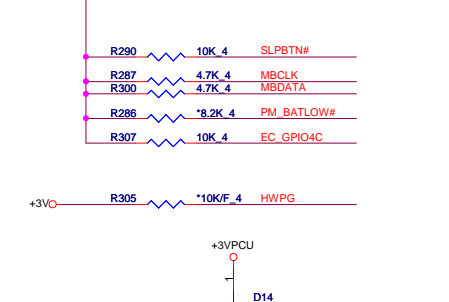
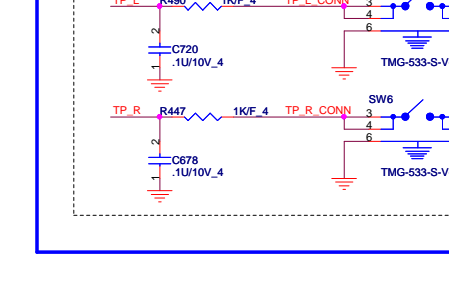
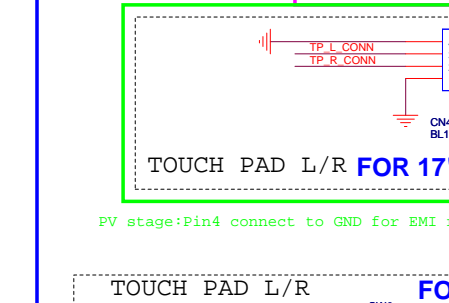
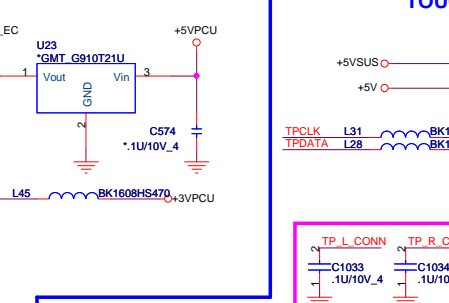
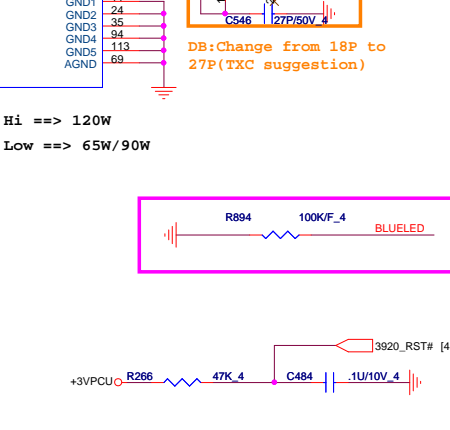
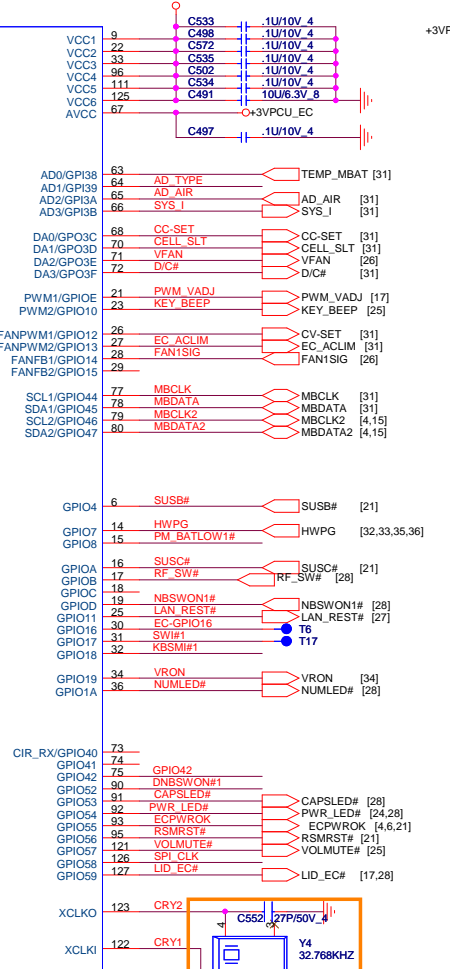
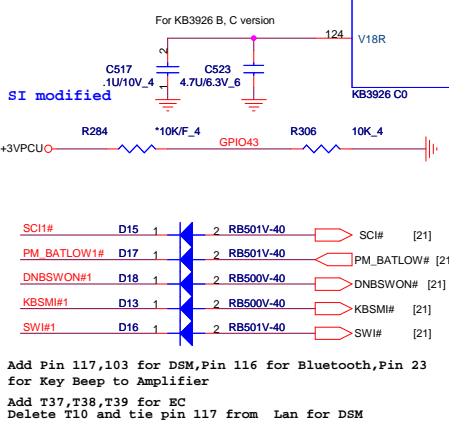
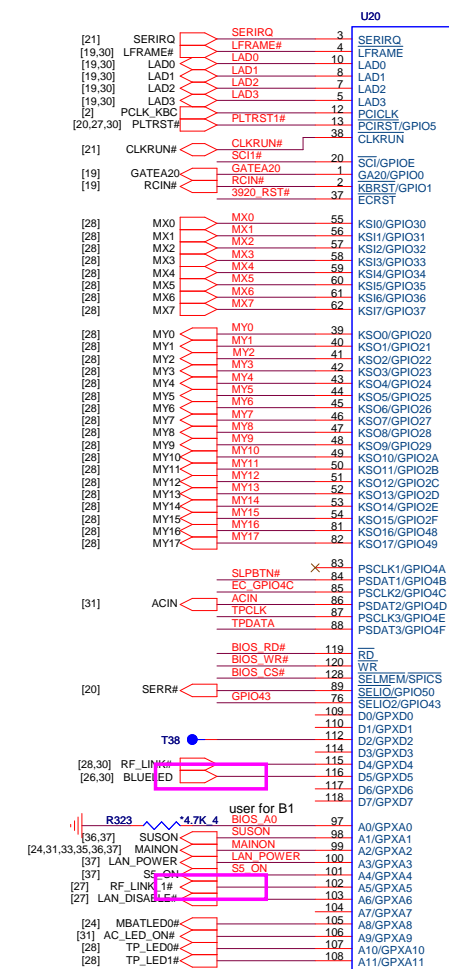
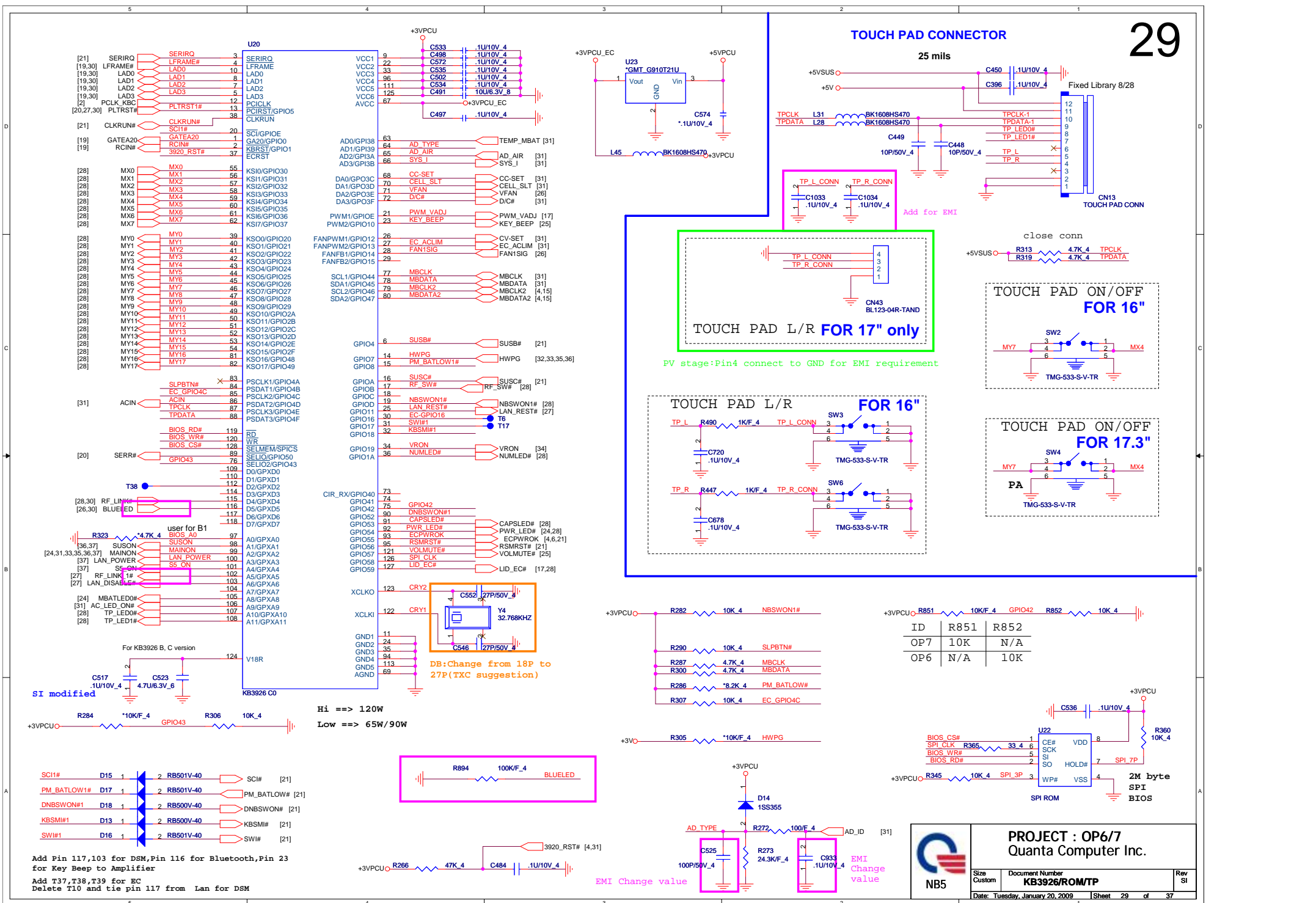


DB: change FP to MDC-1-179373-2-12P-RUV

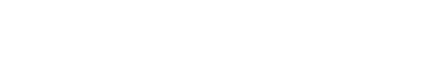
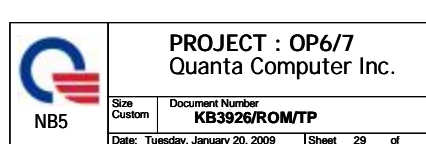
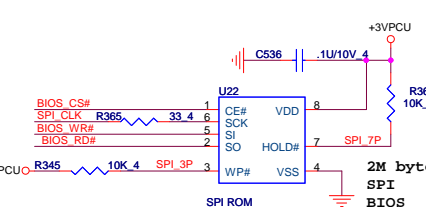


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ID	R851	R852
OP7	10K	N/A
OP6	N/A	10K



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Add Pin 117,103 for DSM,Pin 116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM

Hi ==> 120W
Low ==> 65W/90W

EMI Change value

EMI Change value

DB:Change from 18P to 27P(TXC suggestion)

user for B1

SI modified

For KB3926 B, C version

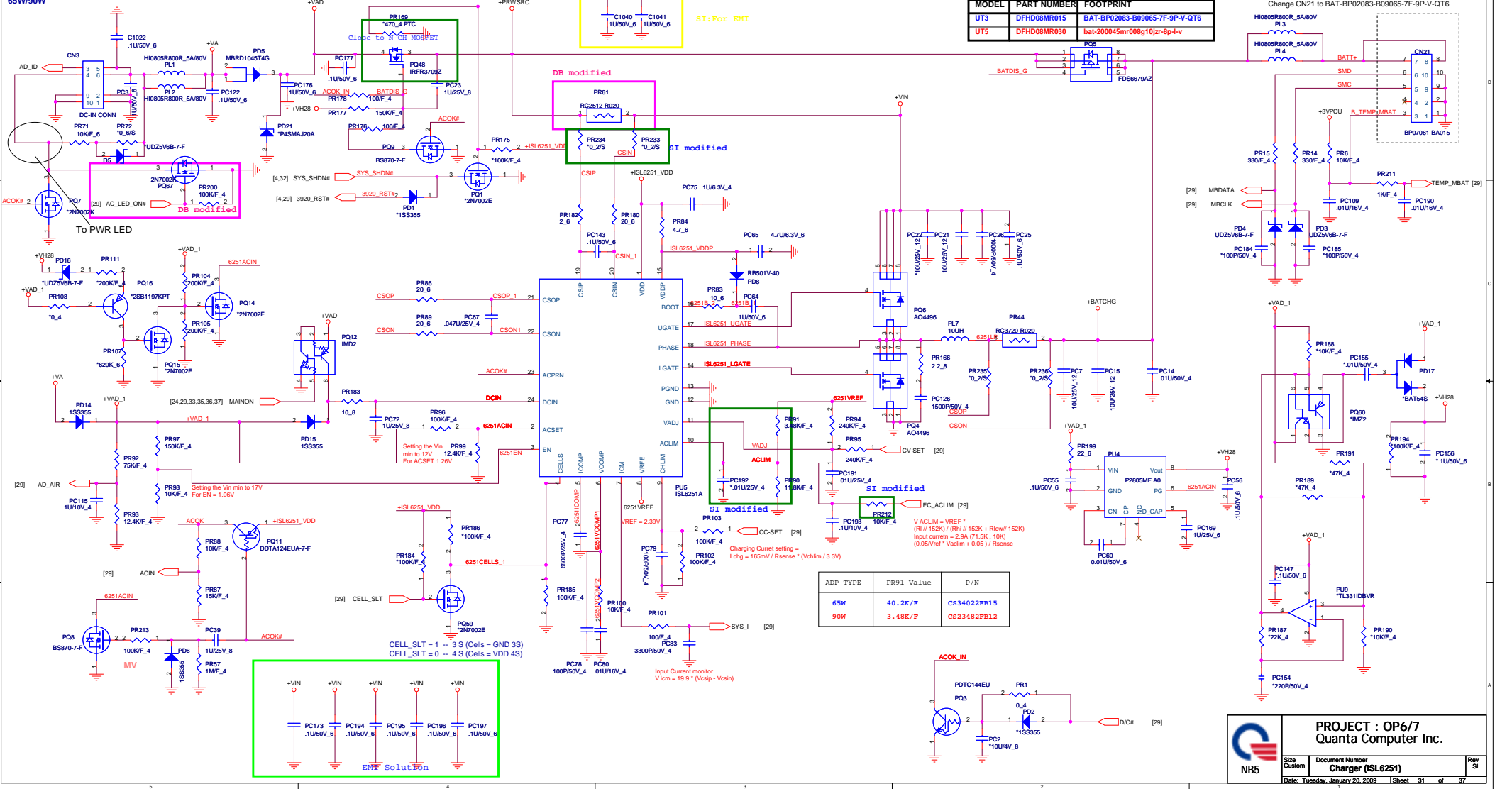
close conn

Fixed Library 8/28

PNB5

TOP DC JACK
65W/90W

BATTERY CONNECTOR TYP		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr068g10jr-8p-1-v



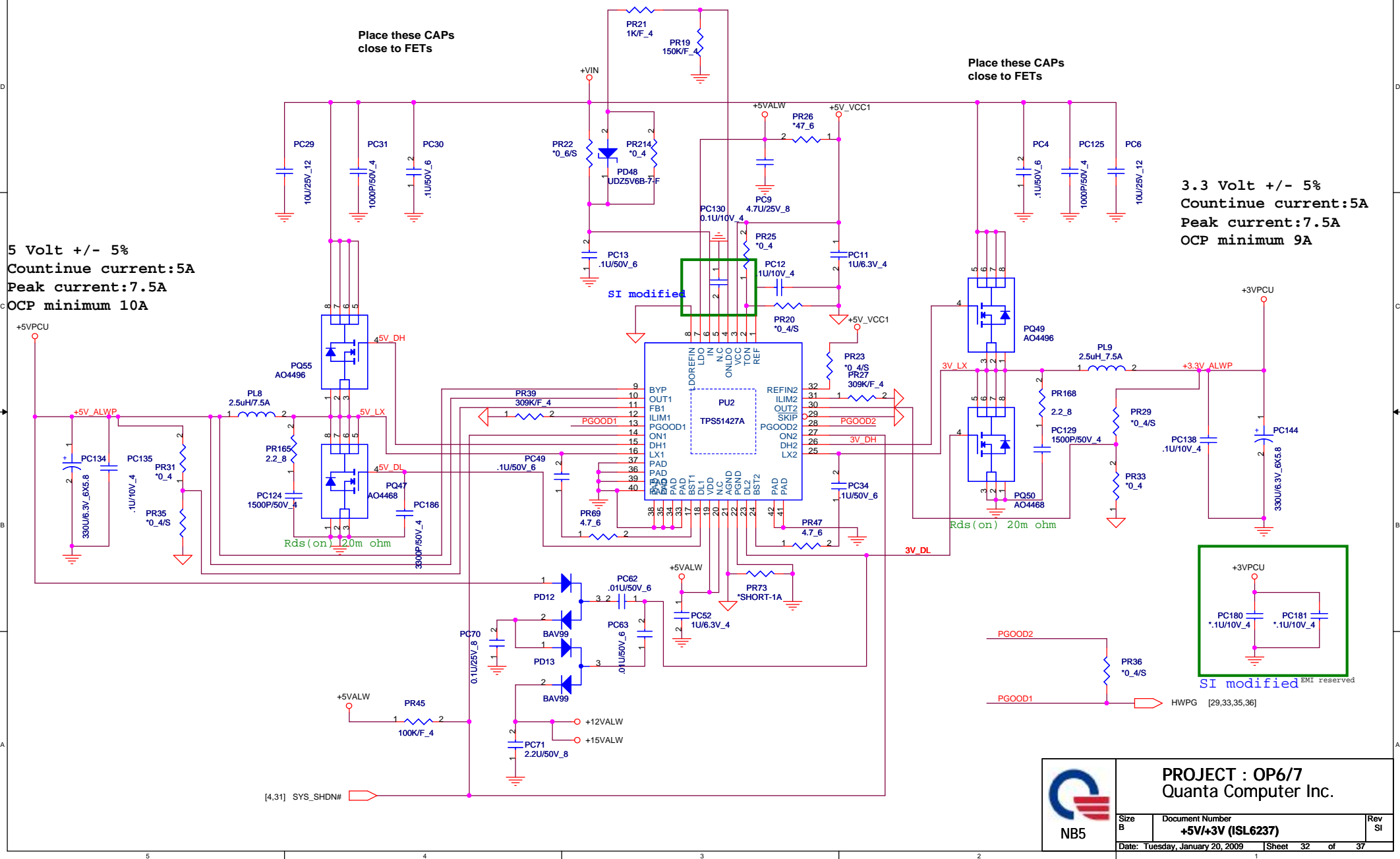
ADP TYPE	PR91 Value	P/N
65W	40.2K/F	CS34022PB15
90W	3.48K/F	CS23482PB12

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Charger (ISL6251) Rev SI

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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

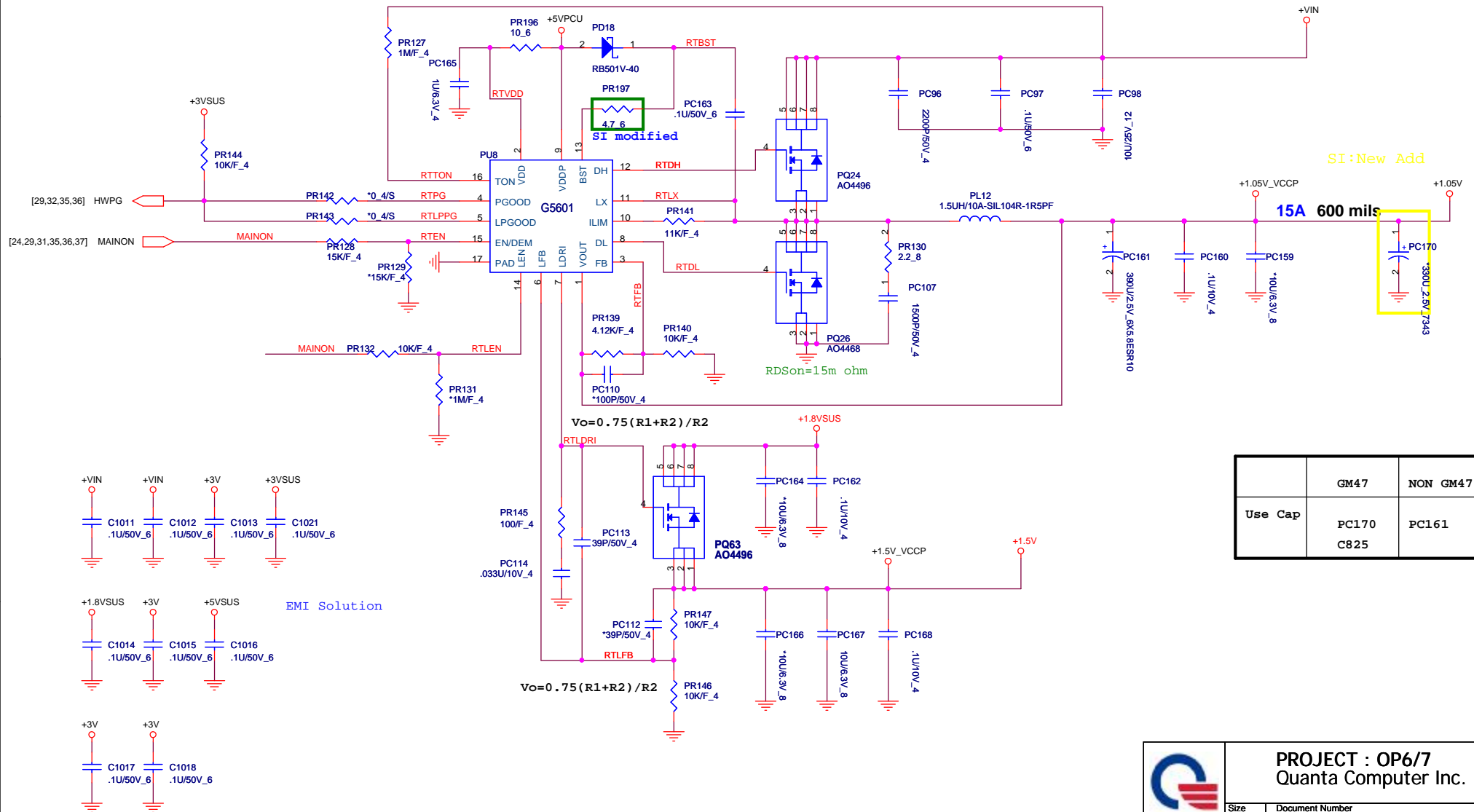


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VCCP1.05V & +1.5V

+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A



SI:New Add

15A 600 mils

$$V_o = 0.75 (R1 + R2) / R2$$

$$V_o = 0.75 (R1 + R2) / R2$$

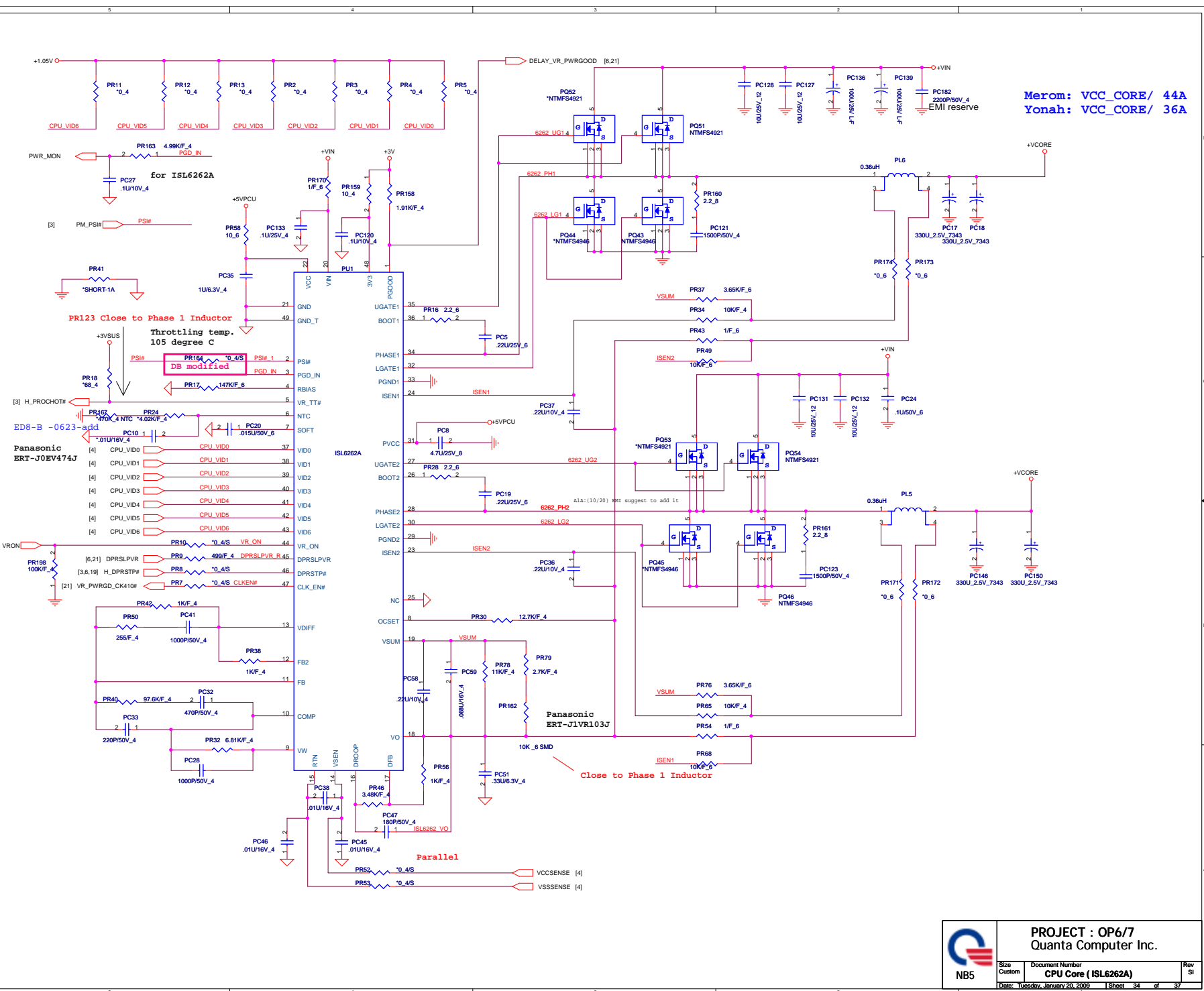
	GM47	NON GM47
Use Cap	PC170 C825	PC161

EMI Solution



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Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A

for ISL6262A
PSI#

Throttling temp.
105 degree C

Panasonic
ERT-J0EV474J

VRON#

PR198
100K_F_4

PR40
97.6K_F_4

PC33
220P/50V_4

PC46
.01U/16V_4

PC45
.01U/16V_4

PR52
.0_4S

PR53
.0_4S

PC47
180P/50V_4

ISL6262 VO

Parallel

VCCSENSE [4]

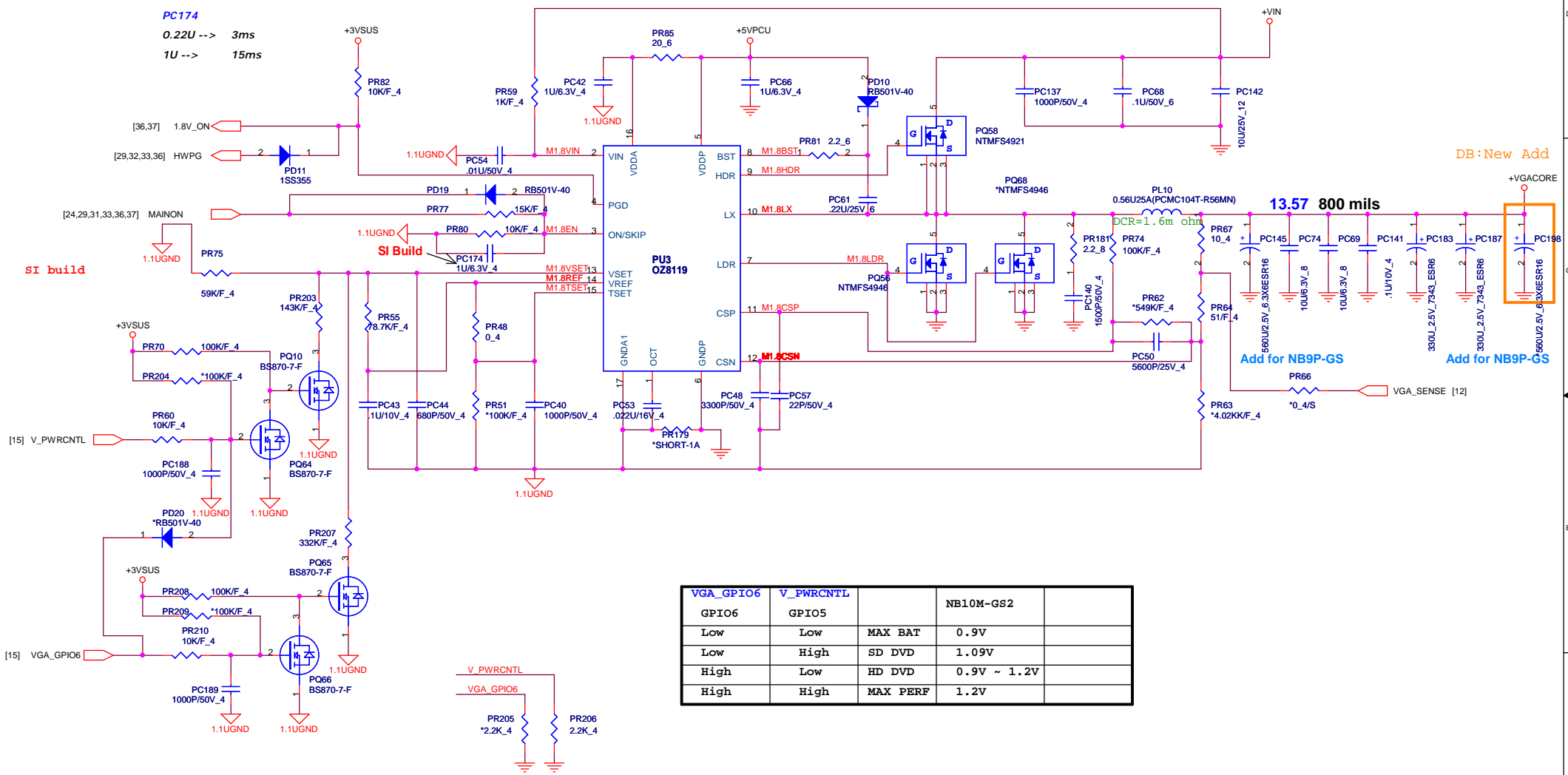
VSSSENSE [4]

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	Size Custom	Document Number CPU Core (ISL6262A)	Rev SI
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VGA Core & VCC1.1

+1.1Volt +/- 5%
 Countinue current:17.54A
 Peak current:22.8A
 OCP minimum 23A

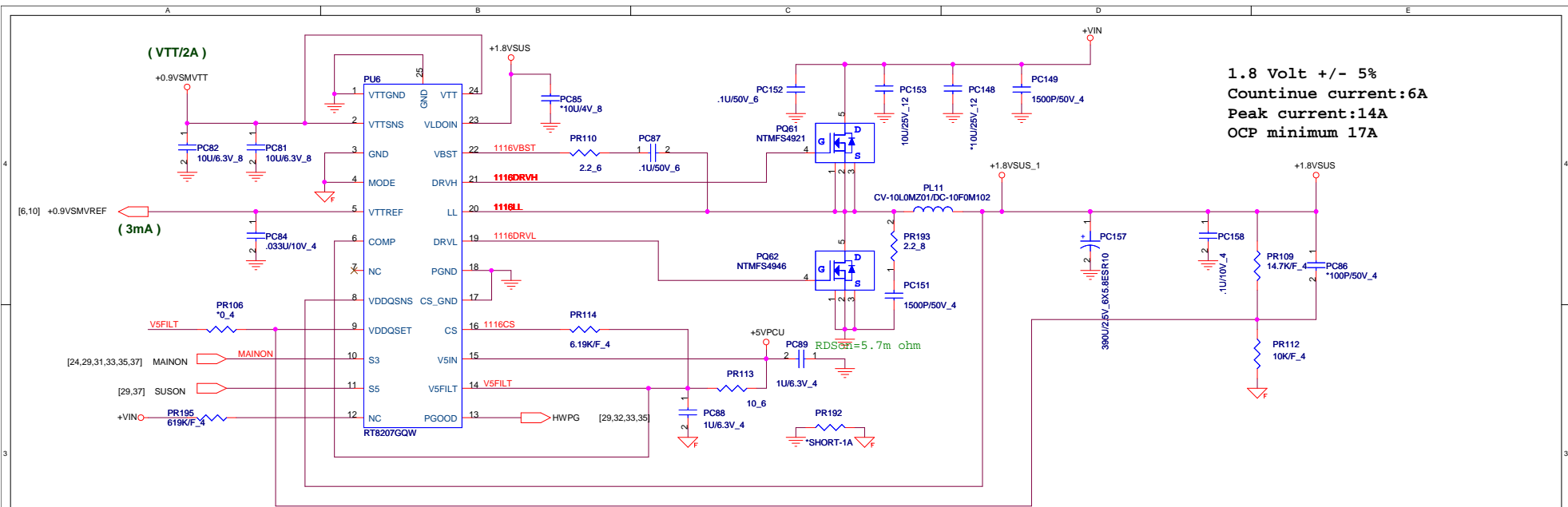
PC174
 0.22U --> 3ms
 1U --> 15ms



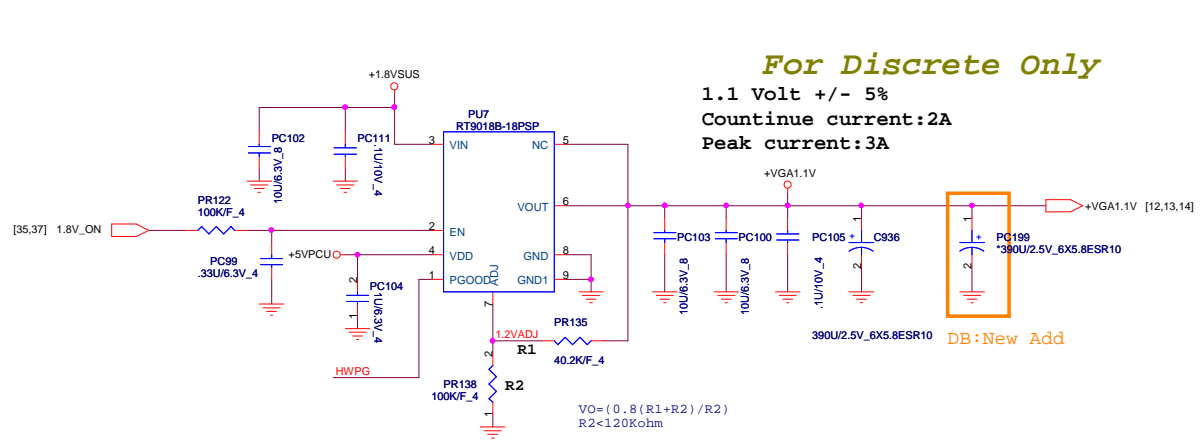
VGA_GPIO6	V_PWRCNTL		NB10M-GS2	
Low	Low	MAX BAT	0.9V	
Low	High	SD DVD	1.09V	
High	Low	HD DVD	0.9V ~ 1.2V	
High	High	MAX PERF	1.2V	

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 Quanta Computer Inc.

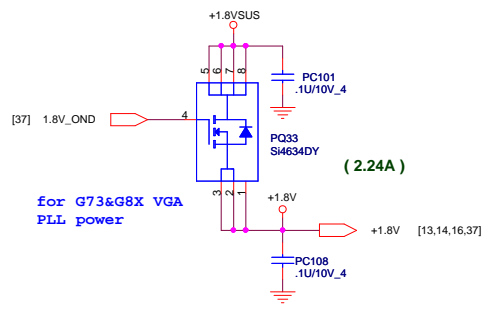
Size Custom	Document Number VGA Core OZ8119	Rev SI
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Change PR122 tied to 1.8V_ON as power sequence request



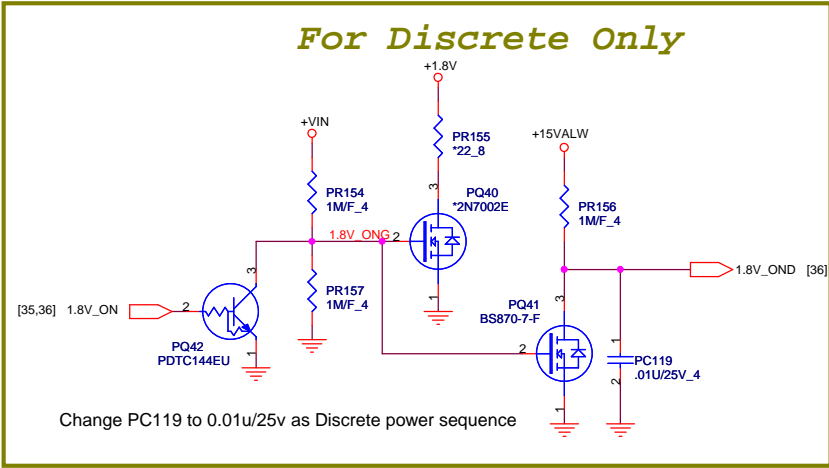
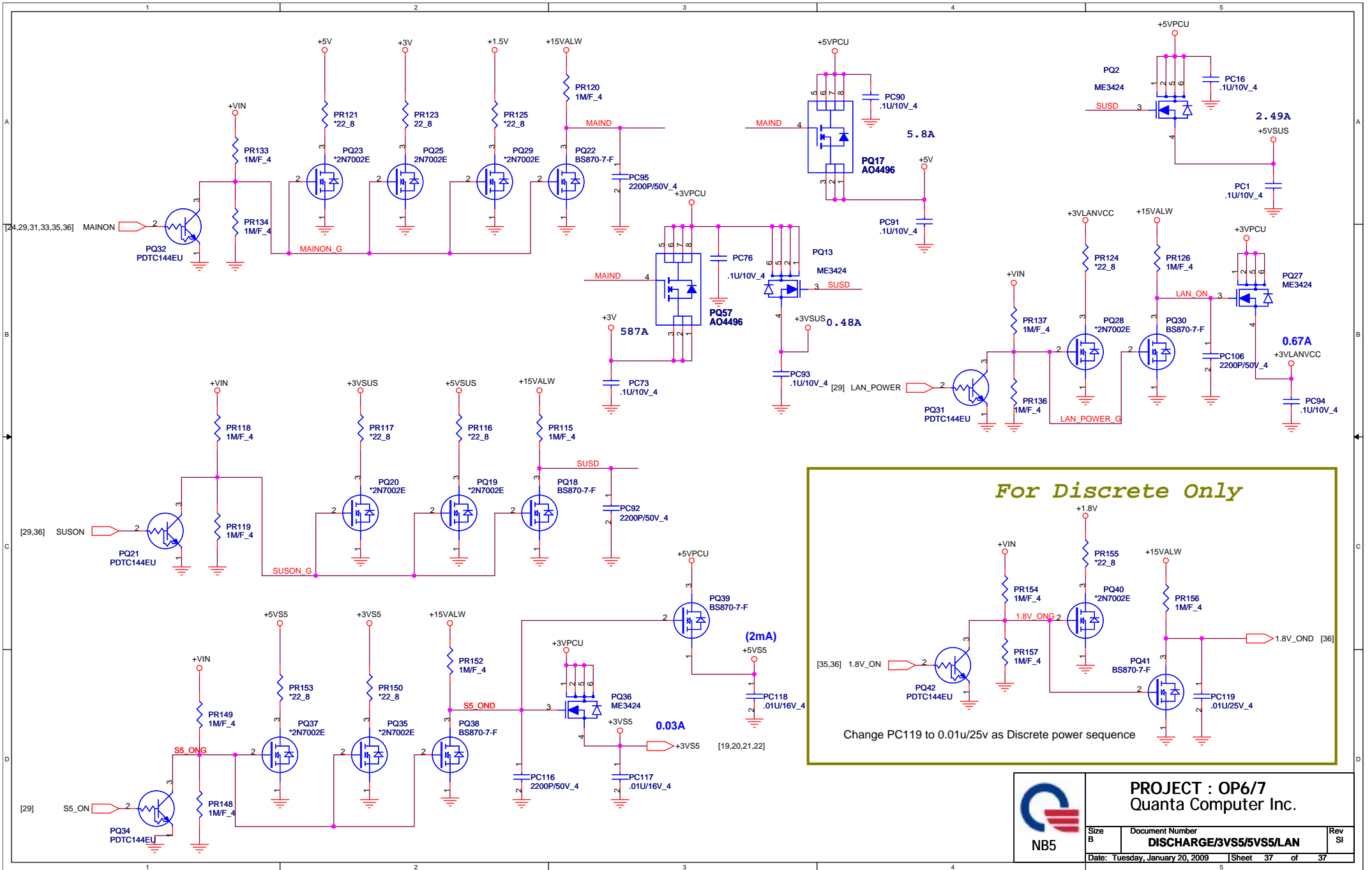
For Discrete Only
 1.1 Volt +/- 5%
 Continune current: 2A
 Peak current: 3A



for G73&G8X VGA
 PLL power



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