

Table of Contents

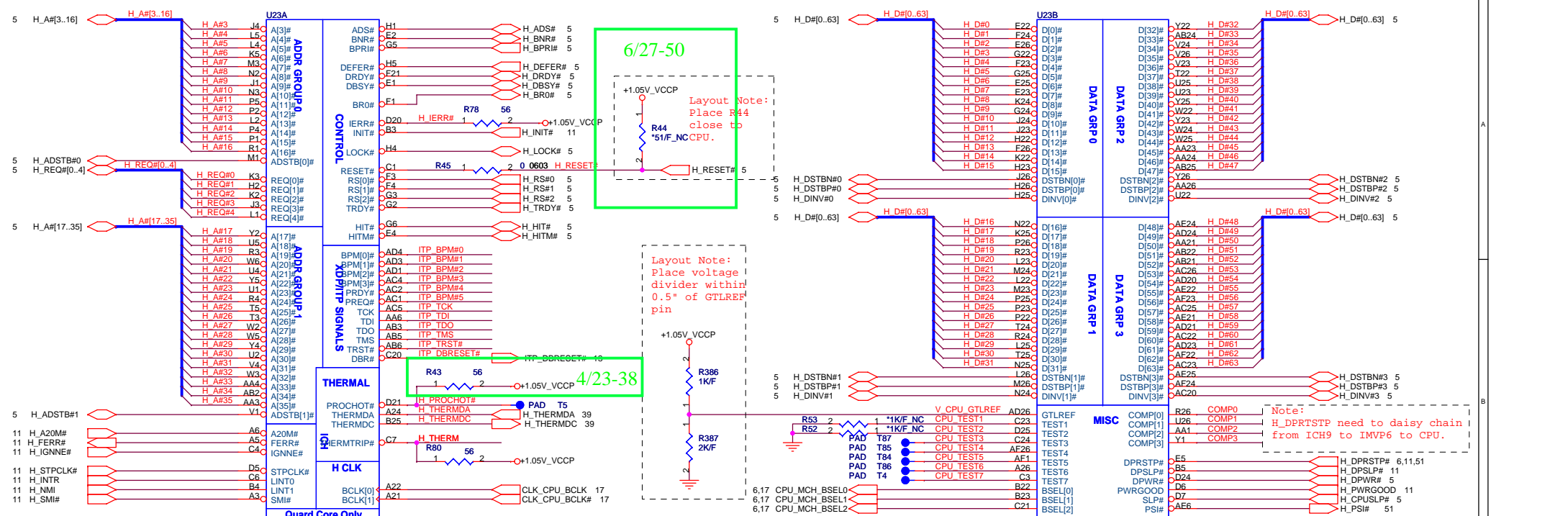
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH8M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	HDMI
23	LCD Conn. & SSP
24	CRT Conn
25	SATA Conn
26-27	CARD READER/Conn & 1394
28	Express Card & Smart Card
29-30	Mini Card
31	SIO (ITE8512)
32	FLASH/RTC
33	USB
35	TP / KEYBOARD
36	SWITCH /LED
37	FAN & Thermal
38-39	Audio CODEC(ALC888)/Phone Jack
40-41	LOM / Switch
44	System Reset Circuit
46	Battery Selector & Charger
48	1.05VCCP / 1.5V RUJN
49	DDR2_1.8VSUS, 0.9V
51	CPU_ISL6266(2phase)
52	MAX8744 (+5.5V,+3.3V)
53	RUN Power Switch
54	DCIN,Batt
55	PAD& SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Dianram

Power States

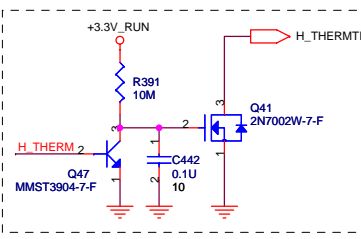
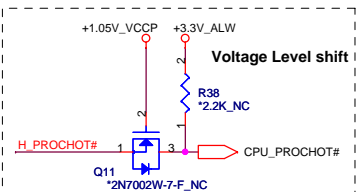
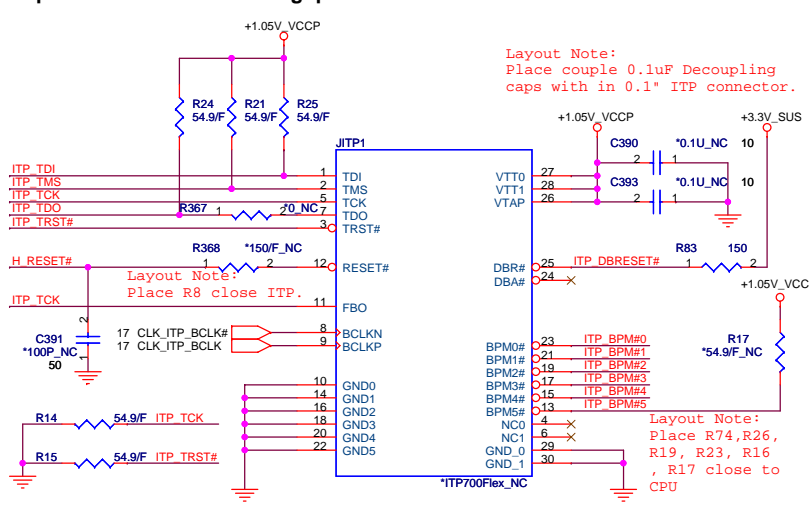
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0-S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0-S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54,56	LCD/CHARGE POWER	ALWON	S0-S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0-S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	18,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

GND PLANE	PAGE	DESCRIPTION
⏚ 8731AGND	46	
⏚ AGND_0.9V	49	
⏚ AGND_DC/DC	52	
⏚ AGND_DC2	48	
⏚ AGND_DDR	49	
⏚ AGND_ISL6260	51	
⏚ GND	ALL	





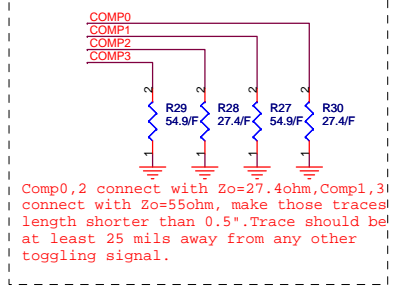
Populate ITP700Flex for bringup 2/18-5



ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

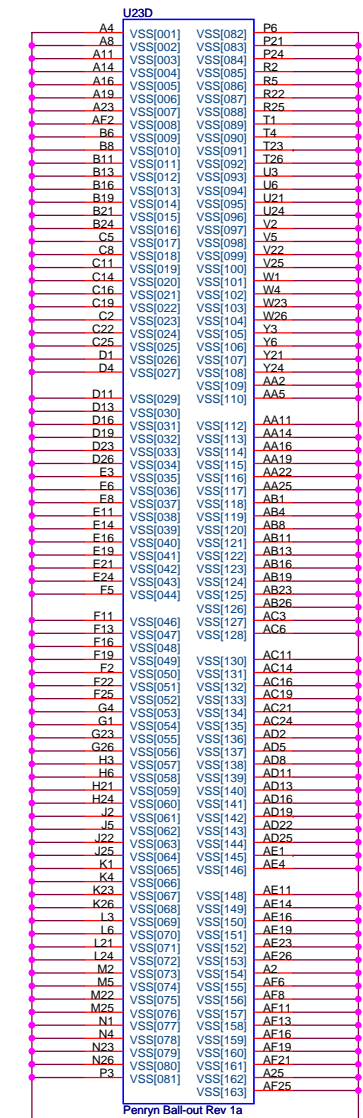
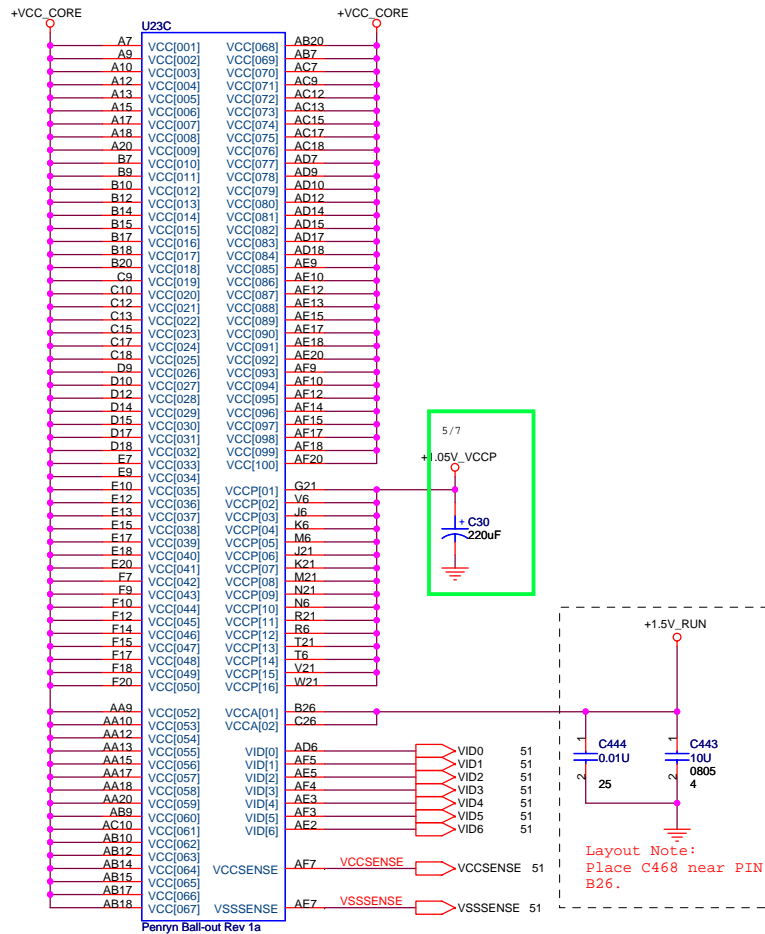
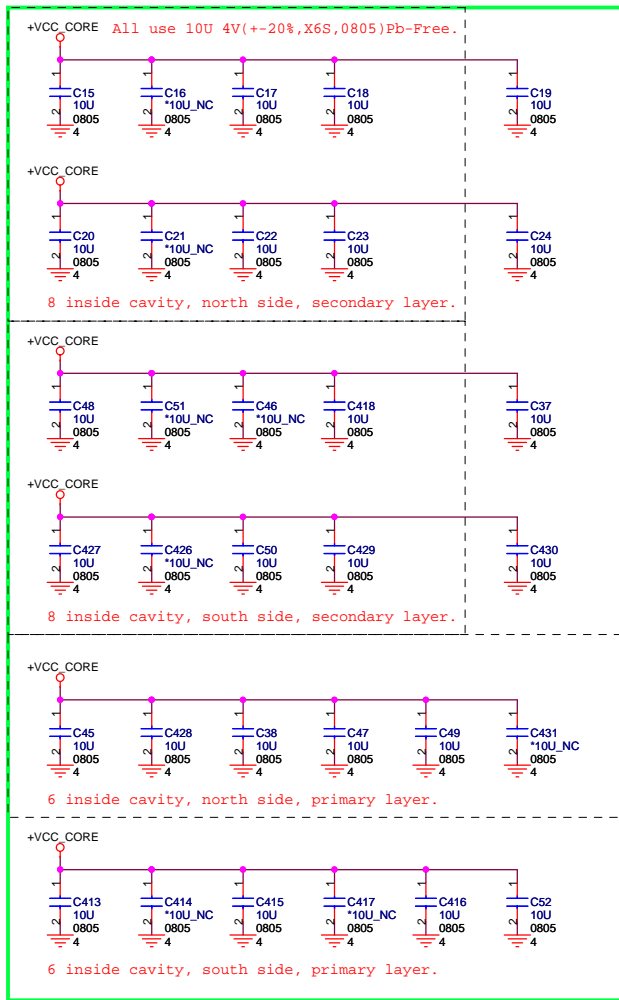
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

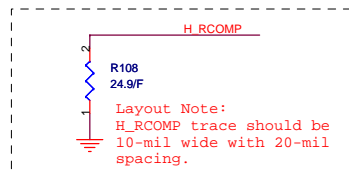
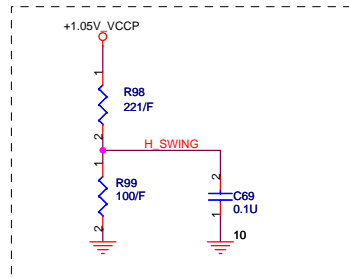
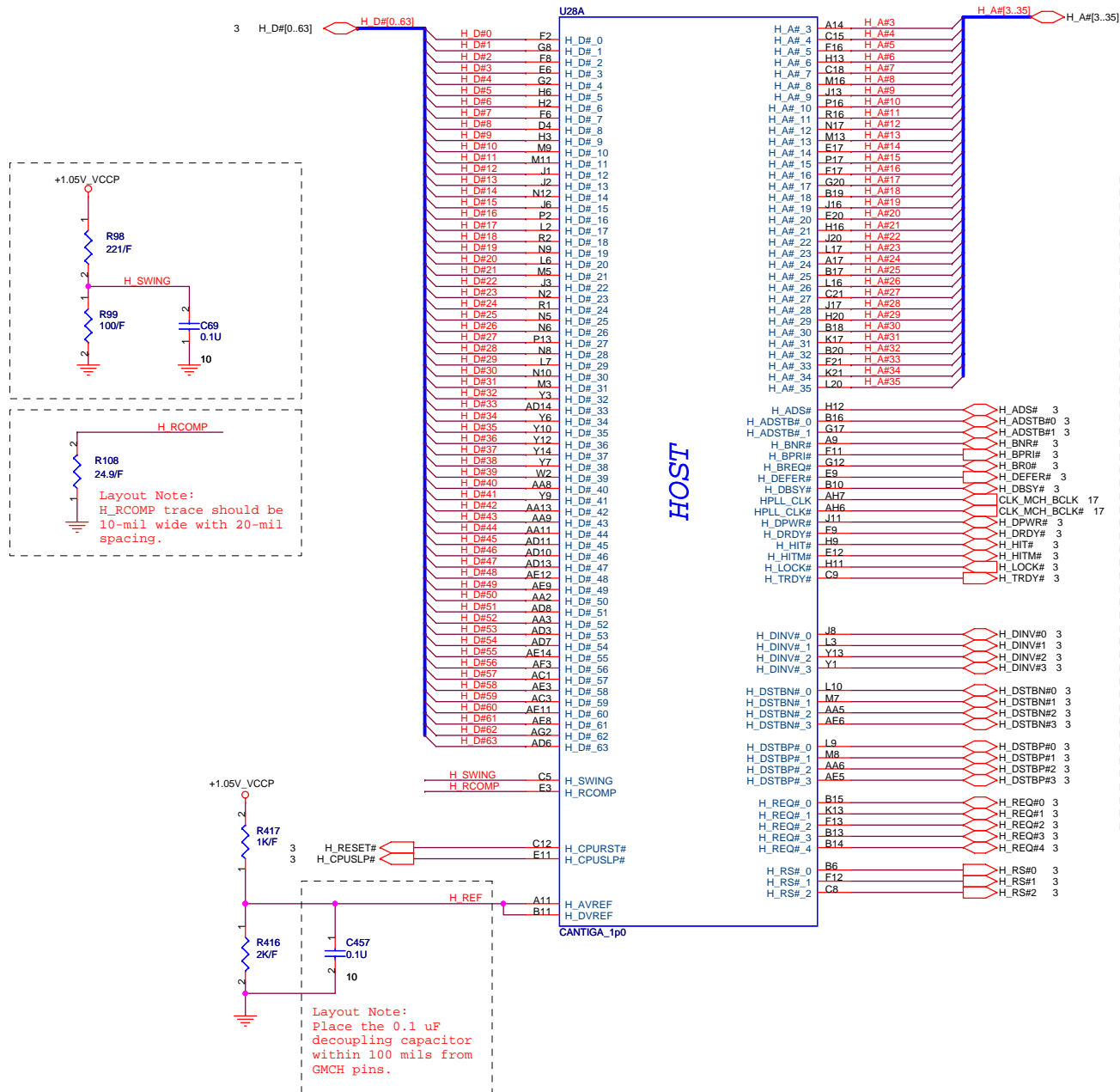


Merom Processor (HOST BUS)

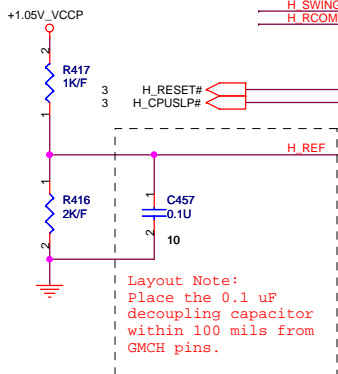
Size	Document Number FM7B	Rev	1A
------	----------------------	-----	----

Date: Wednesday, July 16, 2008 Sheet 3 of 60

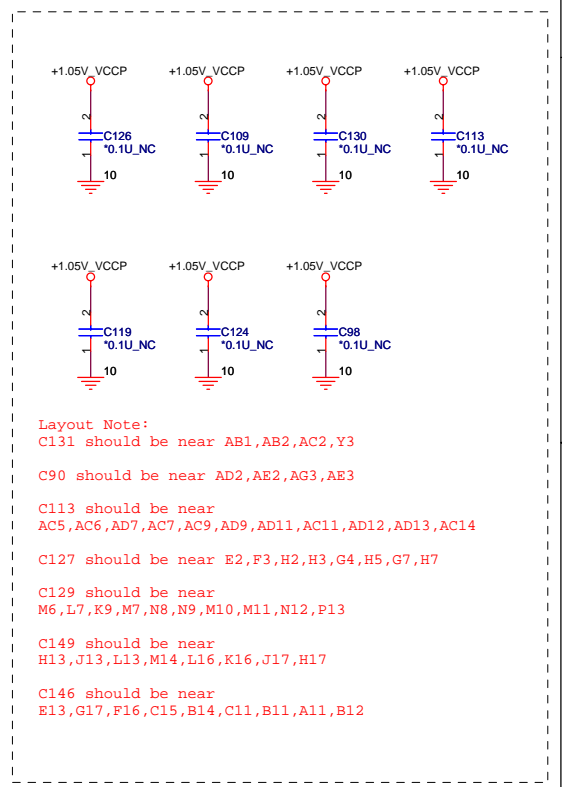




Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.



Layout Note:
C131 should be near AB1,AB2,AC2,Y3
C90 should be near AD2,AE2,AG3,AE3
C113 should be near
AC5,AC6,AD7,AC7,AC9,AD9,AD11,AC11,AD12,AD13,AC14
C127 should be near
E2,F3,H2,H3,G4,H5,G7,H7
C129 should be near
M6,L7,K9,M7,N8,N9,M10,M11,N12,P13
C149 should be near
H13,J13,L13,M14,L16,K16,J17,H17
C146 should be near
E13,G17,F16,C15,B14,C11,B11,A11,B12



15 DDR_A_D[0..63]

U28D

DDR A D0	AJ38	SA_DQ_0
DDR A D1	AJ41	SA_DQ_1
DDR A D2	AN38	SA_DQ_2
DDR A D3	AM38	SA_DQ_3
DDR A D4	AJ36	SA_DQ_4
DDR A D5	AJ40	SA_DQ_5
DDR A D6	AM44	SA_DQ_6
DDR A D7	AM42	SA_DQ_7
DDR A D8	AN43	SA_DQ_8
DDR A D9	AN44	SA_DQ_9
DDR A D10	AJ40	SA_DQ_10
DDR A D11	AT138	SA_DQ_11
DDR A D12	AN41	SA_DQ_12
DDR A D13	AN39	SA_DQ_13
DDR A D14	AJ44	SA_DQ_14
DDR A D15	AJ42	SA_DQ_15
DDR A D16	AV39	SA_DQ_16
DDR A D17	AY44	SA_DQ_17
DDR A D18	BA40	SA_DQ_18
DDR A D19	BD43	SA_DQ_19
DDR A D20	AV41	SA_DQ_20
DDR A D21	AY43	SA_DQ_21
DDR A D22	BB41	SA_DQ_22
DDR A D23	BC40	SA_DQ_23
DDR A D24	AY37	SA_DQ_24
DDR A D25	BD38	SA_DQ_25
DDR A D26	AV37	SA_DQ_26
DDR A D27	AT36	SA_DQ_27
DDR A D28	AV38	SA_DQ_28
DDR A D29	BR38	SA_DQ_29
DDR A D30	AV36	SA_DQ_30
DDR A D31	AW36	SA_DQ_31
DDR A D32	BD13	SA_DQ_32
DDR A D33	AU11	SA_DQ_33
DDR A D34	BC11	SA_DQ_34
DDR A D35	BA12	SA_DQ_35
DDR A D36	AU13	SA_DQ_36
DDR A D37	AV13	SA_DQ_37
DDR A D38	BD12	SA_DQ_38
DDR A D39	BC12	SA_DQ_39
DDR A D40	BD9	SA_DQ_40
DDR A D41	BA9	SA_DQ_41
DDR A D42	AU10	SA_DQ_42
DDR A D43	AV9	SA_DQ_43
DDR A D44	BA11	SA_DQ_44
DDR A D45	BD9	SA_DQ_45
DDR A D46	AY8	SA_DQ_46
DDR A D47	BA6	SA_DQ_47
DDR A D48	AV5	SA_DQ_48
DDR A D49	AV7	SA_DQ_49
DDR A D50	AT9	SA_DQ_50
DDR A D51	AN8	SA_DQ_51
DDR A D52	AU5	SA_DQ_52
DDR A D53	AU6	SA_DQ_53
DDR A D54	AT5	SA_DQ_54
DDR A D55	AN10	SA_DQ_55
DDR A D56	AM11	SA_DQ_56
DDR A D57	AM5	SA_DQ_57
DDR A D58	AJ9	SA_DQ_58
DDR A D59	AJ8	SA_DQ_59
DDR A D60	AN12	SA_DQ_60
DDR A D61	AM13	SA_DQ_61
DDR A D62	AJ11	SA_DQ_62
DDR A D63	AJ12	SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDR A BS0	DDR_A_BS0	15,16
SA_BS_1	BG18	DDR A BS1	DDR_A_BS1	15,16
SA_BS_2	AT25	DDR A BS2	DDR_A_BS2	15,16
SA_RAS#	BB20	DDR A RAS#	DDR_A_RAS#	15,16
SA_CAS#	BD20	DDR A CAS#	DDR_A_CAS#	15,16
SA_WE#	AY20	DDR A WE#	DDR_A_WE#	15,16
SA_DM_0	AM37	DDR A DM0	DDR_A_DM[0..7]	15
SA_DM_1	AY41	DDR A DM1		
SA_DM_2	AU39	DDR A DM2		
SA_DM_3	BB12	DDR A DM3		
SA_DM_4	AY6	DDR A DM4		
SA_DM_5	AT7	DDR A DM5		
SA_DM_6	AJ5	DDR A DM6		
SA_DM_7	AJ5	DDR A DM7		
SA_DQS_0	AJ44	DDR A DQS0	DDR_A_DQS[0..7]	15
SA_DQS_1	AT44	DDR A DQS1		
SA_DQS_2	BA43	DDR A DQS2		
SA_DQS_3	BC37	DDR A DQS3		
SA_DQS_4	AW12	DDR A DQS4		
SA_DQS_5	BC8	DDR A DQS5		
SA_DQS_6	AU8	DDR A DQS6		
SA_DQS_7	AM7	DDR A DQS7		
SA_DQS#_0	AJ43	DDR A DQS#0	DDR_A_DQS#[0..7]	15
SA_DQS#_1	AT43	DDR A DQS#1		
SA_DQS#_2	BA44	DDR A DQS#2		
SA_DQS#_3	BD37	DDR A DQS#3		
SA_DQS#_4	AY12	DDR A DQS#4		
SA_DQS#_5	BD8	DDR A DQS#5		
SA_DQS#_6	AU9	DDR A DQS#6		
SA_DQS#_7	AM8	DDR A DQS#7		
SA_MA_0	BA21	DDR A MA0	DDR_A_MA[0..14]	15,16
SA_MA_1	BC24	DDR A MA1		
SA_MA_2	BG24	DDR A MA2		
SA_MA_3	BH24	DDR A MA3		
SA_MA_4	BG25	DDR A MA4		
SA_MA_5	BA24	DDR A MA5		
SA_MA_6	BD24	DDR A MA6		
SA_MA_7	BG27	DDR A MA7		
SA_MA_8	BE25	DDR A MA8		
SA_MA_9	AW24	DDR A MA9		
SA_MA_10	BC21	DDR A MA10		
SA_MA_11	BG26	DDR A MA11		
SA_MA_12	BH26	DDR A MA12		
SA_MA_13	BH17	DDR A MA13		
SA_MA_14	AY25	DDR A MA14		

CANTIGA_1p0

15 DDR_B_D[0..63]

U28E

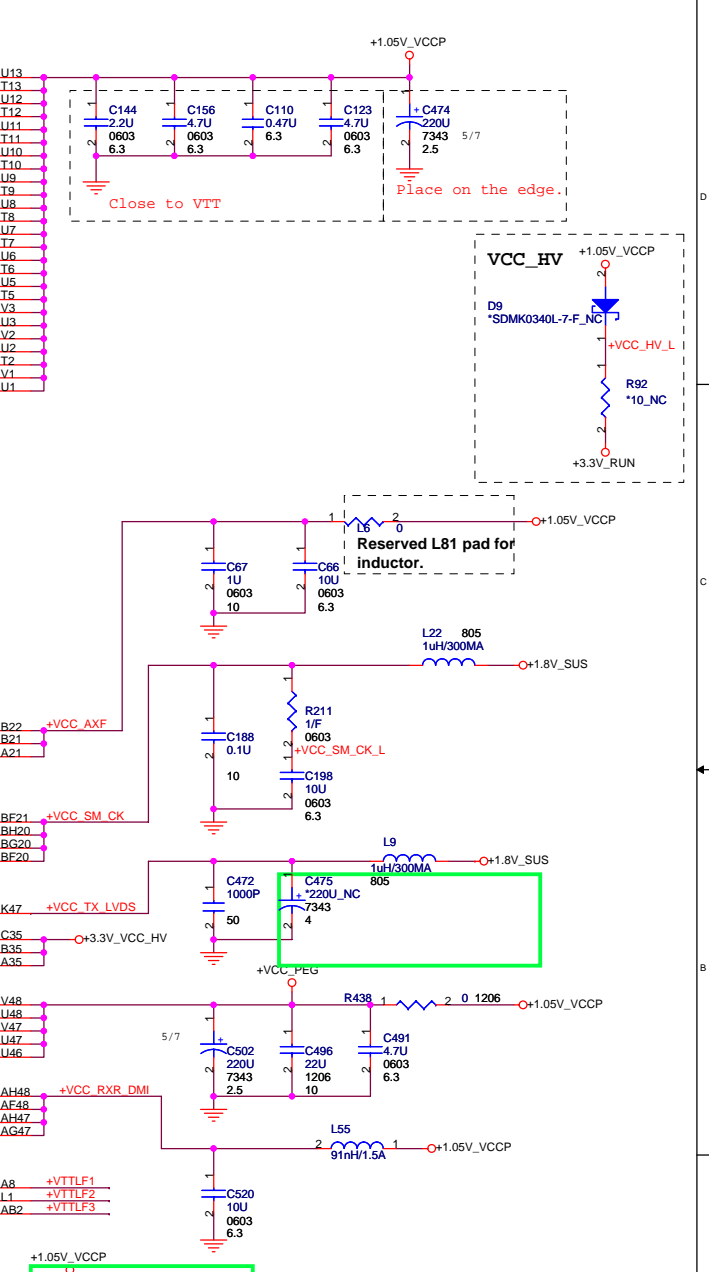
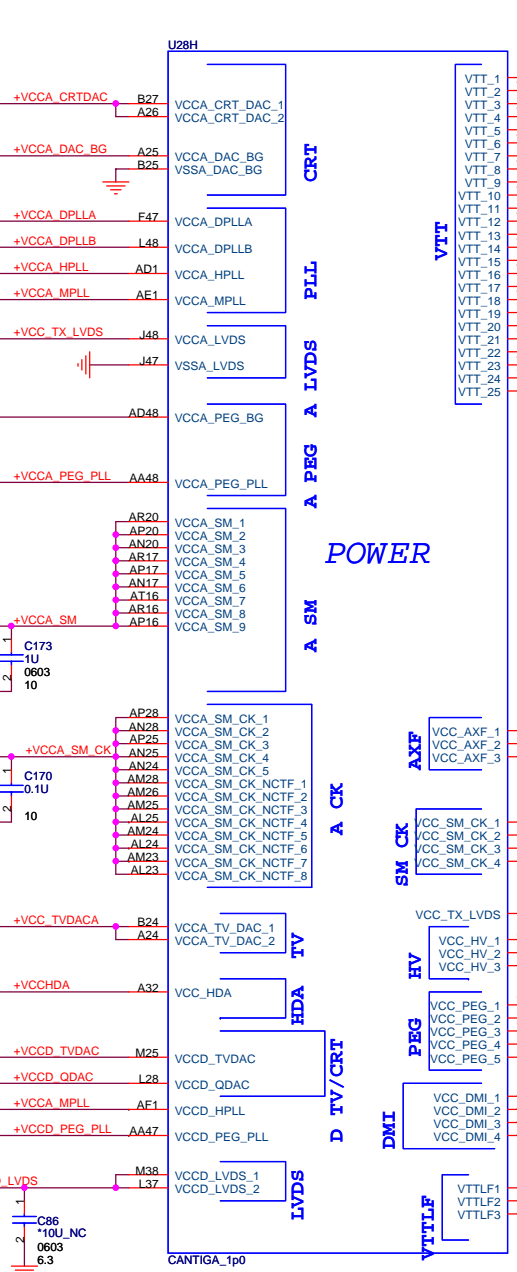
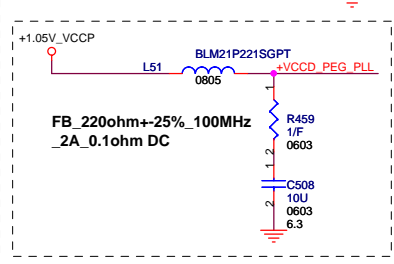
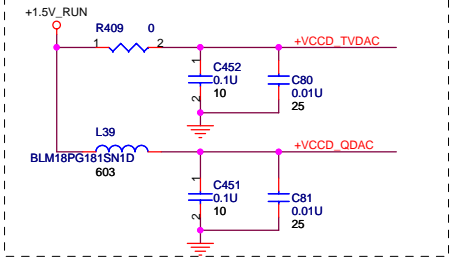
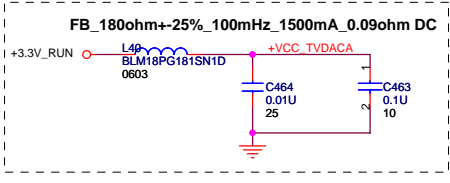
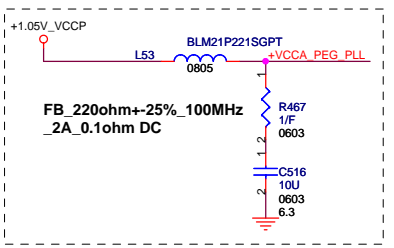
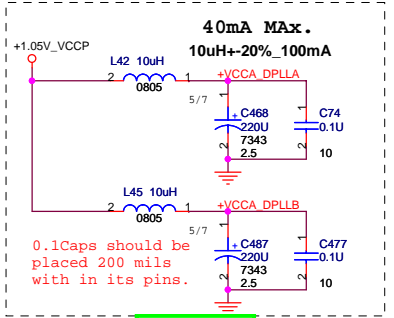
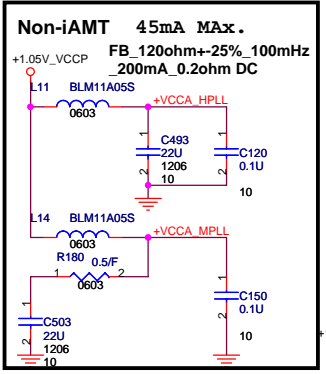
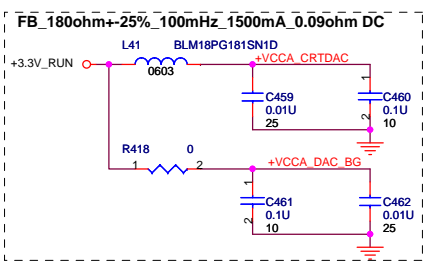
DDR B D0	AK47	SB_DQ_0
DDR B D1	AH46	SB_DQ_1
DDR B D2	AP47	SB_DQ_2
DDR B D3	AP46	SB_DQ_3
DDR B D4	AJ46	SB_DQ_4
DDR B D5	AJ48	SB_DQ_5
DDR B D6	AP48	SB_DQ_6
DDR B D7	AP48	SB_DQ_7
DDR B D8	AU47	SB_DQ_8
DDR B D9	AJ46	SB_DQ_9
DDR B D10	BA48	SB_DQ_10
DDR B D11	AY48	SB_DQ_11
DDR B D12	AT47	SB_DQ_12
DDR B D13	AR47	SB_DQ_13
DDR B D14	BA47	SB_DQ_14
DDR B D15	BC47	SB_DQ_15
DDR B D16	BC46	SB_DQ_16
DDR B D17	BC44	SB_DQ_17
DDR B D18	BG43	SB_DQ_18
DDR B D19	BF43	SB_DQ_19
DDR B D20	BE45	SB_DQ_20
DDR B D21	BC41	SB_DQ_21
DDR B D22	BF40	SB_DQ_22
DDR B D23	BF41	SB_DQ_23
DDR B D24	BG38	SB_DQ_24
DDR B D25	BF38	SB_DQ_25
DDR B D26	BH35	SB_DQ_26
DDR B D27	BG35	SB_DQ_27
DDR B D28	BH40	SB_DQ_28
DDR B D29	BG39	SB_DQ_29
DDR B D30	BG34	SB_DQ_30
DDR B D31	BH34	SB_DQ_31
DDR B D32	BH14	SB_DQ_32
DDR B D33	BG12	SB_DQ_33
DDR B D34	BH11	SB_DQ_34
DDR B D35	BG8	SB_DQ_35
DDR B D36	BH12	SB_DQ_36
DDR B D37	BF11	SB_DQ_37
DDR B D38	BF8	SB_DQ_38
DDR B D39	BG7	SB_DQ_39
DDR B D40	BC5	SB_DQ_40
DDR B D41	BC6	SB_DQ_41
DDR B D42	AY3	SB_DQ_42
DDR B D43	AY1	SB_DQ_43
DDR B D44	BF6	SB_DQ_44
DDR B D45	BF5	SB_DQ_45
DDR B D46	BA1	SB_DQ_46
DDR B D47	BD3	SB_DQ_47
DDR B D48	AV2	SB_DQ_48
DDR B D49	AU3	SB_DQ_49
DDR B D50	AR3	SB_DQ_50
DDR B D51	AN2	SB_DQ_51
DDR B D52	AY2	SB_DQ_52
DDR B D53	AV1	SB_DQ_53
DDR B D54	AP3	SB_DQ_54
DDR B D55	AR1	SB_DQ_55
DDR B D56	AL1	SB_DQ_56
DDR B D57	AL2	SB_DQ_57
DDR B D58	AJ1	SB_DQ_58
DDR B D59	AH1	SB_DQ_59
DDR B D60	AM2	SB_DQ_60
DDR B D61	AM3	SB_DQ_61
DDR B D62	AH3	SB_DQ_62
DDR B D63	AJ3	SB_DQ_63

DDR SYSTEM MEMORY B

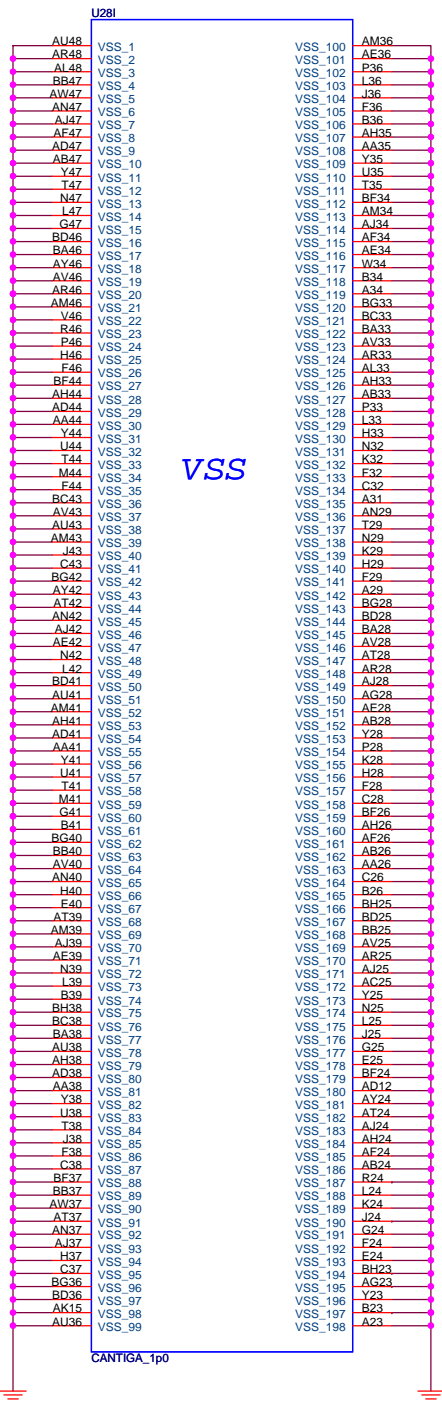
SB_BS_0	BC16	DDR B BS0	DDR_B_BS0	15,16
SB_BS_1	BB17	DDR B BS1	DDR_B_BS1	15,16
SB_BS_2	BB33	DDR B BS2	DDR_B_BS2	15,16
SB_RAS#	AJ17	DDR B RAS#	DDR_B_RAS#	15,16
SB_CAS#	BG16	DDR B CAS#	DDR_B_CAS#	15,16
SB_WE#	BF14	DDR B WE#	DDR_B_WE#	15,16
SB_DM_0	AM47	DDR B DM0	DDR_B_DM[0..7]	15
SB_DM_1	AY47	DDR B DM1		
SB_DM_2	BD40	DDR B DM2		
SB_DM_3	BF35	DDR B DM3		
SB_DM_4	BG11	DDR B DM4		
SB_DM_5	BA3	DDR B DM5		
SB_DM_6	AP1	DDR B DM6		
SB_DM_7	AK2	DDR B DM7		
SB_DQS_0	AL47	DDR B DQS0	DDR_B_DQS[0..7]	15
SB_DQS_1	AV48	DDR B DQS1		
SB_DQS_2	BG41	DDR B DQS2		
SB_DQS_3	BG37	DDR B DQS3		
SB_DQS_4	BH9	DDR B DQS4		
SB_DQS_5	BB2	DDR B DQS5		
SB_DQS_6	AU1	DDR B DQS6		
SB_DQS_7	AN6	DDR B DQS7		
SB_DQS#_0	AL46	DDR B DQS#0	DDR_B_DQS#[0..7]	15
SB_DQS#_1	AV47	DDR B DQS#1		
SB_DQS#_2	BH41	DDR B DQS#2		
SB_DQS#_3	BH37	DDR B DQS#3		
SB_DQS#_4	BG9	DDR B DQS#4		
SB_DQS#_5	BC2	DDR B DQS#5		
SB_DQS#_6	AT2	DDR B DQS#6		
SB_DQS#_7	AN5	DDR B DQS#7		
SB_MA_0	AV17	DDR B MA0	DDR_B_MA[0..14]	15,16
SB_MA_1	BA25	DDR B MA1		
SB_MA_2	AU25	DDR B MA2		
SB_MA_3	AW25	DDR B MA3		
SB_MA_4	BB28	DDR B MA4		
SB_MA_5	AJ28	DDR B MA5		
SB_MA_6	AW28	DDR B MA6		
SB_MA_7	AT33	DDR B MA7		
SB_MA_8	BD33	DDR B MA8		
SB_MA_9	BB16	DDR B MA9		
SB_MA_10	AY33	DDR B MA10		
SB_MA_11	BH15	DDR B MA11		
SB_MA_12	AY33	DDR B MA12		
SB_MA_13	BH15	DDR B MA13		
SB_MA_14	AJ33	DDR B MA14		

CANTIGA_1p0

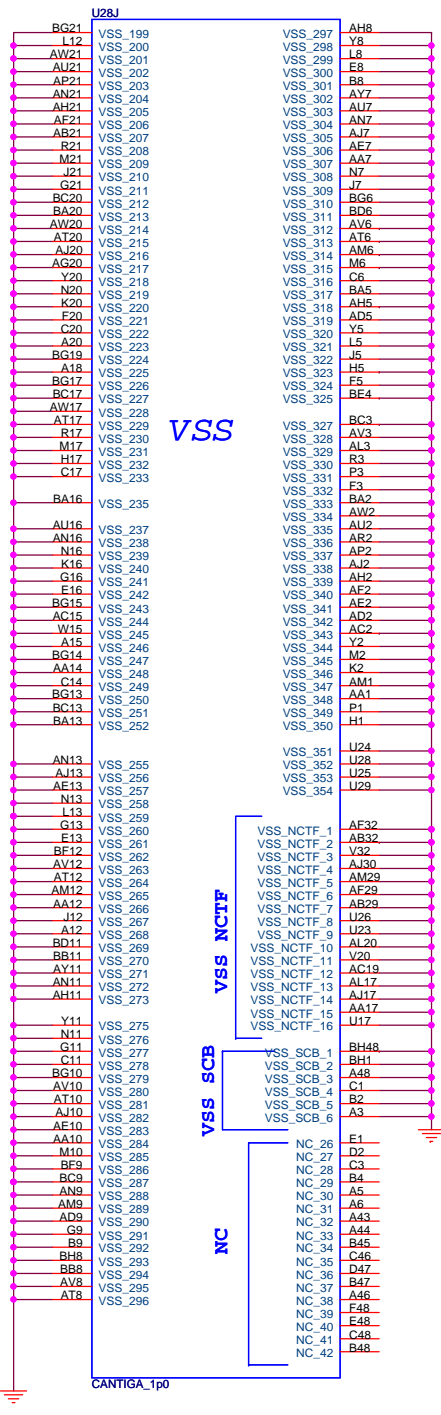




Title: Crestline (POWER)		
Size: FM7B	Document Number: FM7B	Rev: 1A
Date: Wednesday, July 16, 2008	Sheet: 9	of 60



VSS

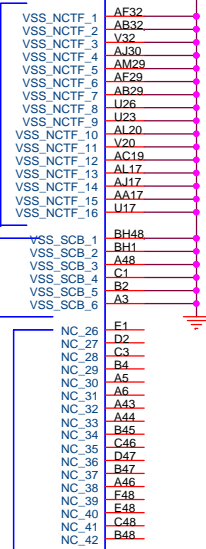


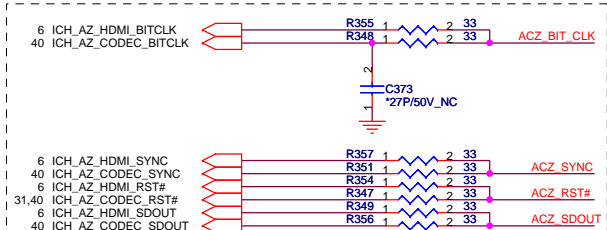
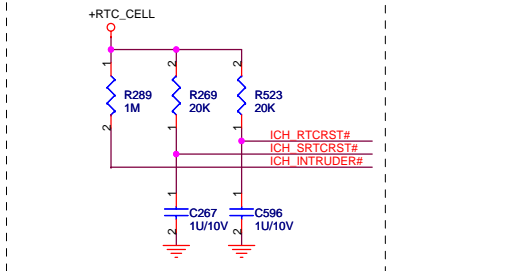
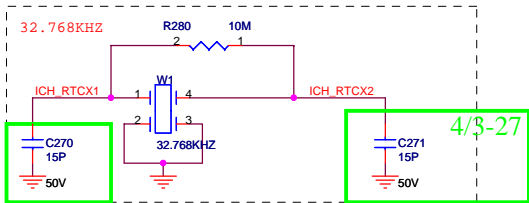
VSS

VSS NCTF

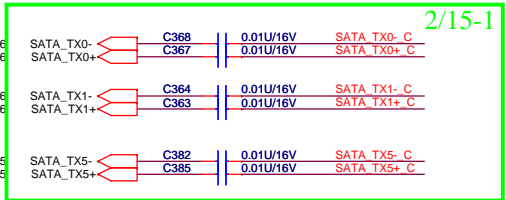
VSS SCB

NC

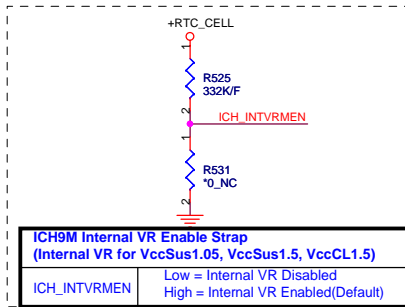




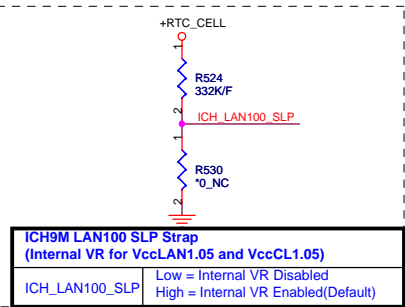
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically, keep the same distance from T for all series termination resistors.



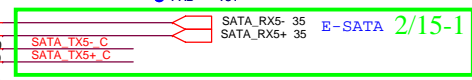
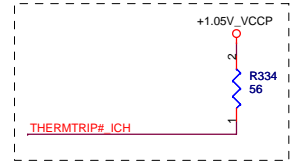
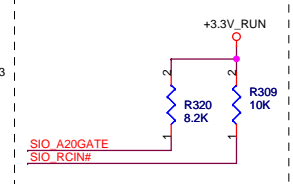
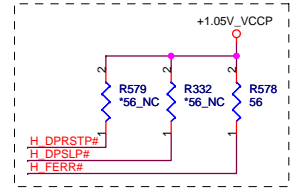
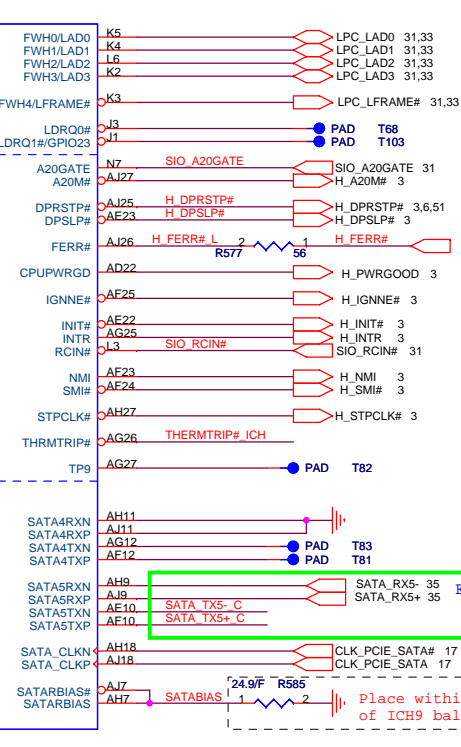
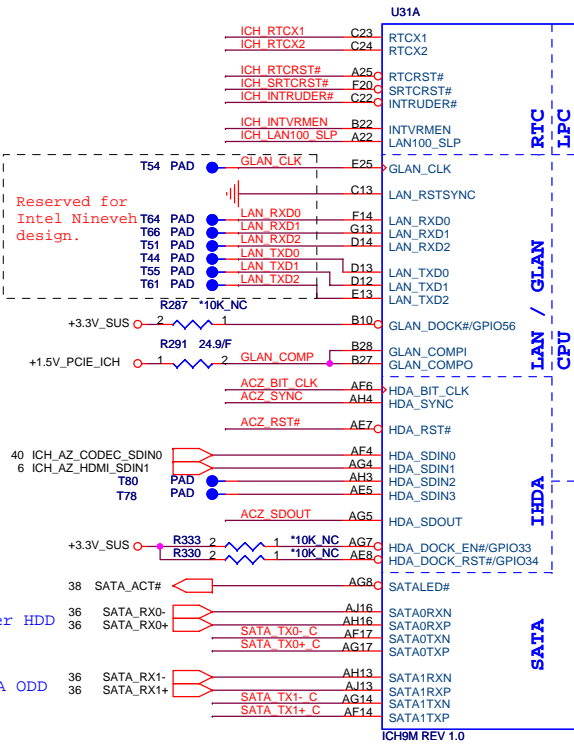
Master HDD
SATA ODD



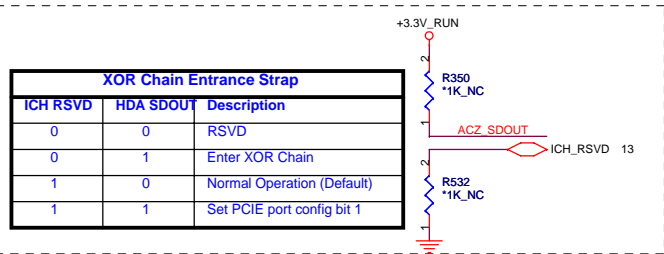
ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled	High = Internal VR Enabled(Default)



ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled	High = Internal VR Enabled(Default)

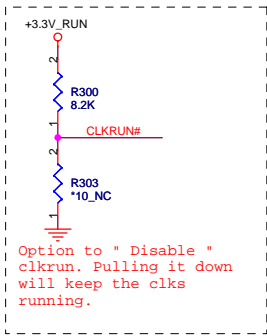
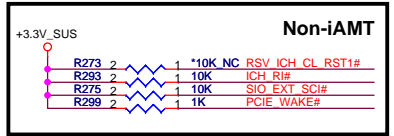
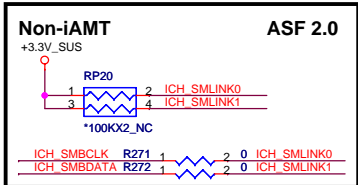
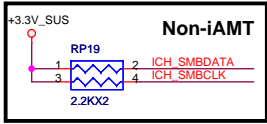


Place within 500mils of ICH9 ball

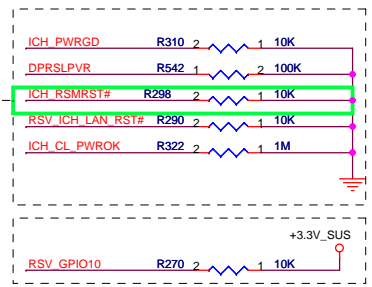
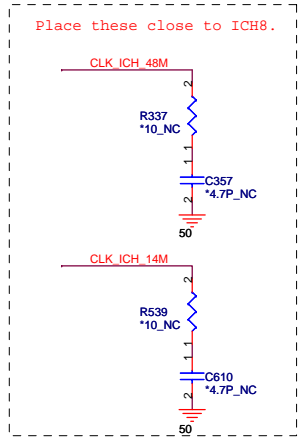
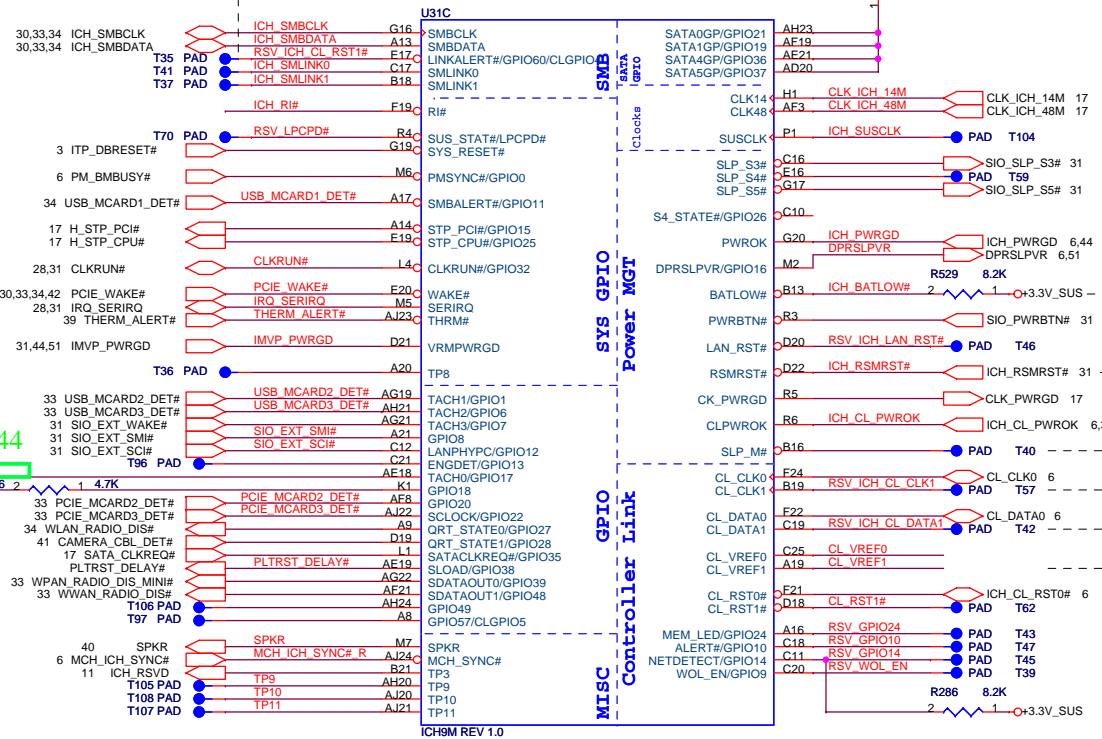


XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1

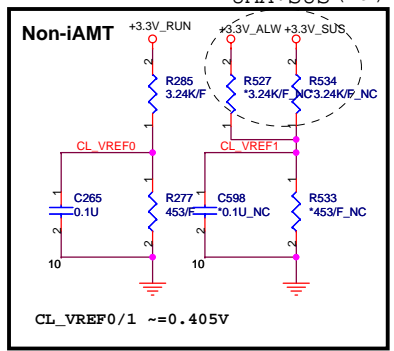
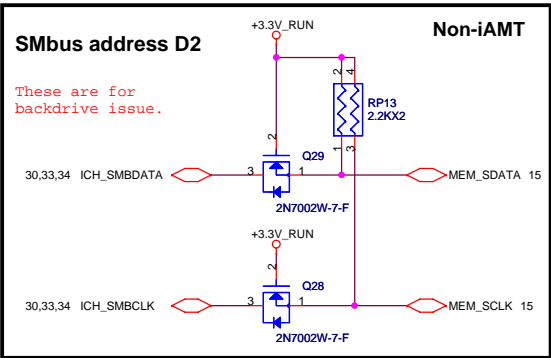
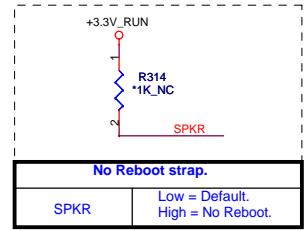
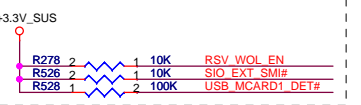
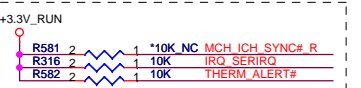
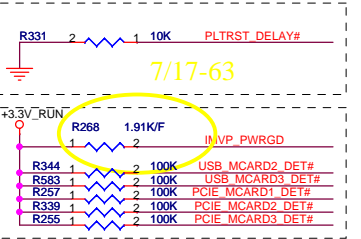




2/25-17 6/11-44



Non-iAMT



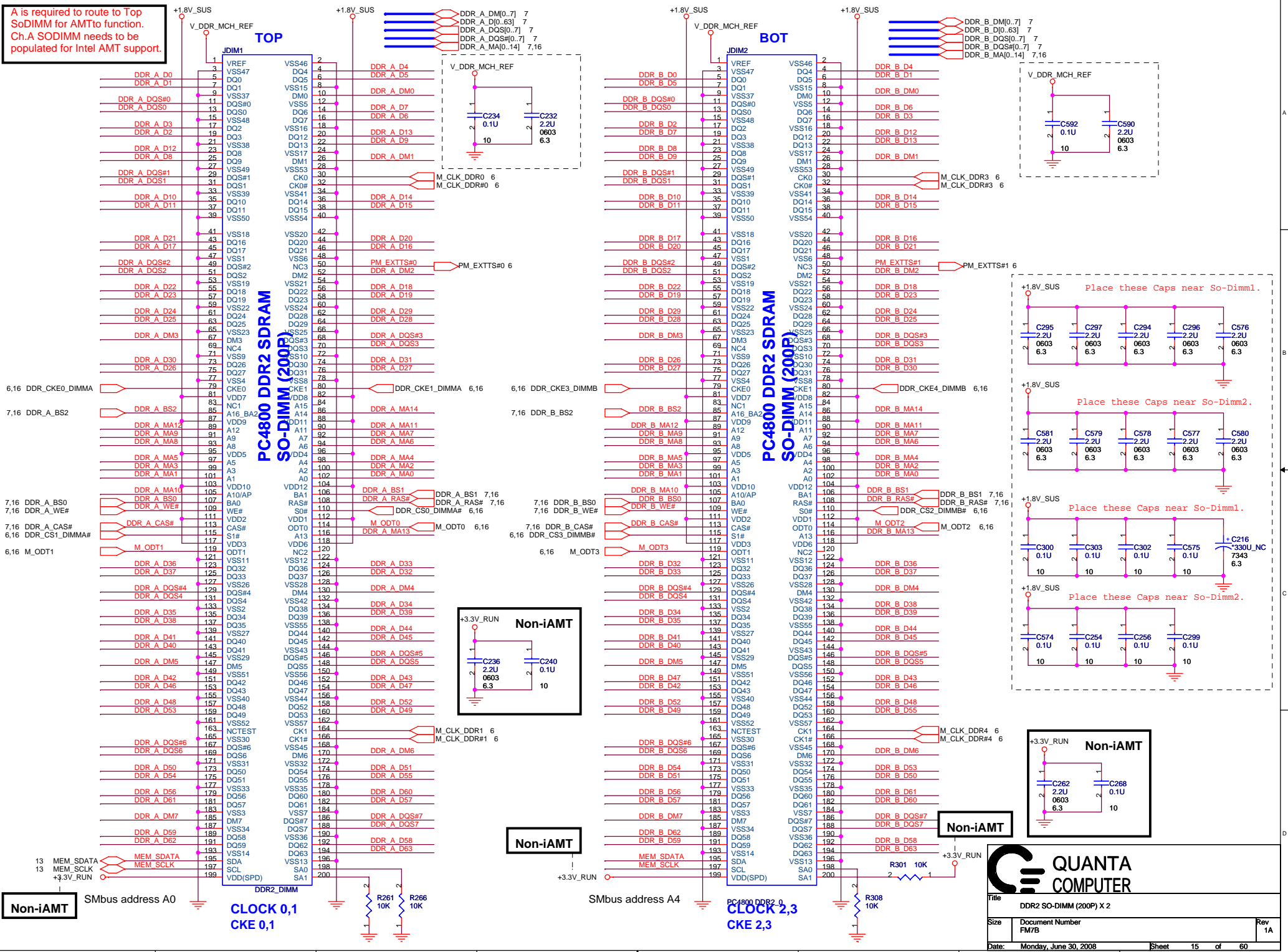
QUANTA COMPUTER

Title: ICH9-M (PM,GPIO,SMB,CL)

Size: Document Number FM7B Rev 1A

Date: Thursday, July 17, 2008 Sheet 13 of 60

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



Non-iAMT

Non-iAMT

Non-iAMT

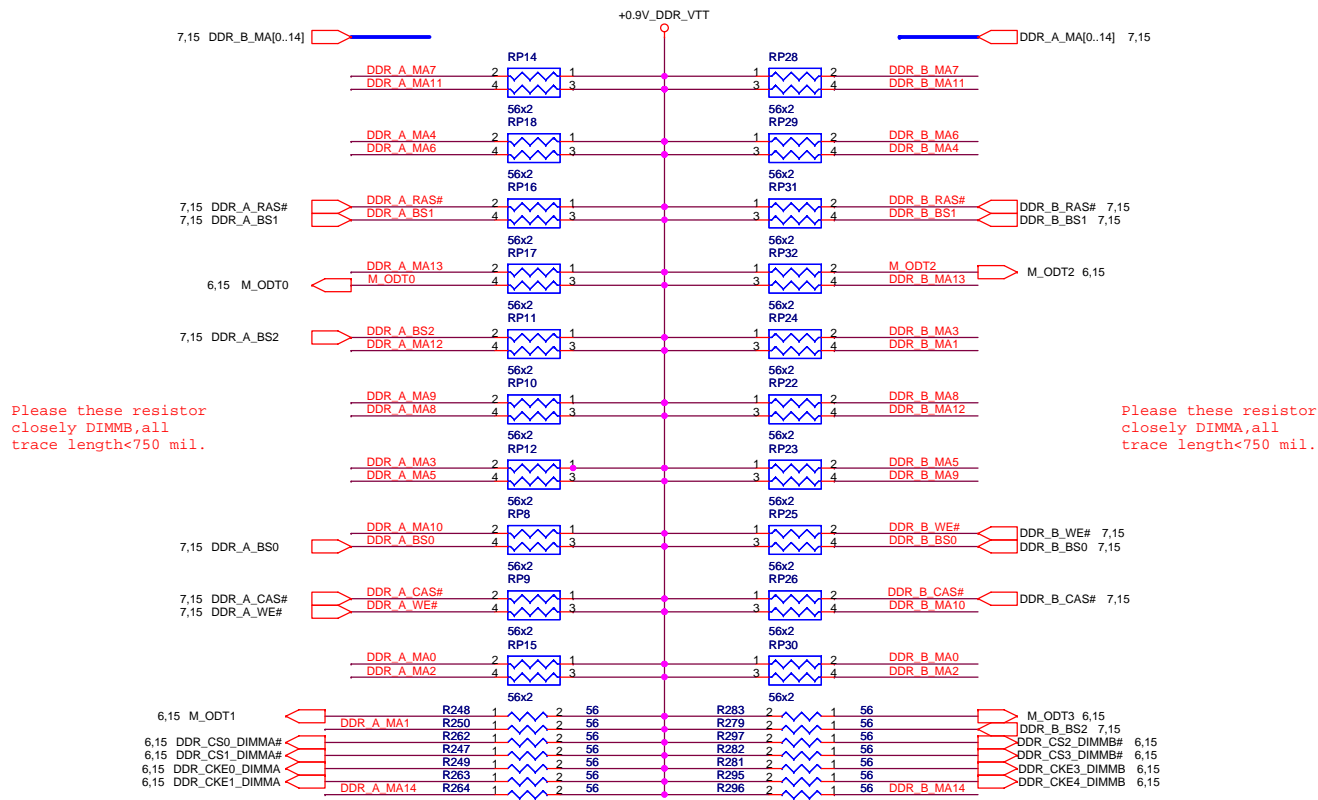
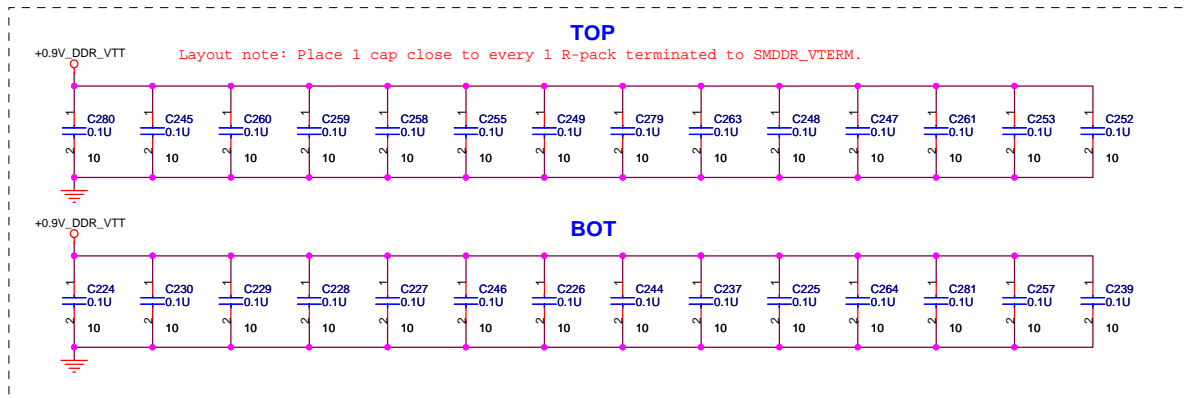
Non-iAMT

QUANTA COMPUTER

Title: DDR2 SO-DIMM (200P) X 2

Size	Document Number FM7B	Rev 1A
------	----------------------	--------

Date: Monday, June 30, 2008 Sheet 15 of 60



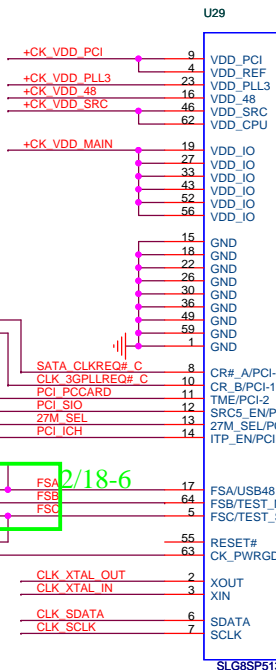
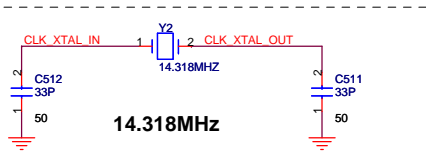
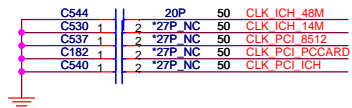
**QUANTA
COMPUTER**

Title: **DDR2 RES ARRAY**

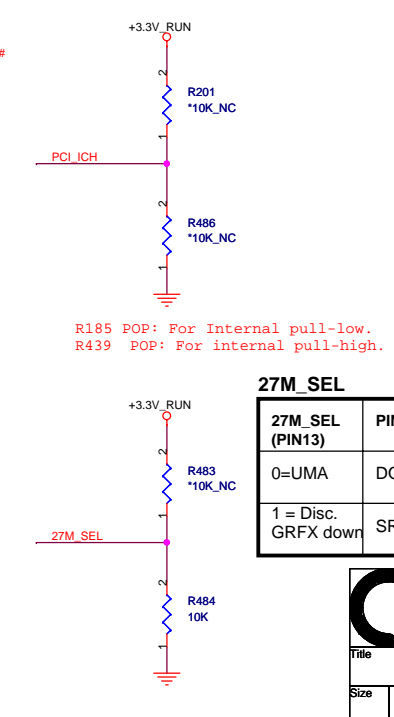
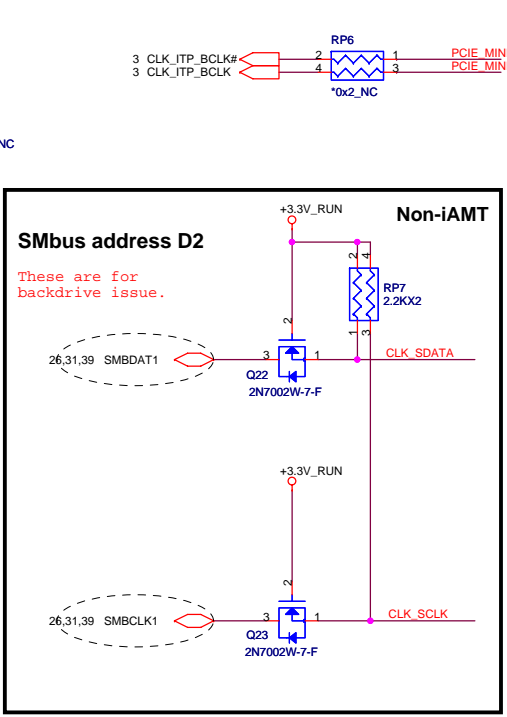
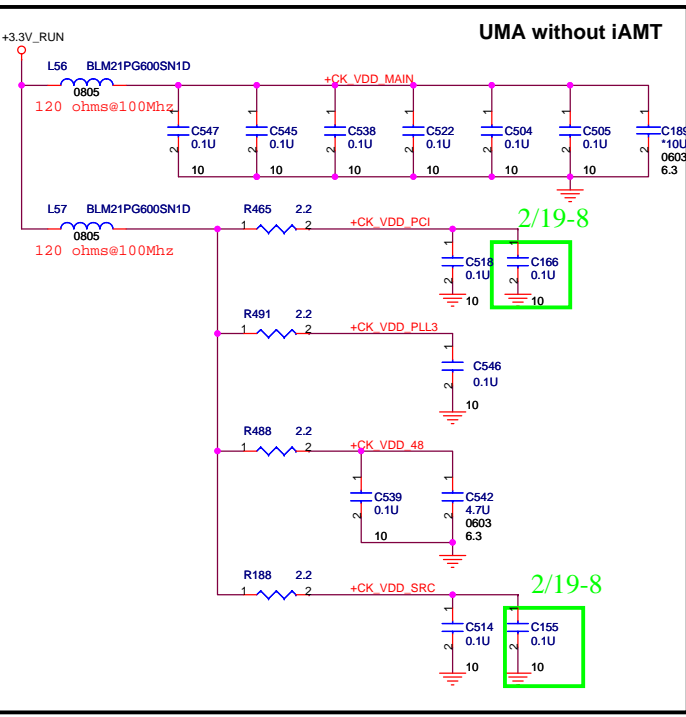
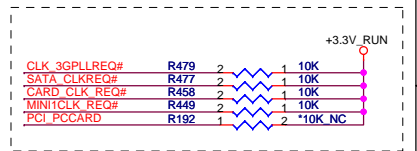
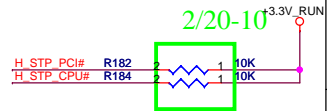
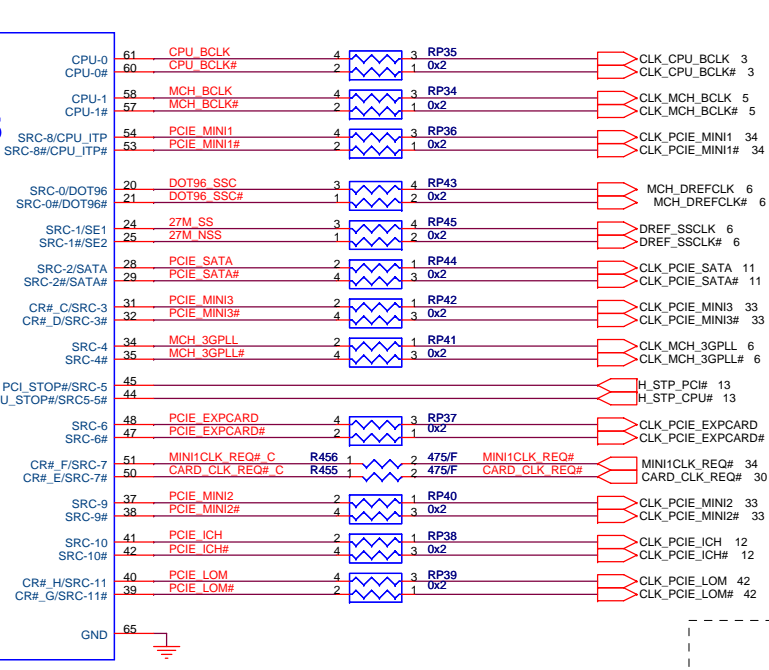
Size: **Document Number FM7B** Rev: **1A**

Date: **Monday, June 30, 2008** Sheet: **16** of **60**

Add capacitor pads for improving WWAN.



CK505 QFN64



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

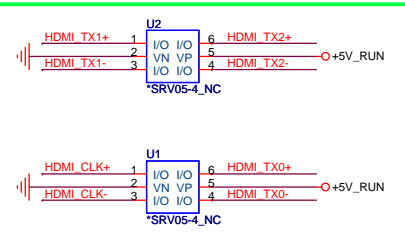
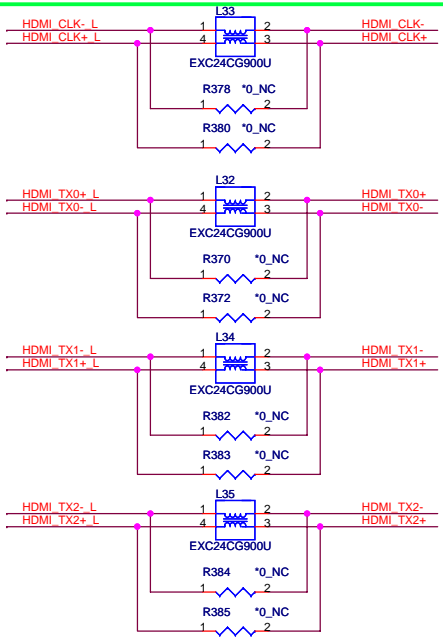
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

Title: CLOCK GENERATOR

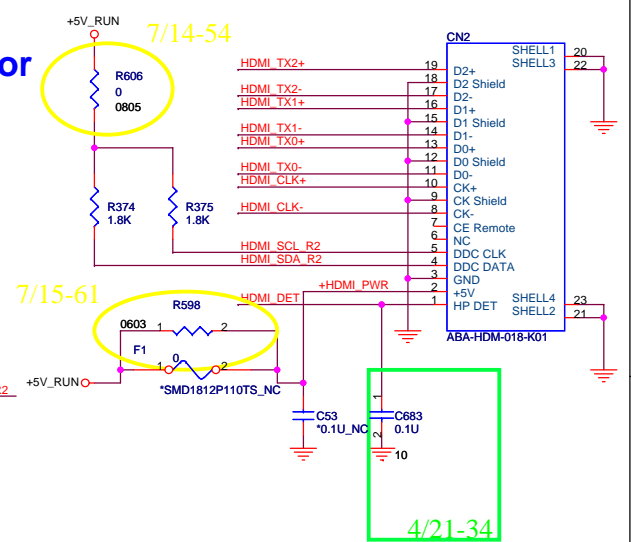
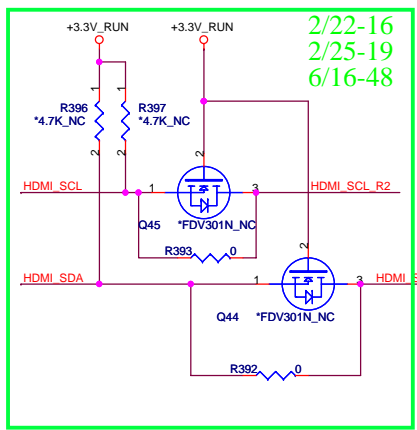
Size: Document Number FM7B Rev 1A

Date: Monday, July 14, 2008 Sheet 17 of 60

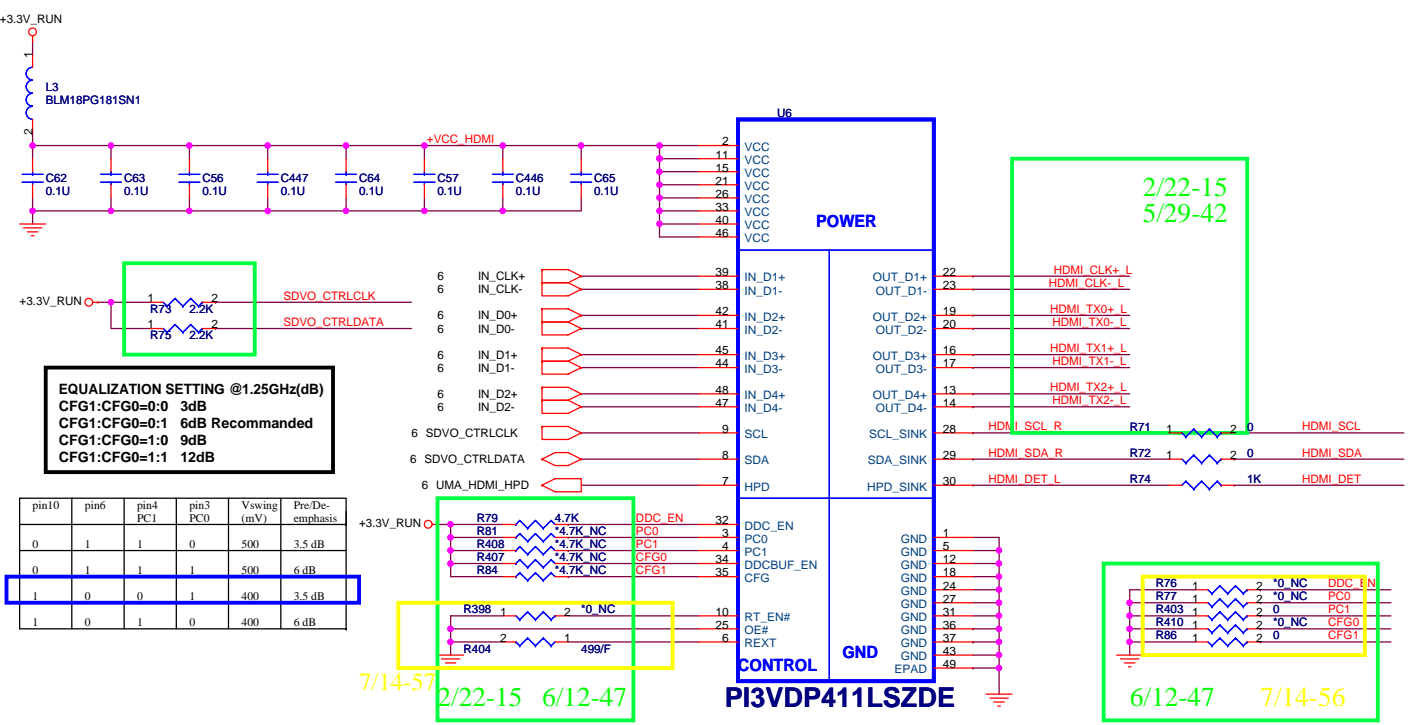


4/17-31

HDMI Connector



Reserve for EMI and close to HDMI CONN




EQUALIZATION SETTING @1.25GHz(dB)

CFG1:CFG0=0:0 3dB
 CFG1:CFG0=0:1 6dB Recommended
 CFG1:CFG0=1:0 9dB
 CFG1:CFG0=1:1 12dB


pin10	pin6	pin4 PC1	pin3 PC0	Vswing (mV)	Pre/De-emphasis
0	1	1	0	500	3.5 dB
0	1	1	1	500	6 dB
1	0	0	1	400	3.5 dB
1	0	1	0	400	6 dB




**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 19 of 60


**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 20 of 60

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 21 of 60

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 22 of 60

A

B

C

D

E

4

4

3


3

2

2

1

1

 QUANTA COMPUTER		
Title		
FLASH, RTC & KC		
Size	Document Number	Rev
FM6B		1A
Date:	Monday, June 30, 2008	Sheet 23 of 60

A

B

C

D

E

1

2

3

4

5

A

A

B


B

C

C

D

D

 QUANTA COMPUTER		
Title Battery Selector		
Size	Document Number FM6B	Rev 1A
Date: Monday, June 30, 2008	Sheet 24 of 60	

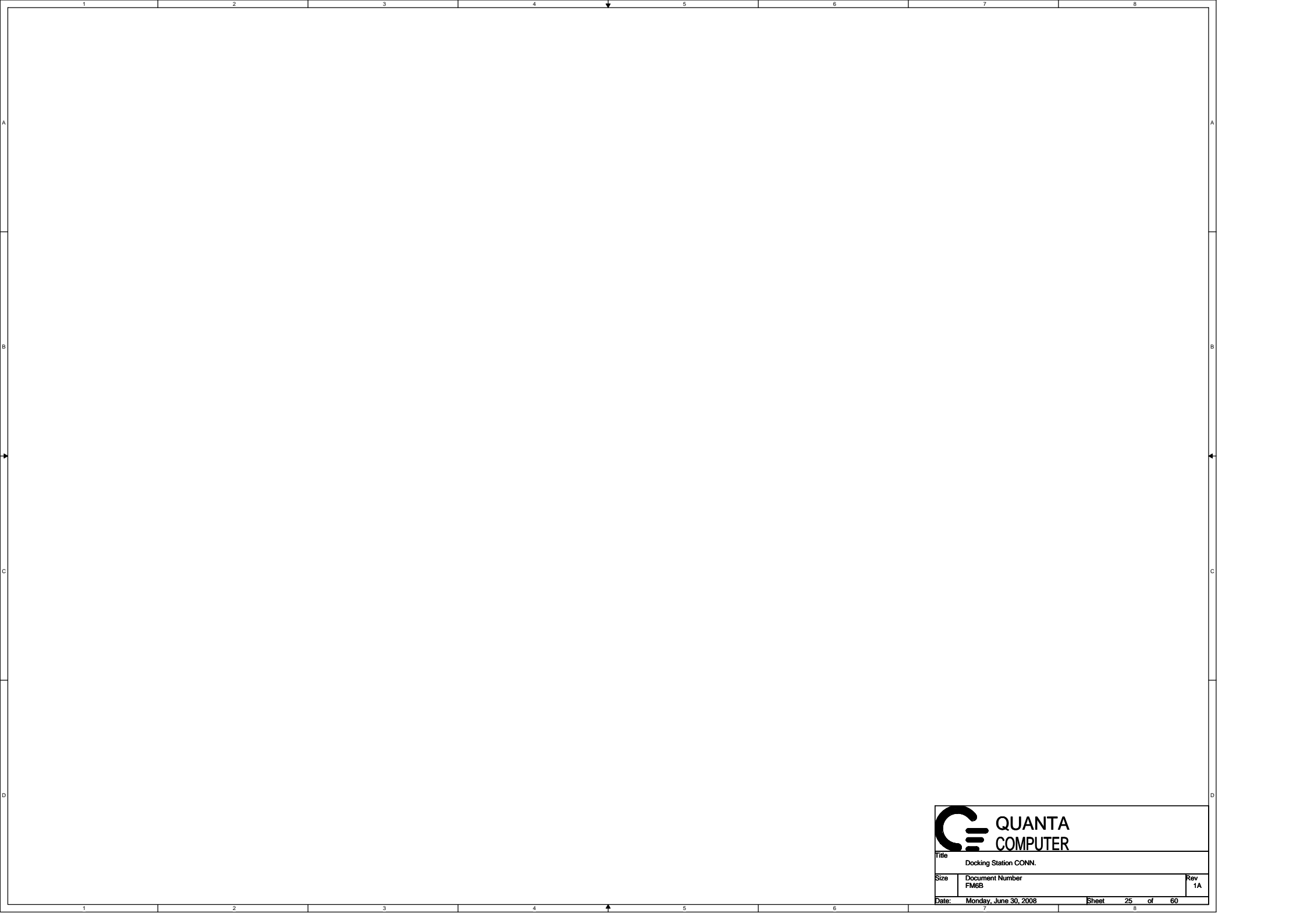
1

2

3

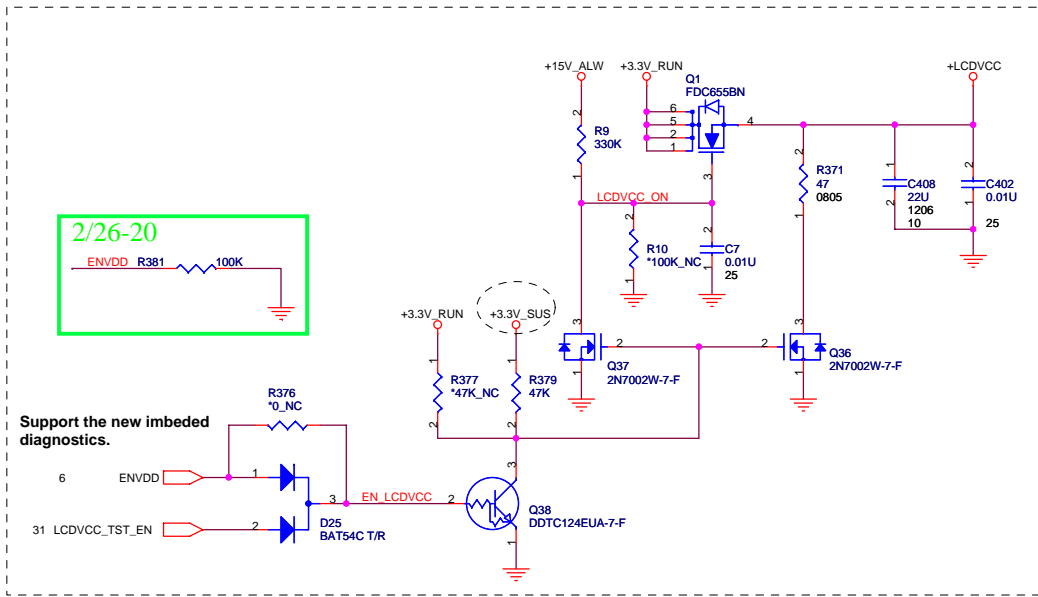
4

5



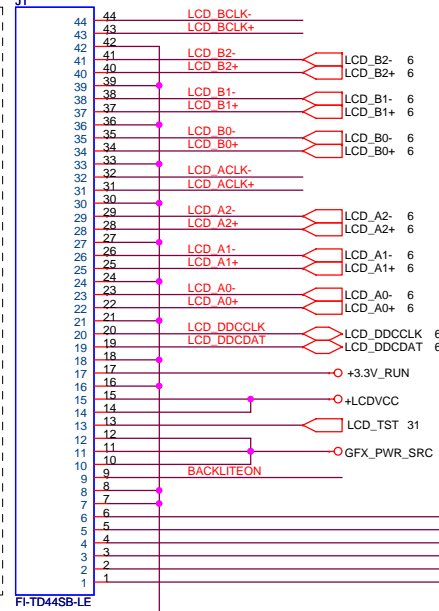
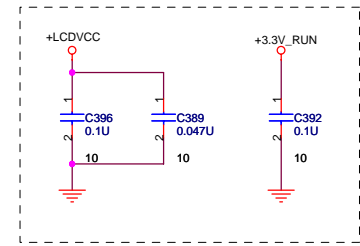
**QUANTA
COMPUTER**

Title		
Docking Station CONN.		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 25 of 60

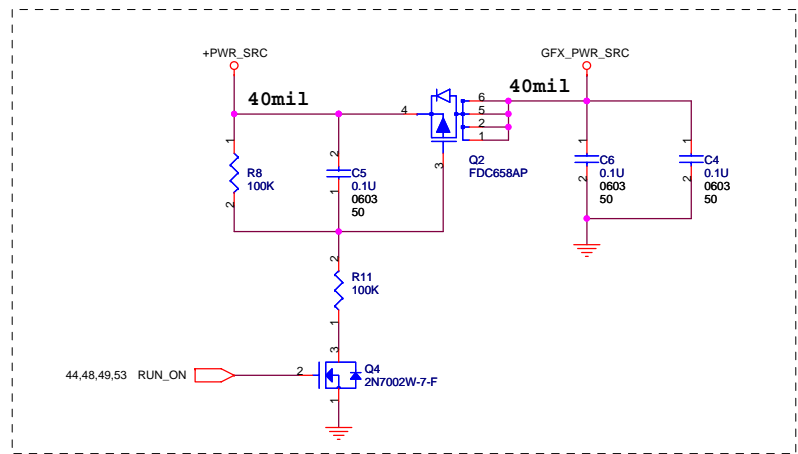
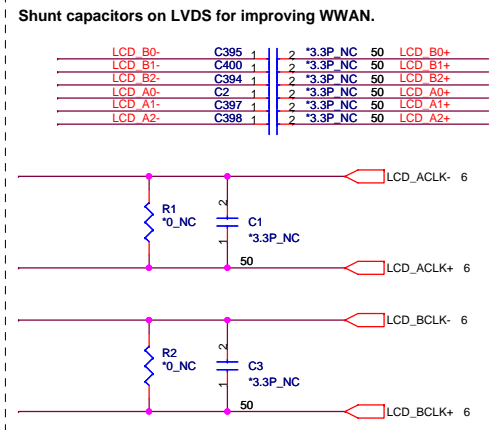
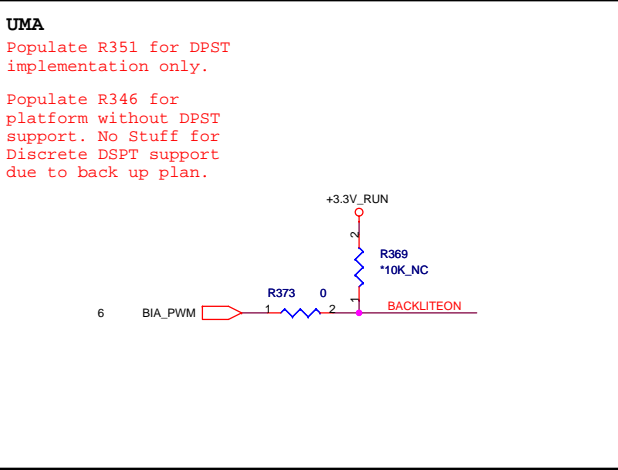


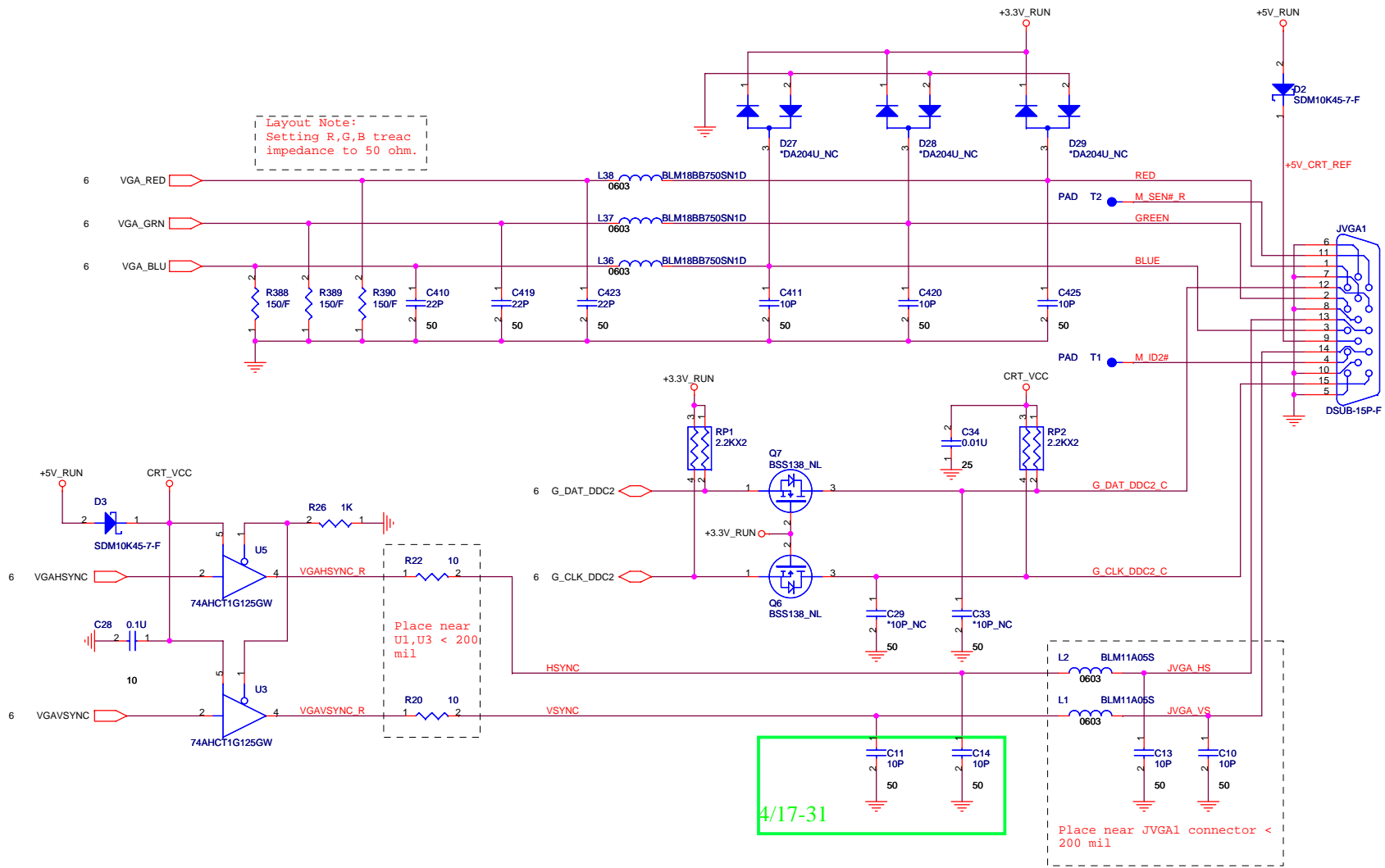
2/26-20
EN_VDD R381 100K

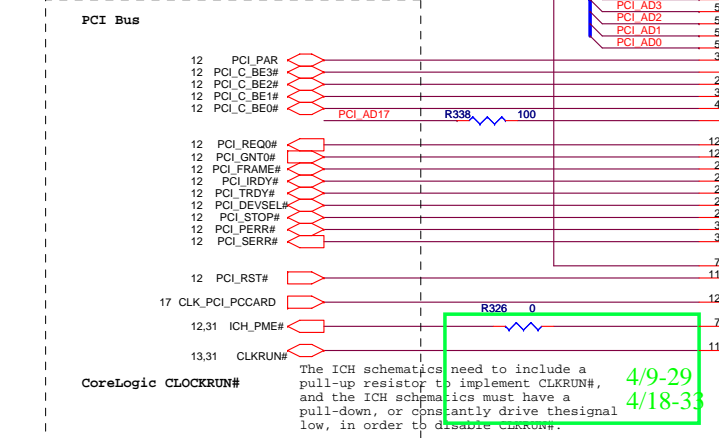
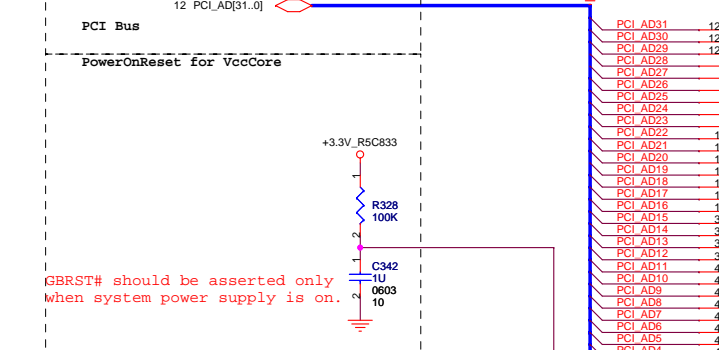
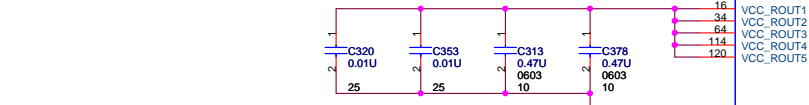
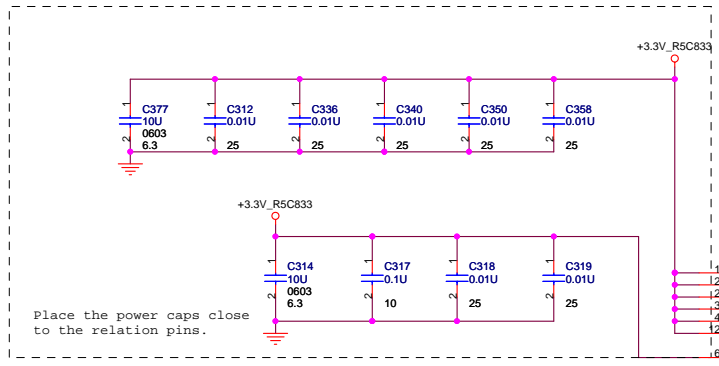
Support the new imbedded diagnostics.



Address : A9H --Contrast
AAH --Backlight

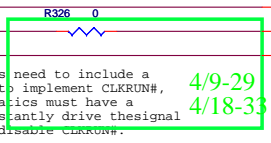
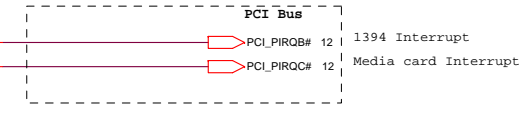
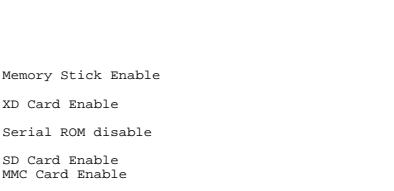
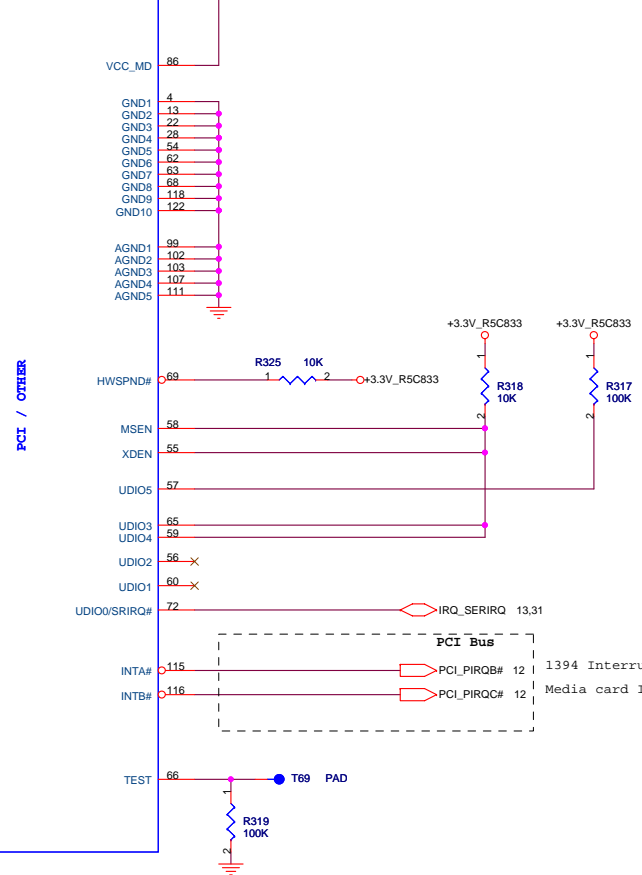
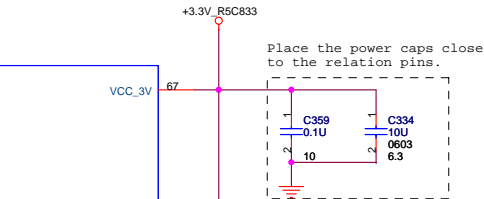




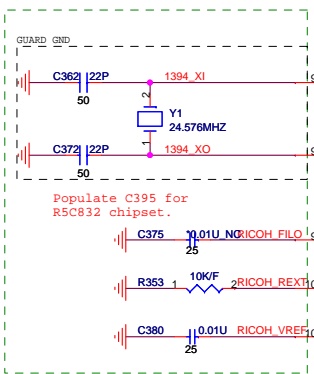


U20B

10	VCC_PCI1
120	VCC_PCI2
127	VCC_PCI3
32	VCC_PCI4
41	VCC_PCI5
128	VCC_PCI6
161	VCC_RIN
18	VCC_ROUT1
34	VCC_ROUT2
64	VCC_ROUT3
114	VCC_ROUT4
120	VCC_ROUT5
125	AD31
126	AD30
127	AD29
1	AD28
2	AD27
3	AD26
5	AD25
6	AD24
9	AD23
11	AD22
12	AD21
14	AD20
15	AD19
17	AD18
18	AD17
19	AD16
36	AD15
37	AD14
38	AD13
38	AD12
40	AD11
42	AD10
43	AD9
44	AD8
46	AD7
47	AD6
48	AD5
49	AD4
50	AD3
51	AD2
52	AD1
53	AD0
33	PAR
7	C/BE3#
21	C/BE2#
35	C/BE1#
45	C/BE0#
8	IDSEL
124	REQ#
123	GNT#
23	FRAME#
24	IRDY#
25	TRDY#
26	DEVSEL#
28	STOP#
30	PERR#
31	SERR#
71	GBRST#
119	PCIRST#
121	PCICLK
70	PME#
117	CLKRUN#

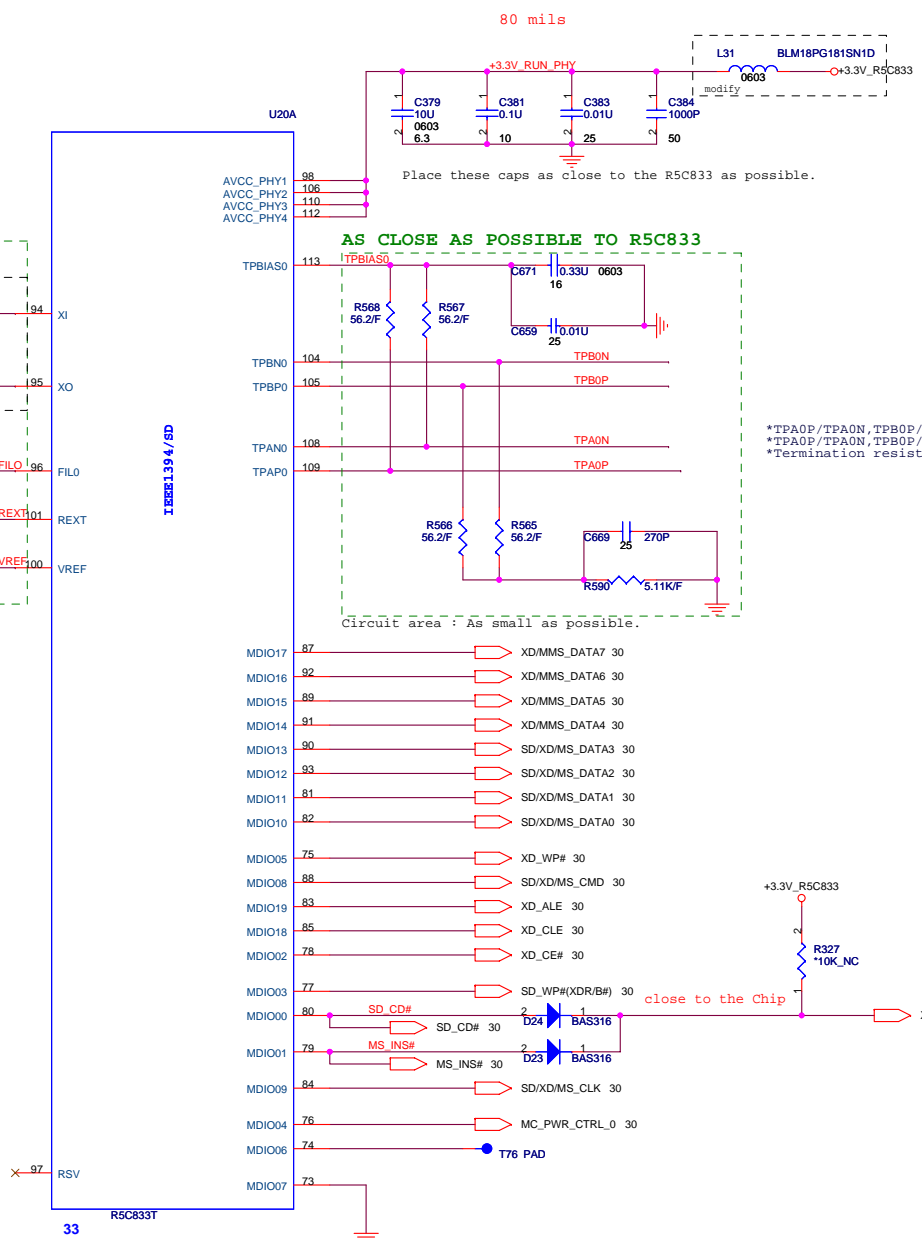


Refer to DELL M07 schematic X06



Populate C395 for R5C832 chipset.

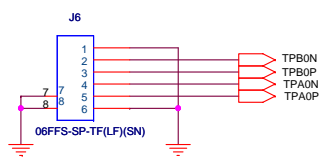
Place these caps as close to the U26 as possible.



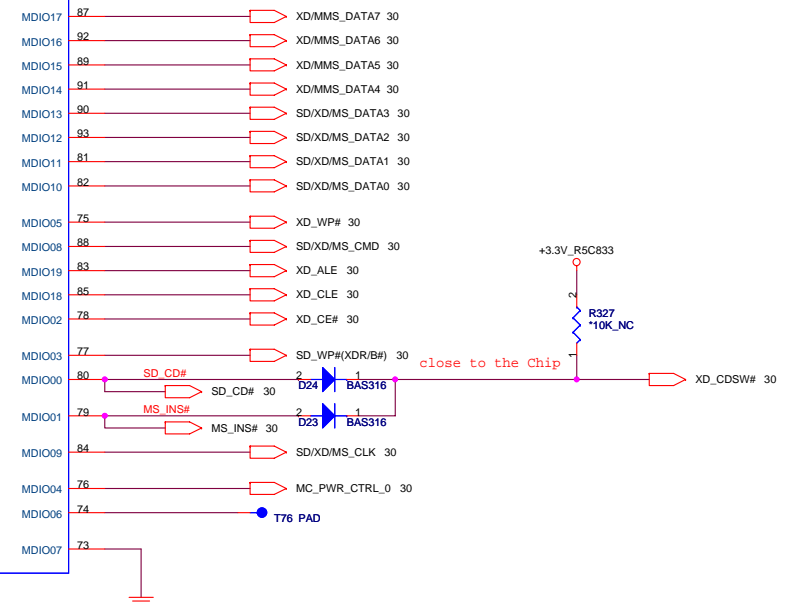
Place these caps as close to the R5C833 as possible.

AS CLOSE AS POSSIBLE TO R5C833

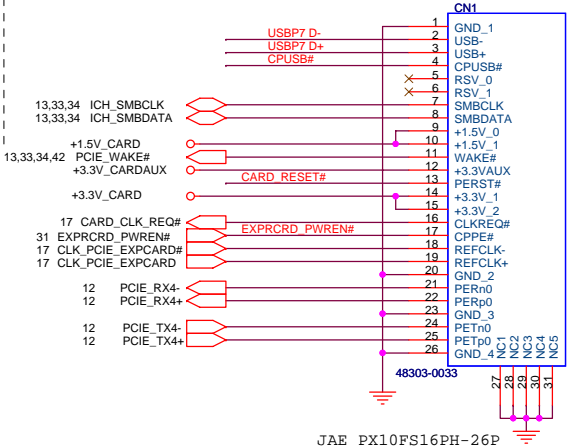
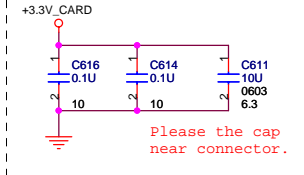
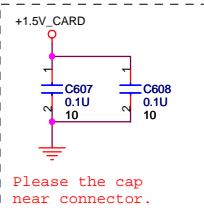
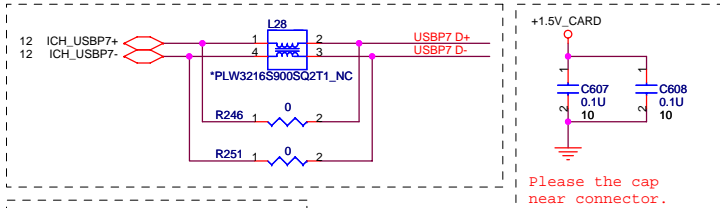
Circuit area : As small as possible.



*TPAOP/TPAON, TPBP0P/TPBON pair trace : As close as possible.
 *TPAOP/TPAON, TPBP0P/TPBON pair trace : Same length electrically.
 *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

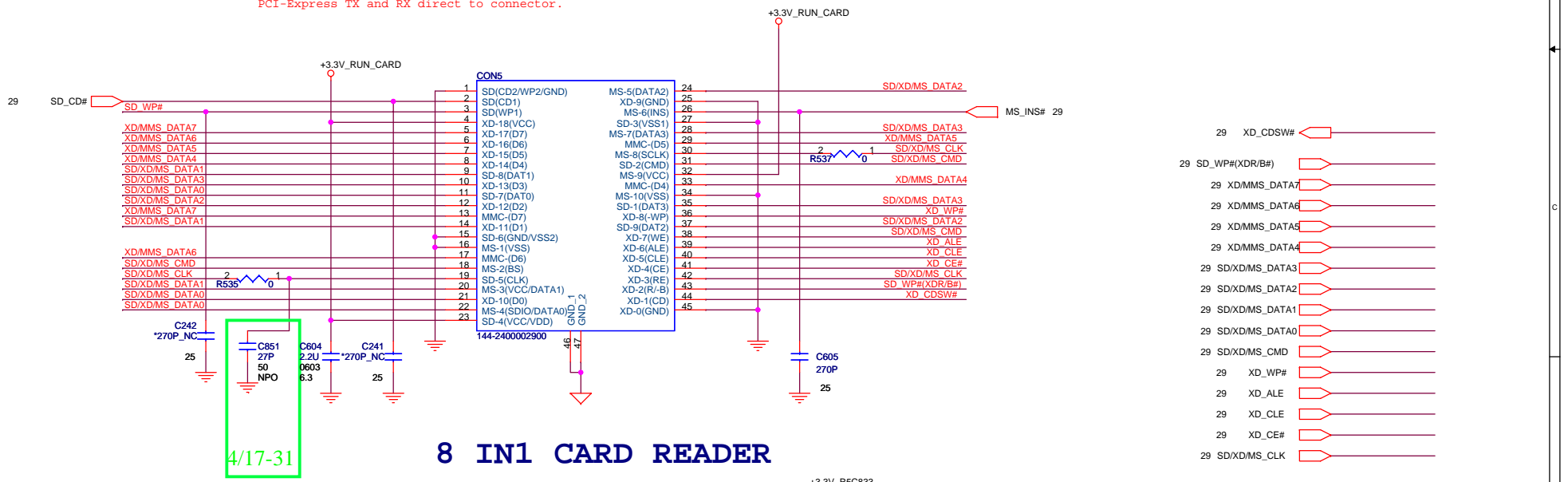
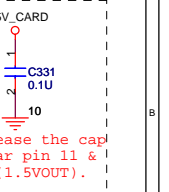
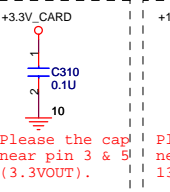
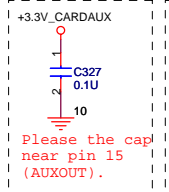
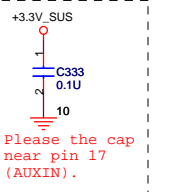
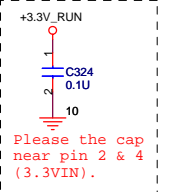
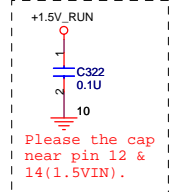
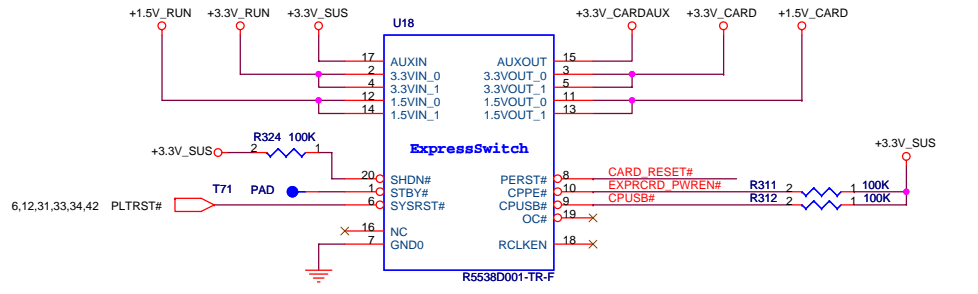


Express Card

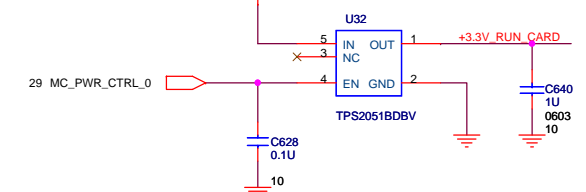
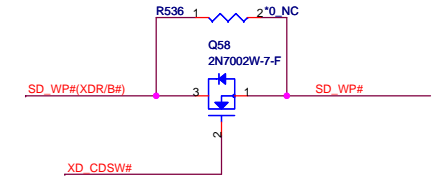
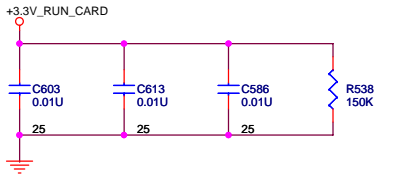


JAE PX10FS16PH-26P
PCI-Express TX and RX direct to connector.

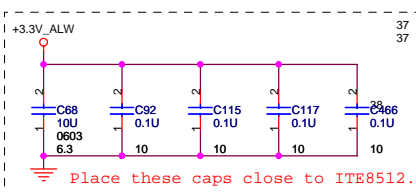
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



8 IN1 CARD READER



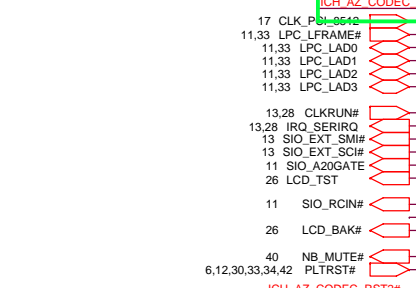
Title: ExpressCard/SmartCard		
Size: FM7B	Document Number: FM7B	Rev: 1A
Date: Monday, July 14, 2008	Sheet: 30	of 60



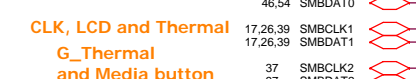
Place these caps close to ITE8512.



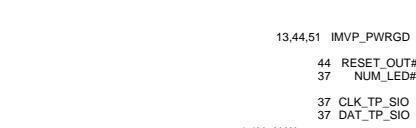
2/15-2



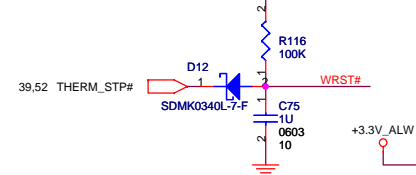
Charge and BAT



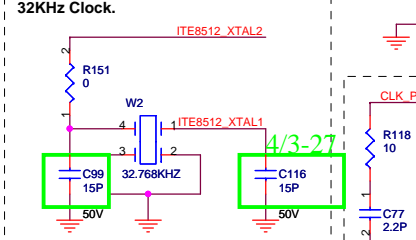
CLK, LCD and Thermal
G_Thermal
and Media button



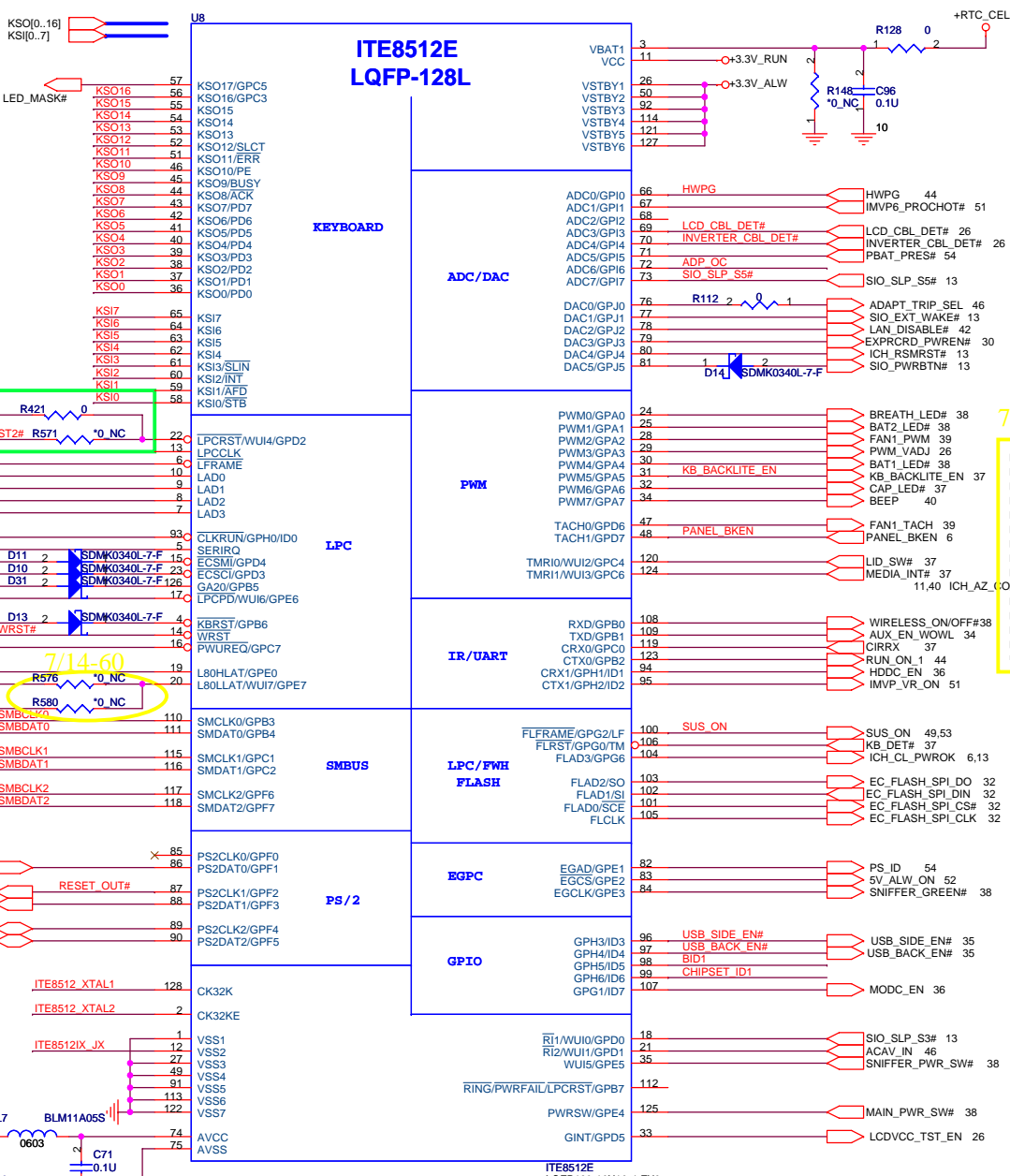
32KHz Clock.



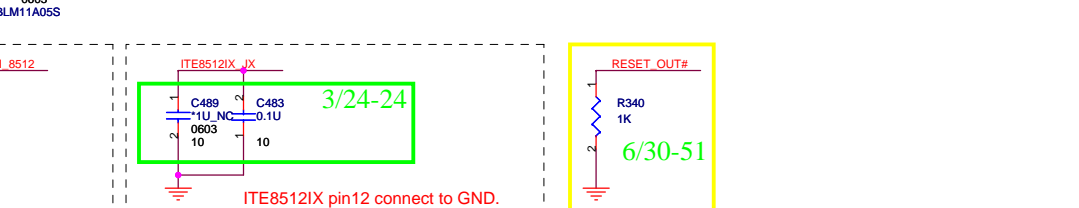
3/24-24



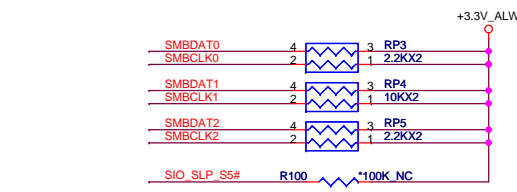
6/30-51



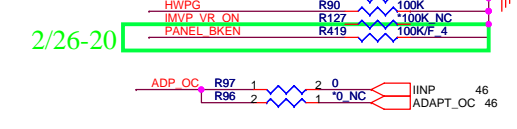
ITE8512E LQFP128-16X16-4-FX2



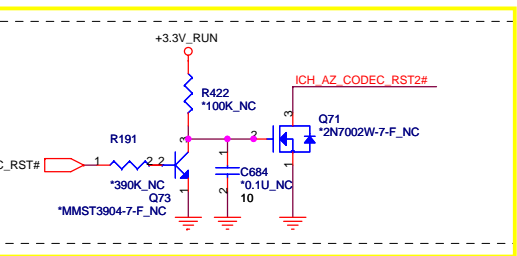
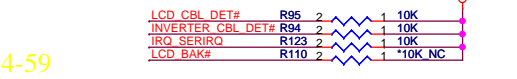
ITE8512IX pin12 connect to GND.
ITE8512JX pin12 connect to 0.1uF, 1uF.



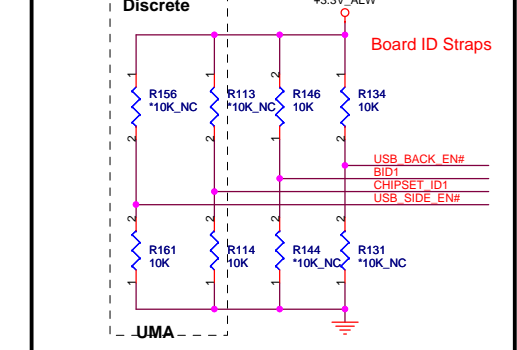
2/26-20



7/14-59



UMA



VGA_IDENTIFY

USB_SIDE_EN#
1 = Discrete Gfx.
0 = UMA.

CHIPSET_ID1	BID1	USB_BACK_EN#	FM7B(UMA)	FM7(Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

QUANTA COMPUTER

Title: Ultra I/O Controller ECE5028

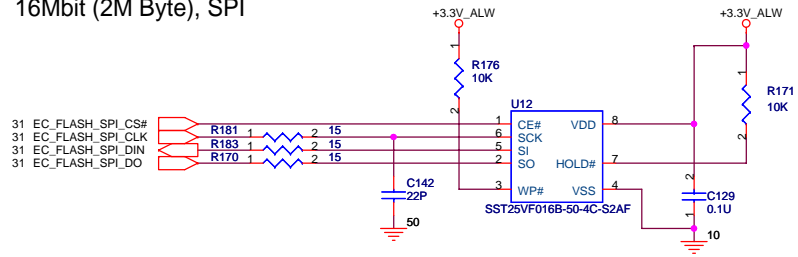
Size: Document Number FM7B

Date: Wednesday, July 16, 2008

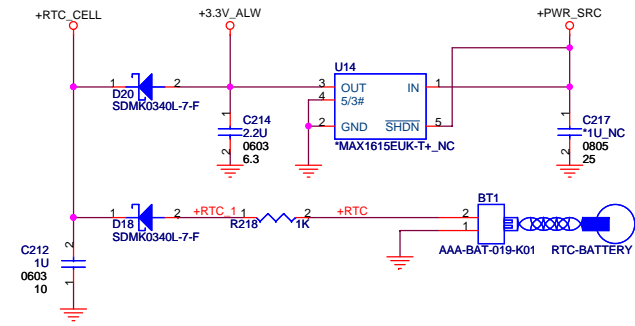
Sheet: 31 of 60

Rev: 1A

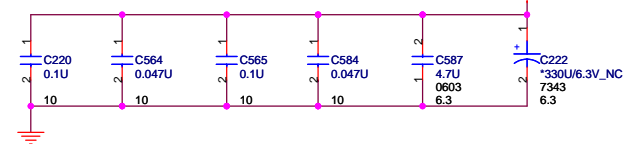
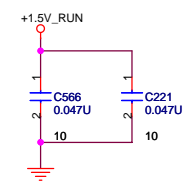
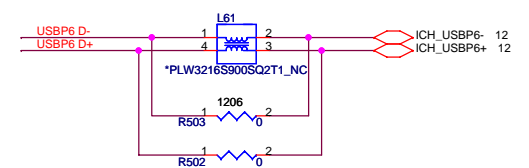
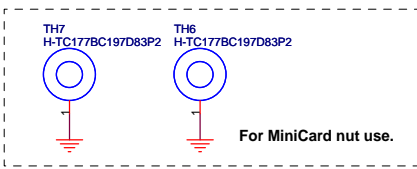
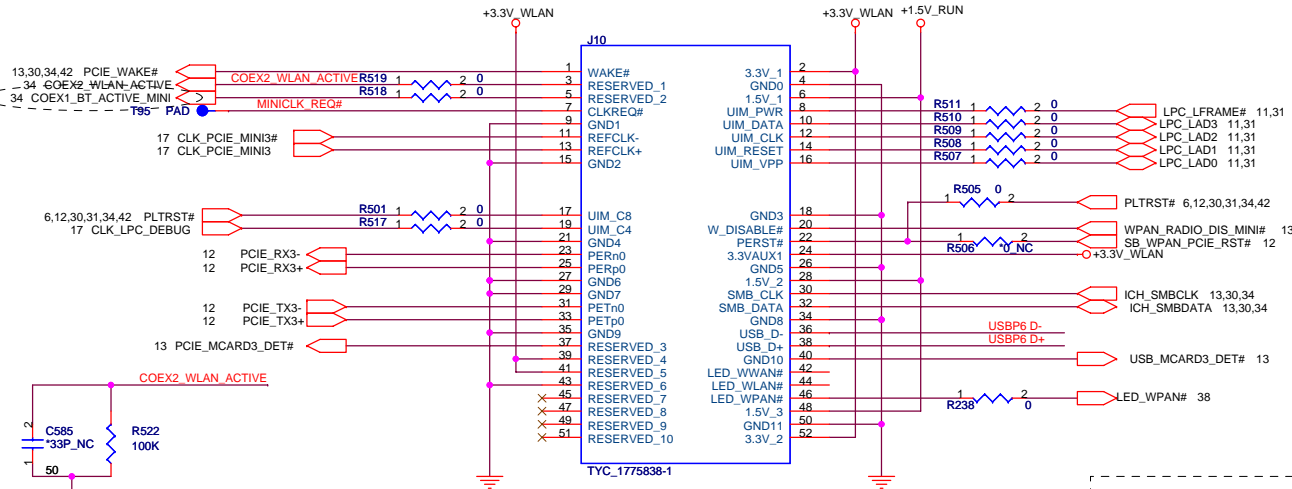
16Mbit (2M Byte), SPI



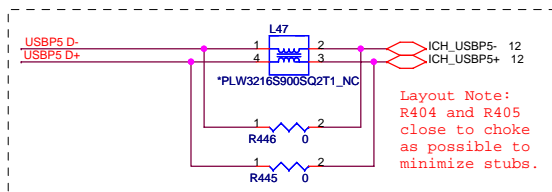
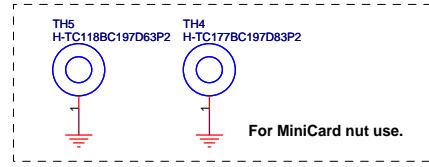
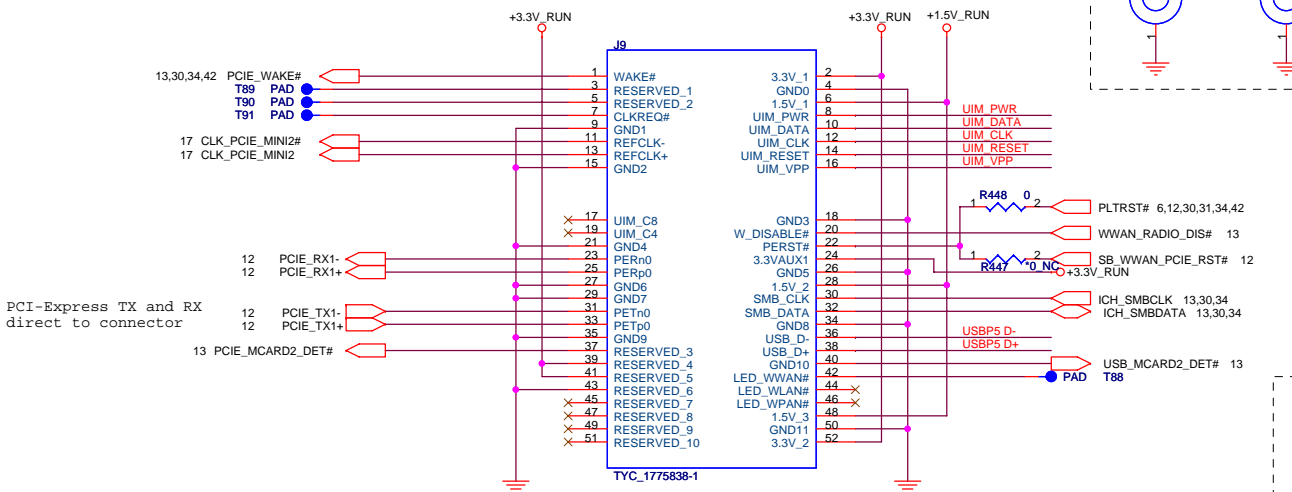
RTC BATTERY



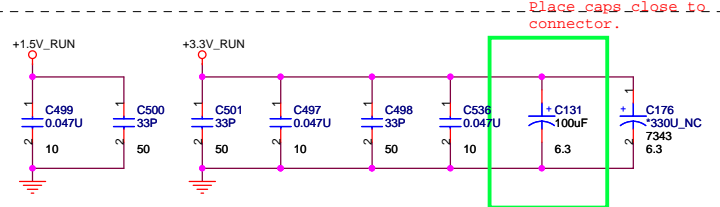
MiniCard Robson, BT. UWB connector



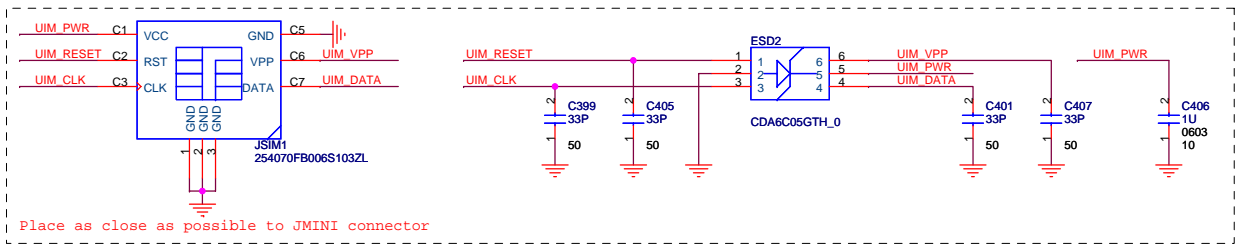
MiniCard WWAN connector



Layout Note:
R404 and R405
close to choke
as possible to
minimize stubs.



Place caps close to connector.

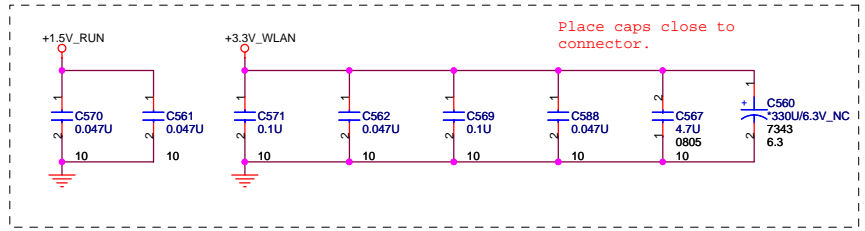
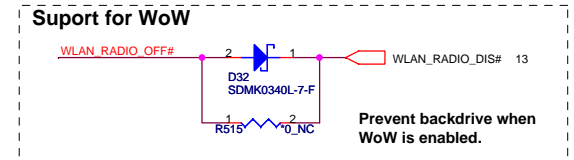
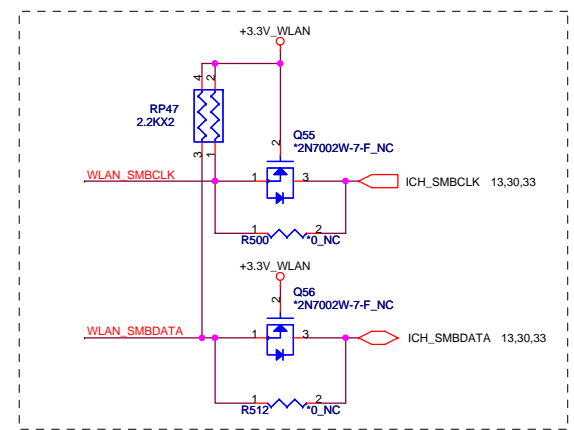
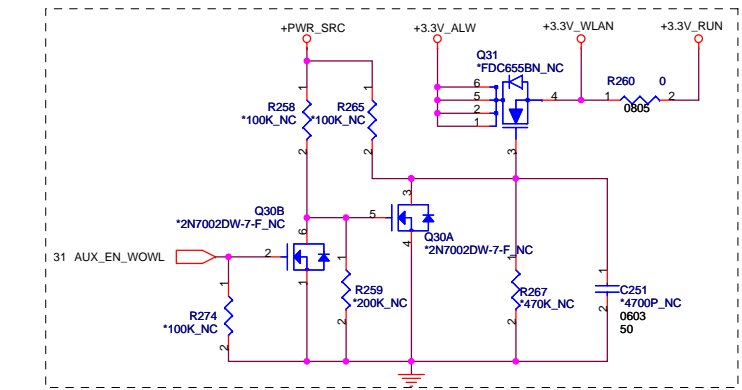
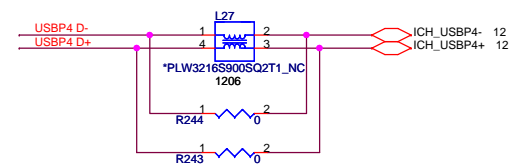
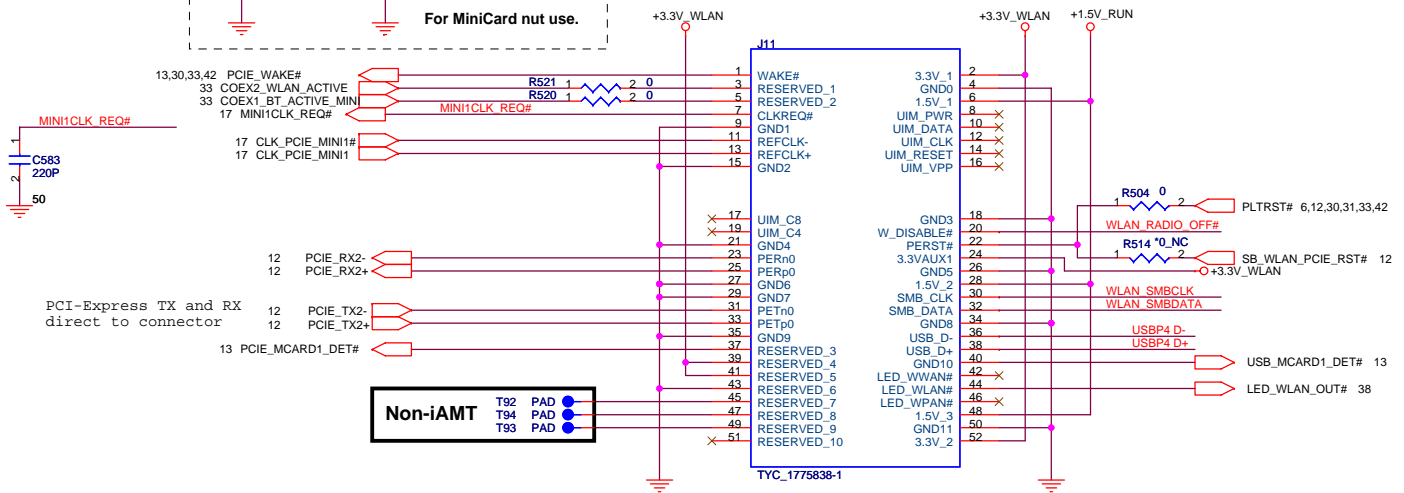
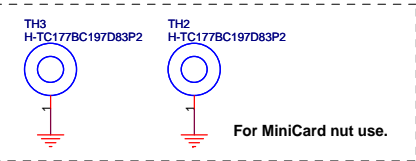


Place as close as possible to JMINI connector

**QUANTA
COMPUTER**

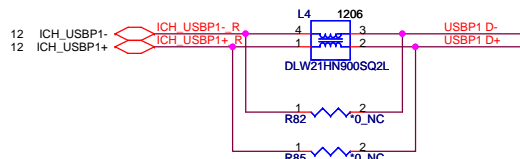
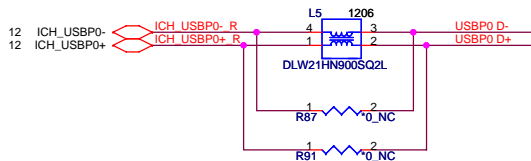
Title: MINI-PCI		
Size: FM7B	Document Number: FM7B	Rev: 1A
Date: Monday, June 30, 2008	Sheet: 33	of: 60

MiniCard WLAN connector



External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

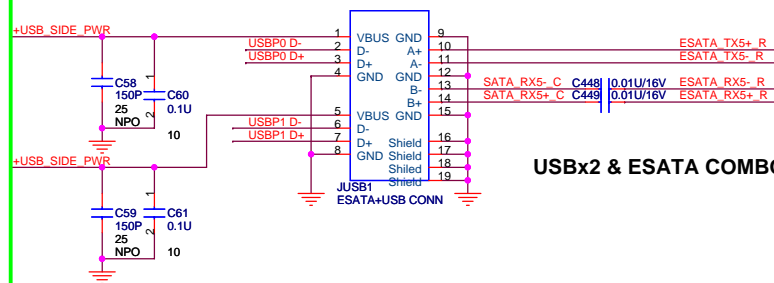
2/22-14
4/17-31



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Side External USBX2

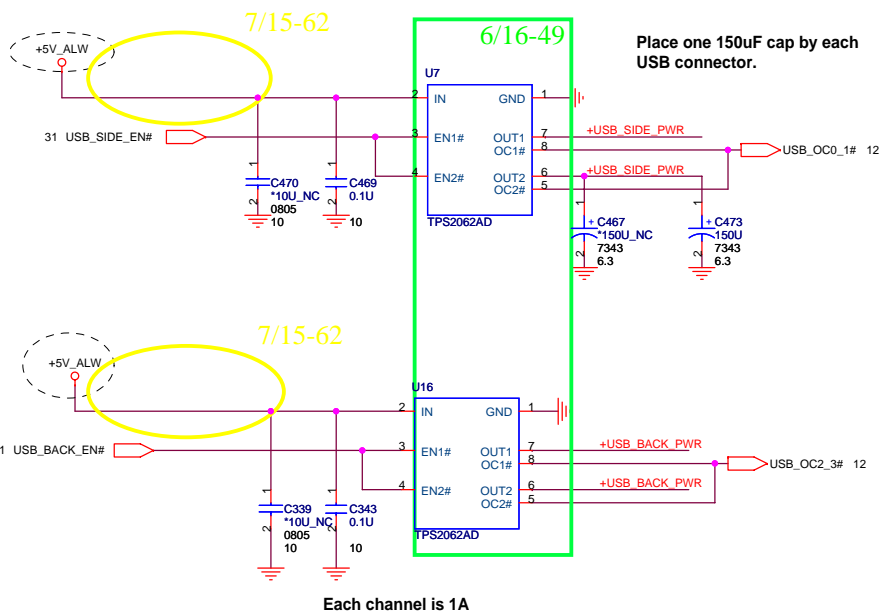
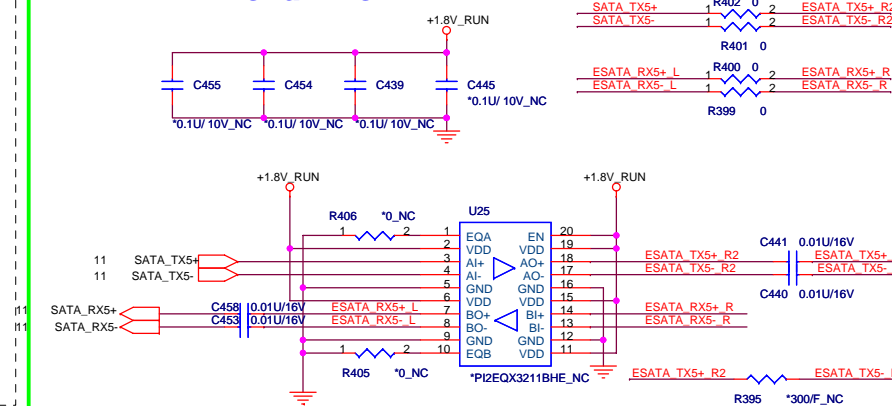
2/15-1



USBx2 & ESATA COMBO

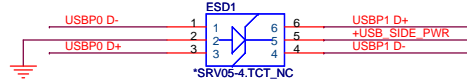
2/20-11
5/29-41

E-SATA Re-driver

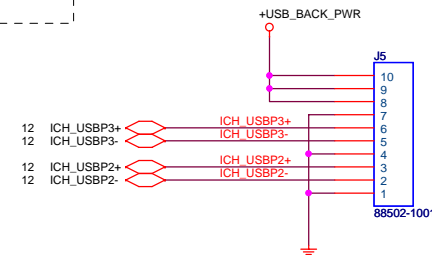


Each channel is 1A

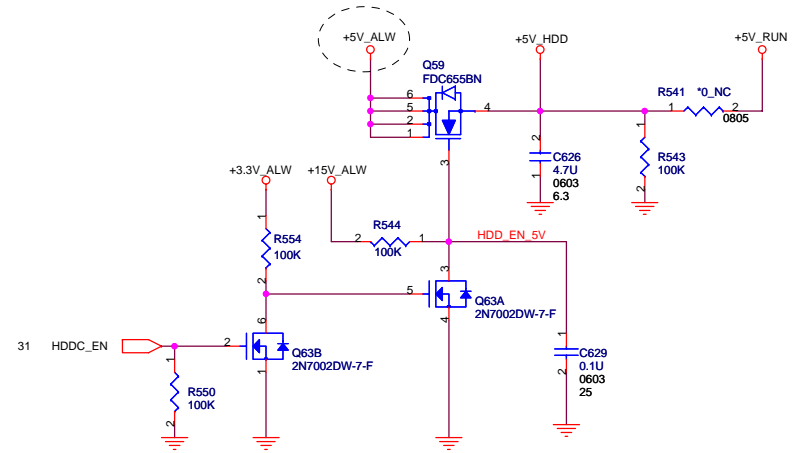
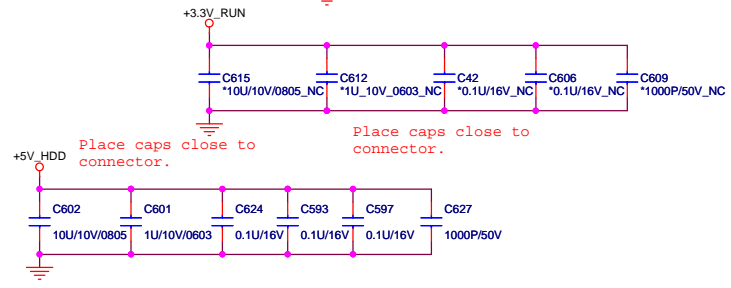
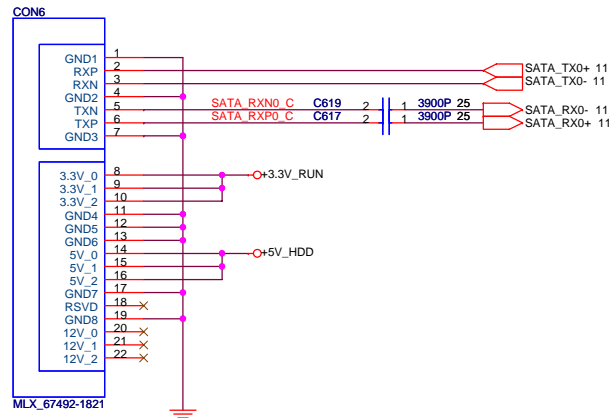
Place ESD diodes as close as possible to USB connector.



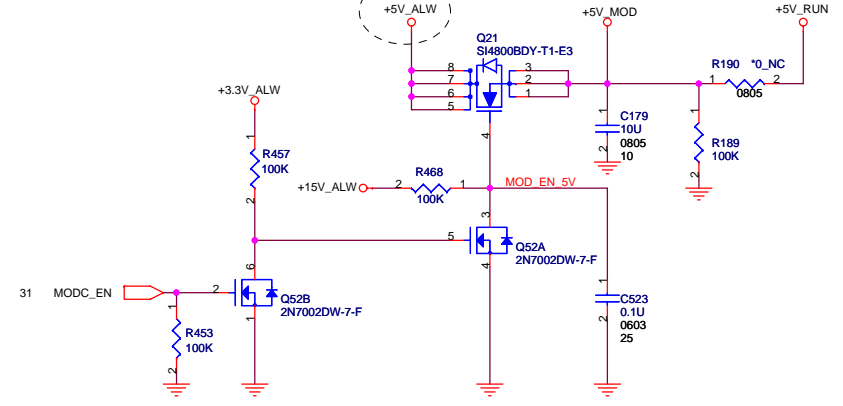
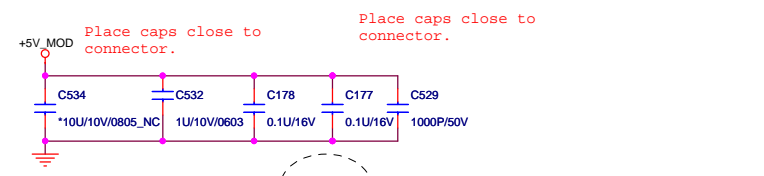
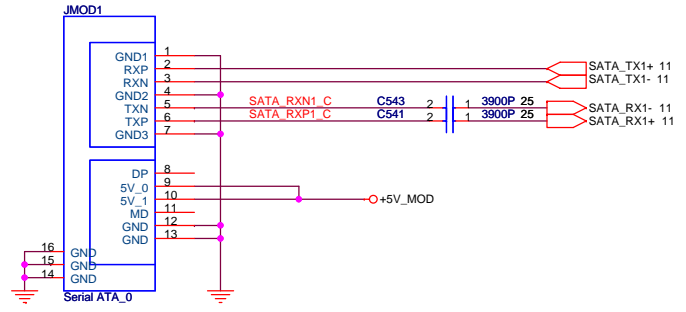
MB side



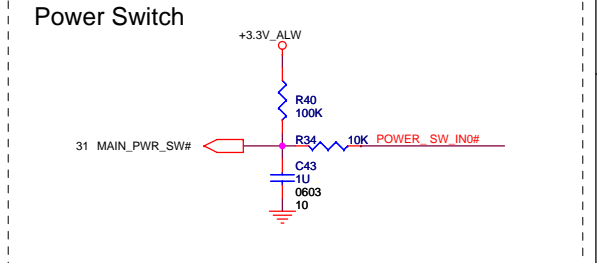
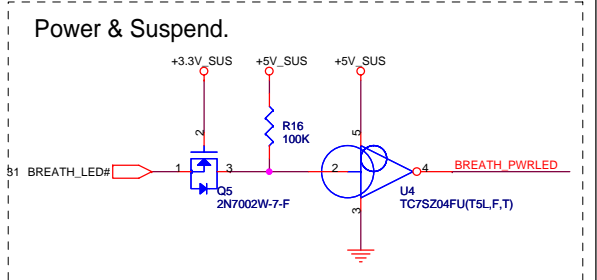
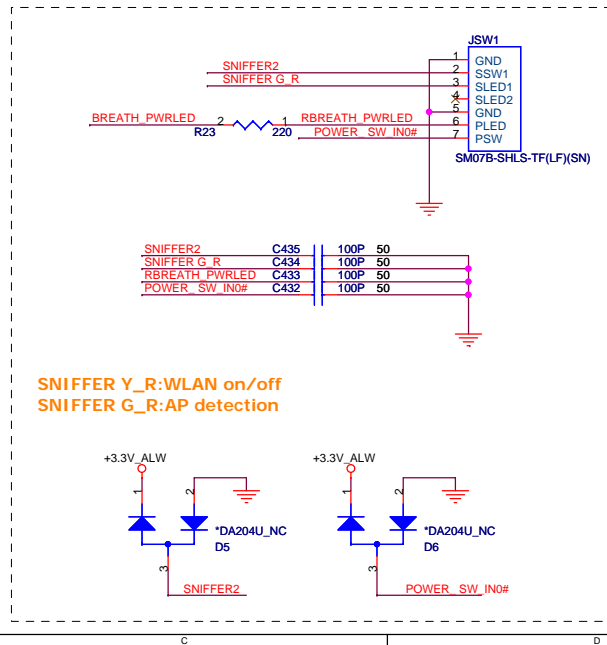
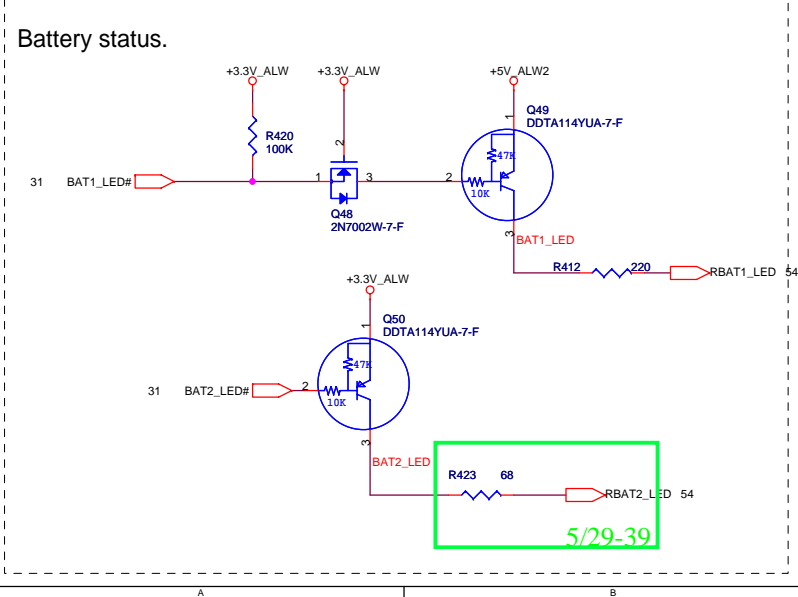
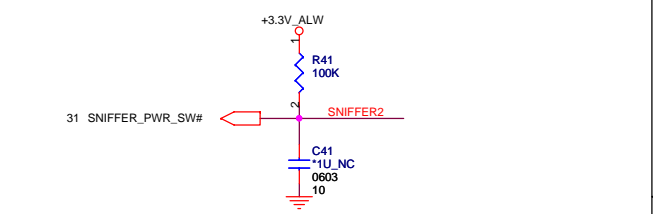
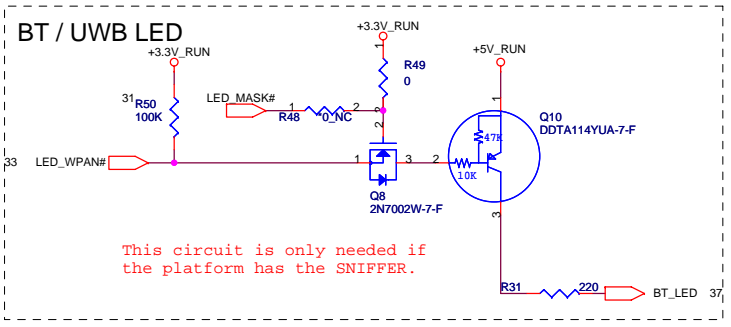
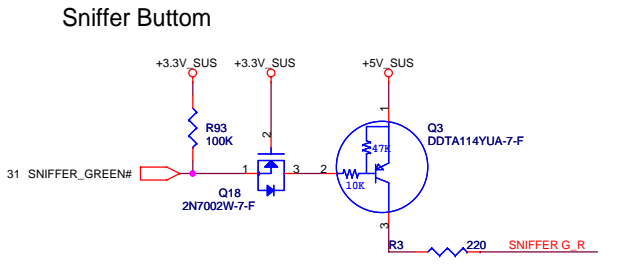
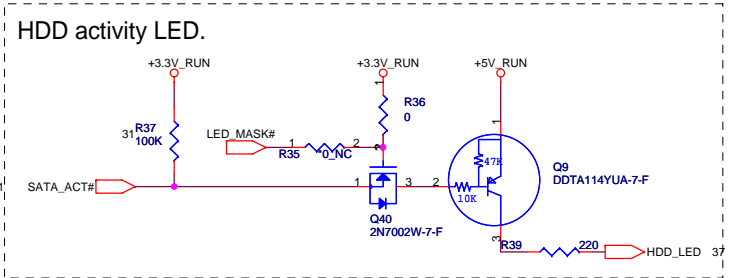
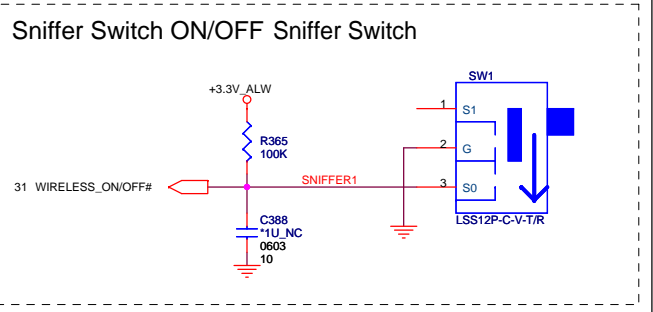
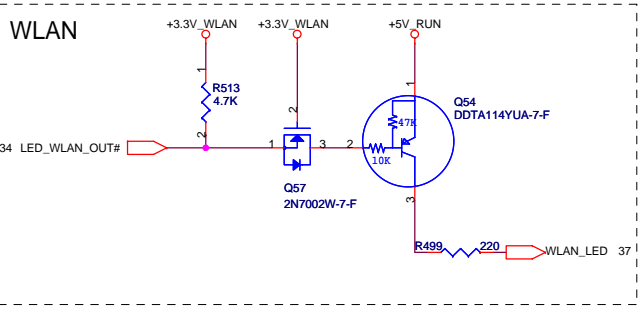
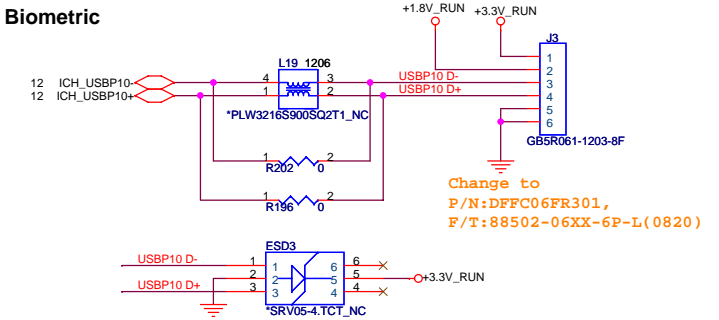
SATA Connector.



ODD Connector



Title		
SATA (HDD&CD_ROM)		
Size	Document Number	Rev
	FM7B	1A
Date:	Monday, July 14, 2008	Sheet 36 of 60

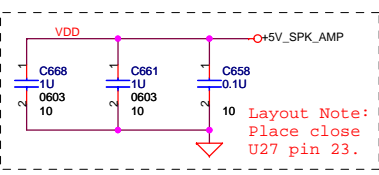
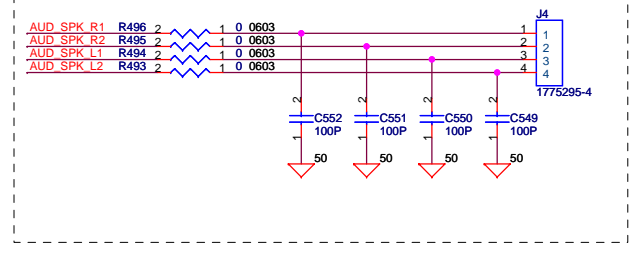
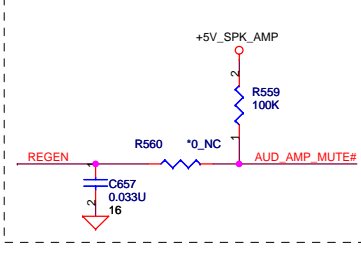
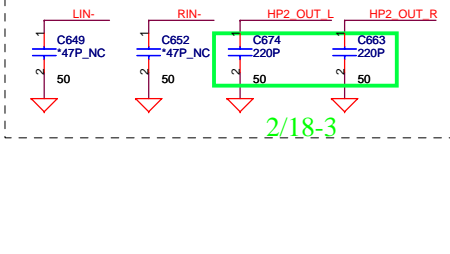
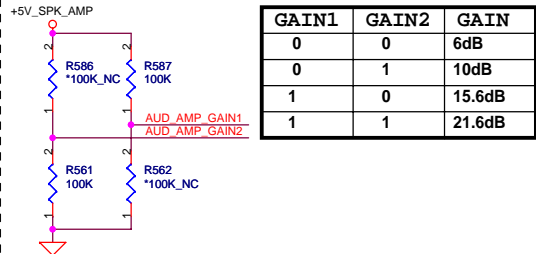


QUANTA COMPUTER

Title: SWITCH, KEYBOARD & LED

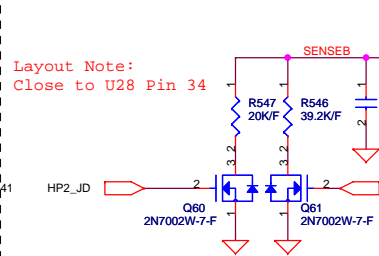
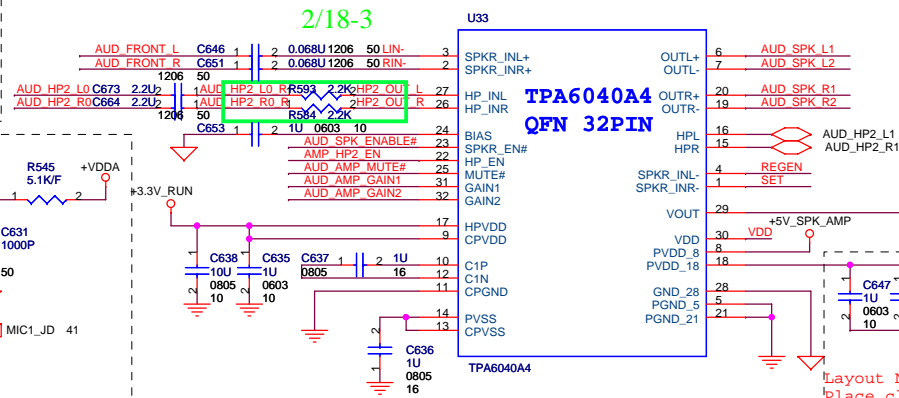
Size: Document Number FM7B Rev 1A

Date: Monday, June 30, 2008 Sheet 38 of 60

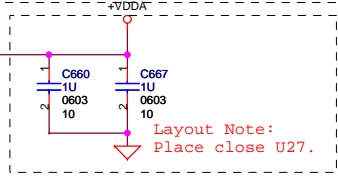
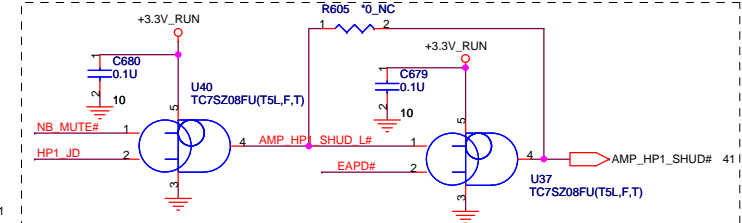


Layout Note:
Place close
U27 pin 23.

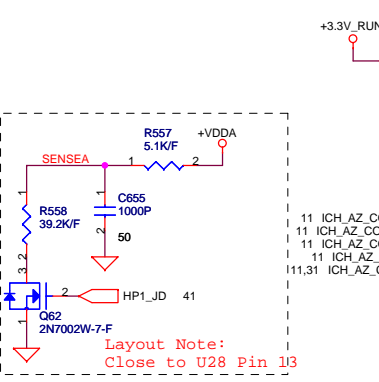
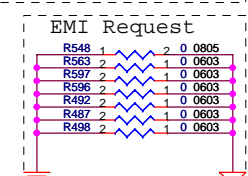
INTERNAL SPEAKER AMP



Layout Note:
Close to U28 Pin 34

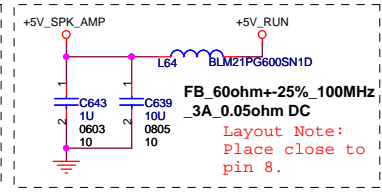
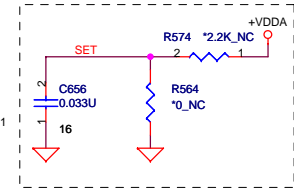
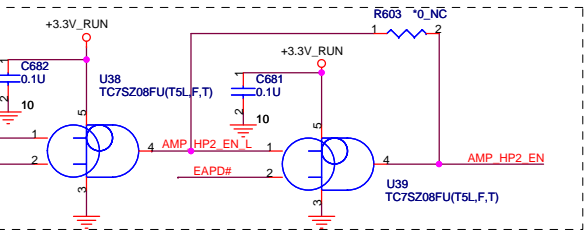
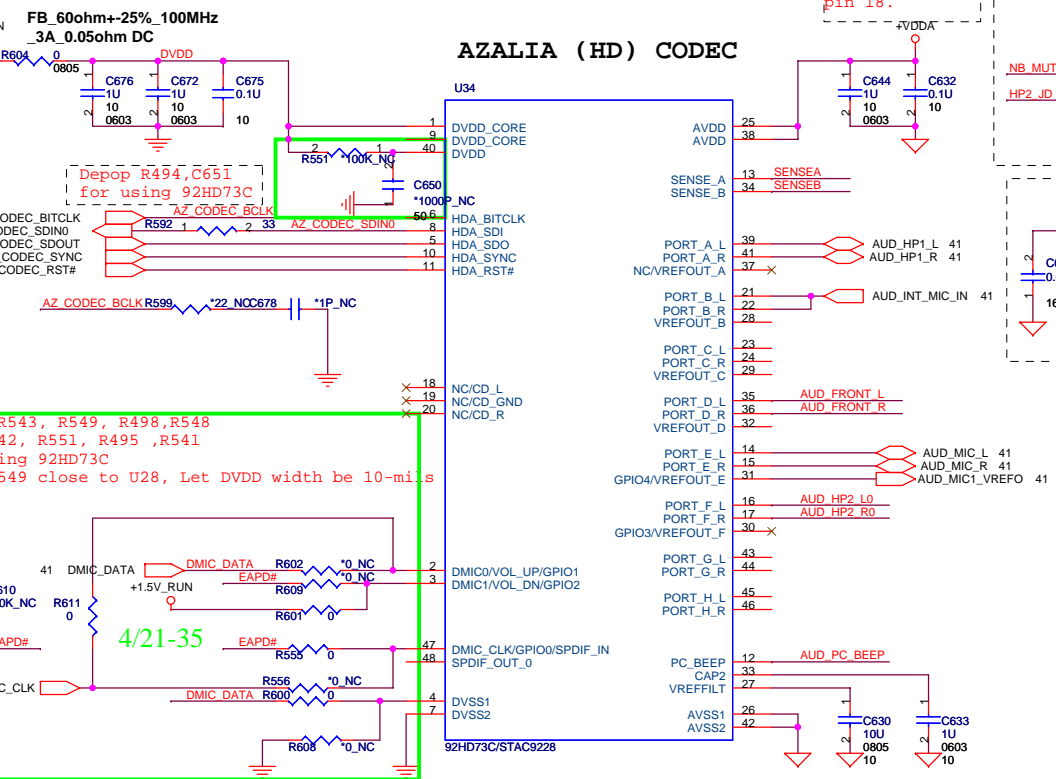


Layout Note:
Place close U27.

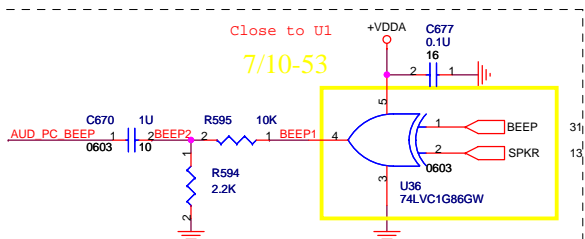


Layout Note:
Close to U28 Pin U3

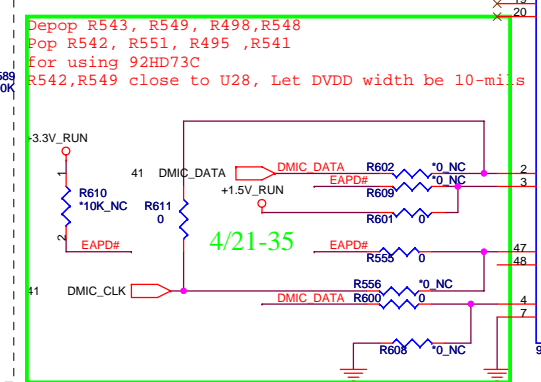
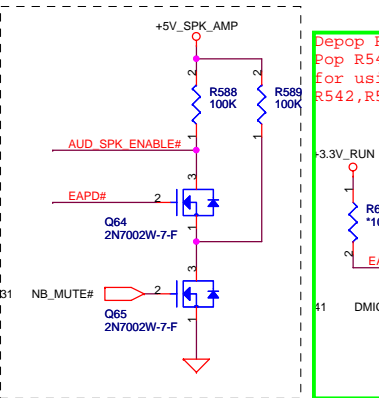
AZALIA (HD) CODEC



Layout Note:
Place close to
pin 8.



Close to U1
7/10-53

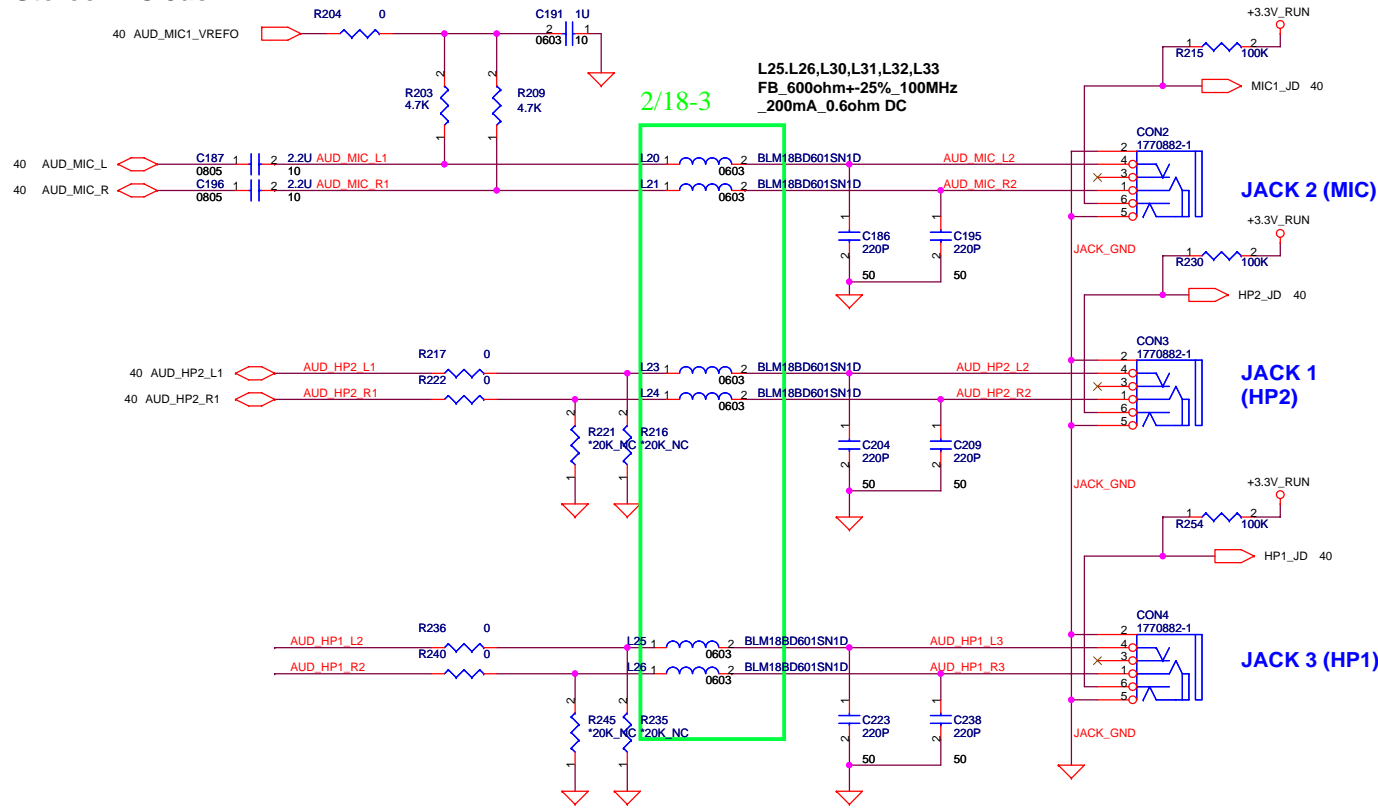


4/21-35

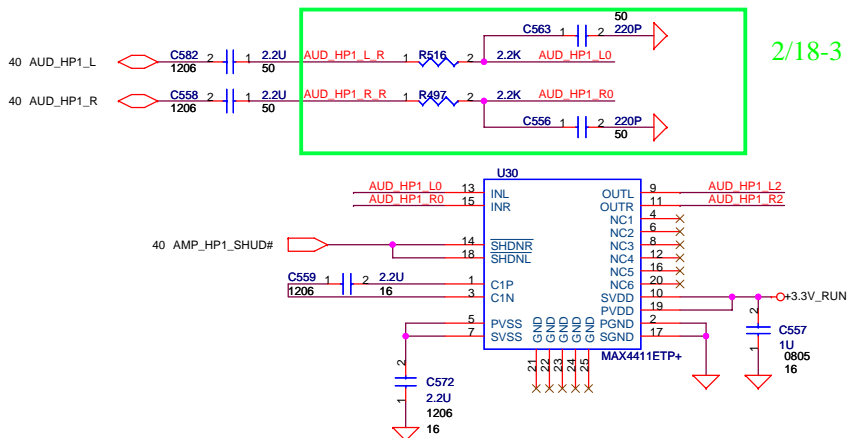
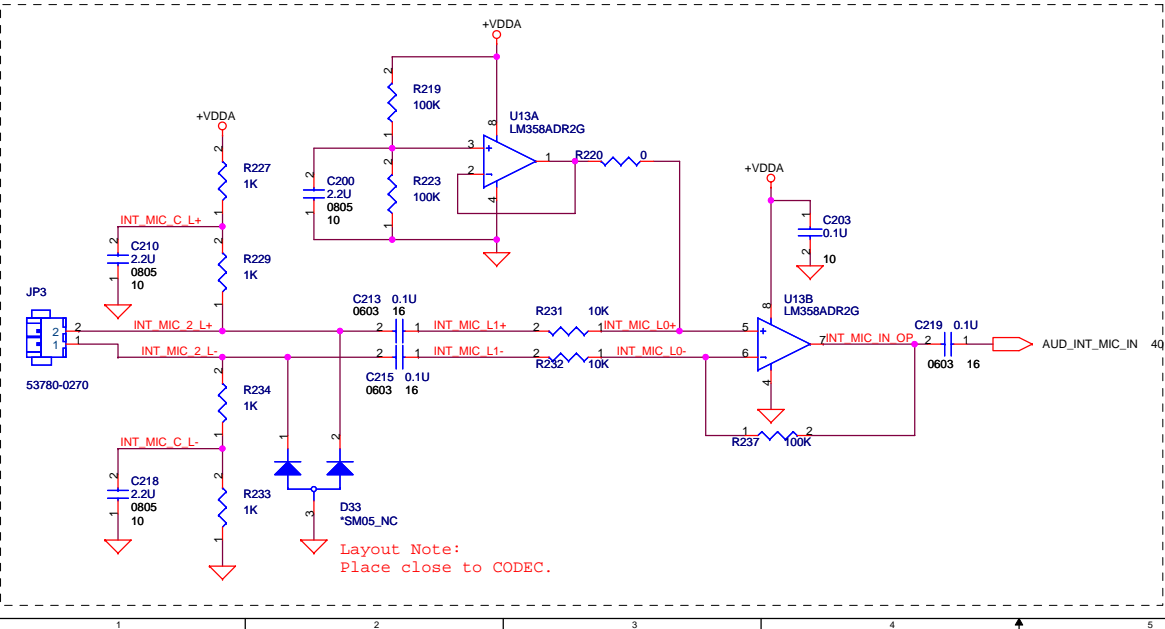
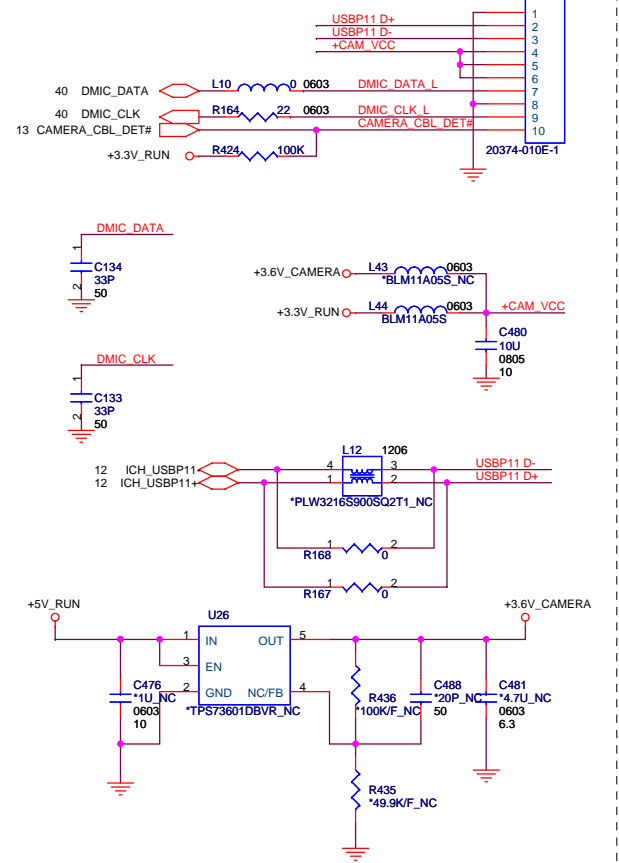
**QUANTA
COMPUTER**

Title: Azelia CODEC
 Size: Document Number FM7B
 Date: Thursday, July 10, 2008 Sheet 40 of 60 Rev 1A

Headphone Jack Stereo MIC Jack

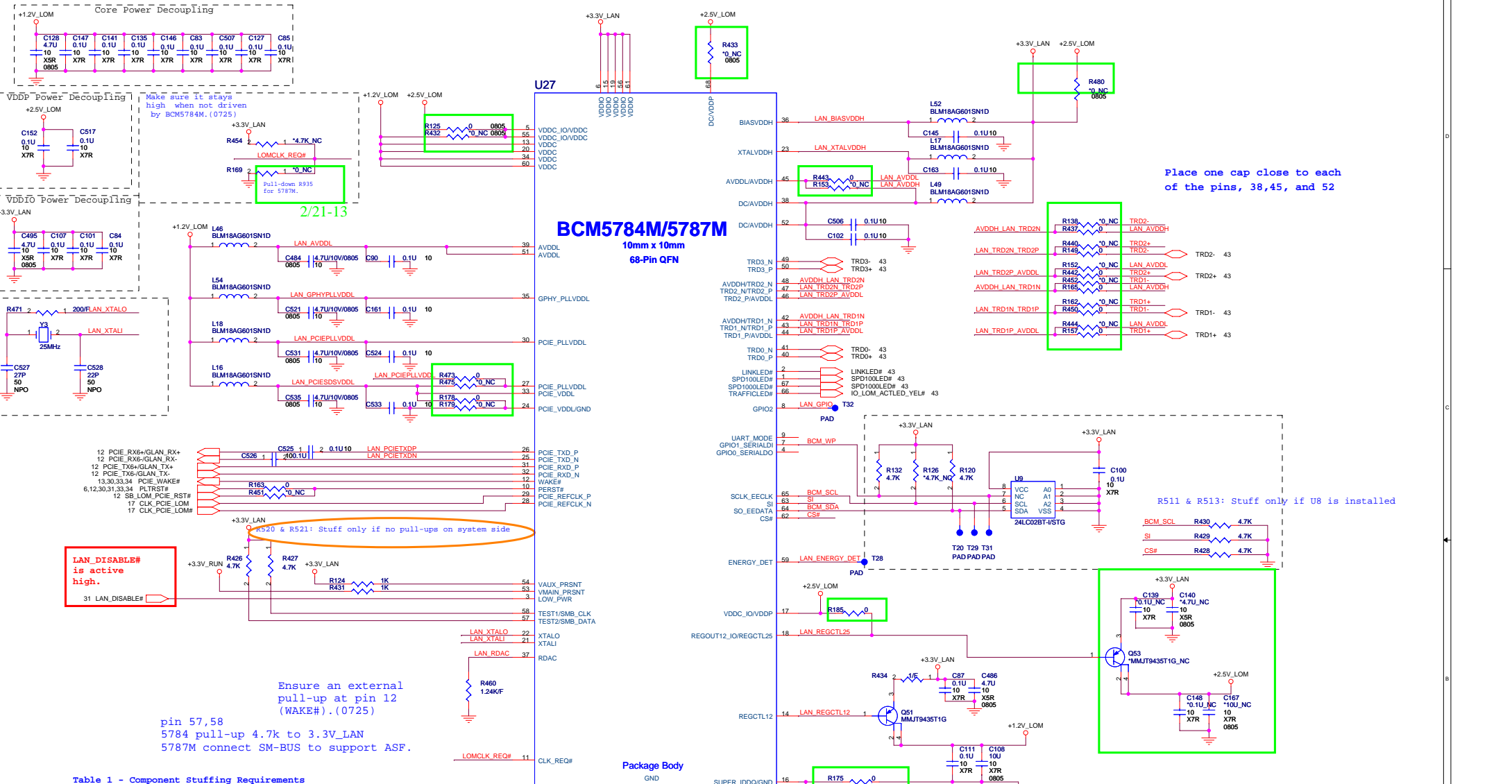


Array Microphone & Camera



**QUANTA
COMPUTER**

Title: AUDIO CONN
Size: Document Number FM7B Rev 1A
Date: Thursday, July 10, 2008 Sheet 41 of 60



BCM5784M/5787M
10mm x 10mm
68-Pin QFN

Place one cap close to each of the pins, 38,45, and 52

R511 & R513: Stuff only if U8 is installed

Ensure an external pull-up at pin 12 (WAKE#). (0725)

pin 57, 58
5784 pull-up 4.7k to 3.3V_LAN
5787M connect SM-BUS to support ASF.

Table 1 - Component Stuffing Requirements

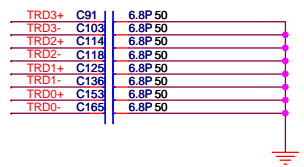
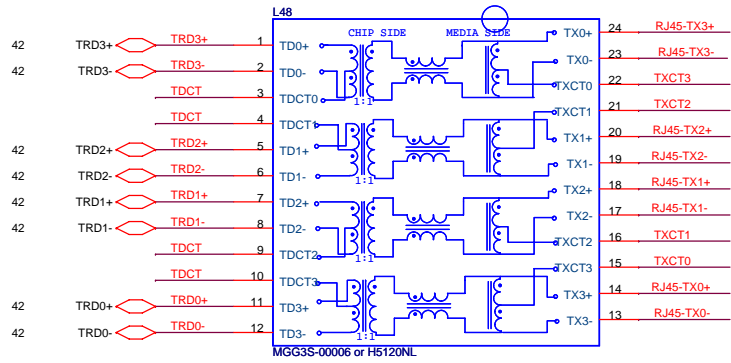
	INSTALL	NOT INSTALL
5787M	R391, R392, R428, R160, Q49, C162, C163, C179, C191, R132, R397, R139, R411, R149, R403, R141, R433	R119, R425, R159, R171, R394, R136, R401, R151, R409, R143, R402, R177
5784	R119, R425, R159, R171, R394, R136, R401, R151, R409, R143, R402, R177	R391, R392, R428, R160, Q49, C162, C163, C179, C191, R132, R397, R139, R411, R149, R403, R141, R433

	5784M	5787M
R157	39k	0
R418	20k	*20k_NC

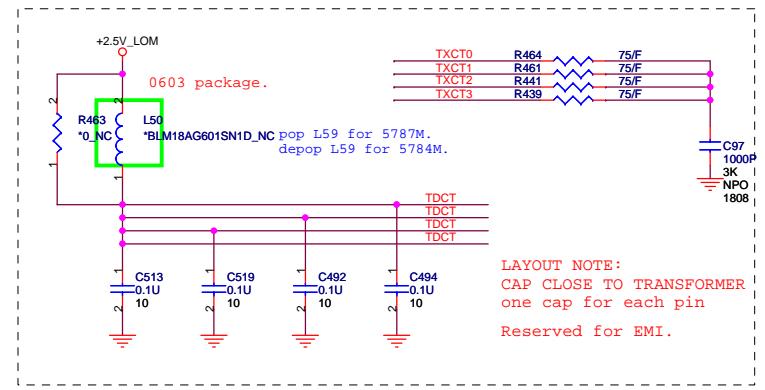
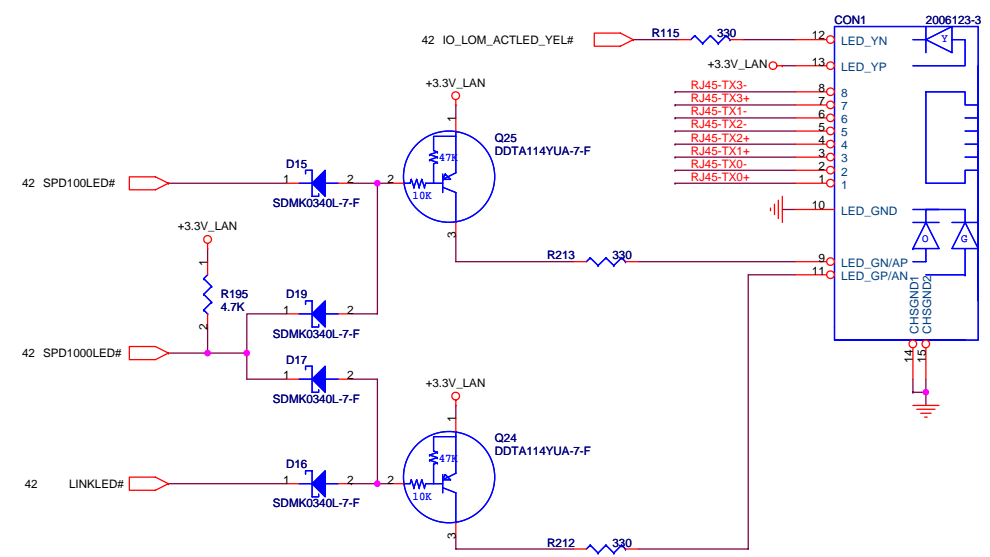
Note: thermal pad



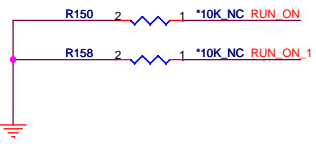
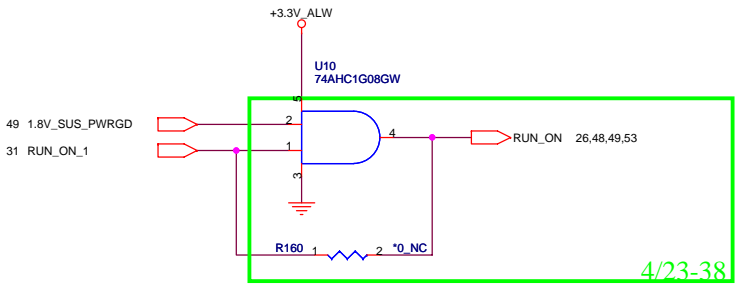
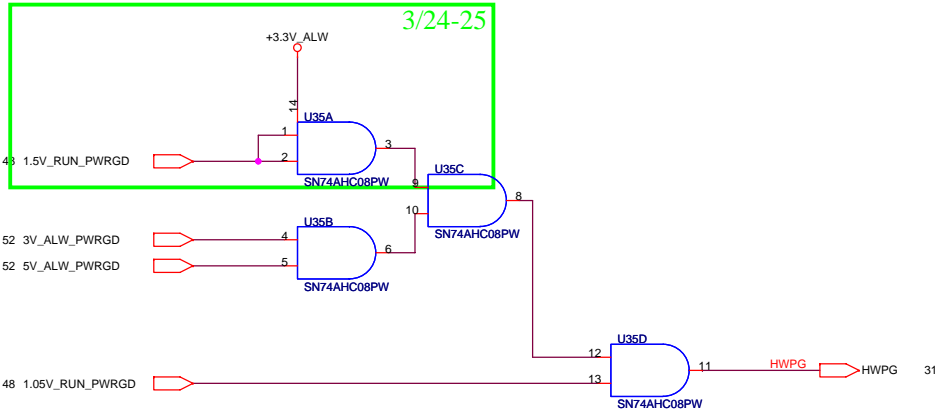
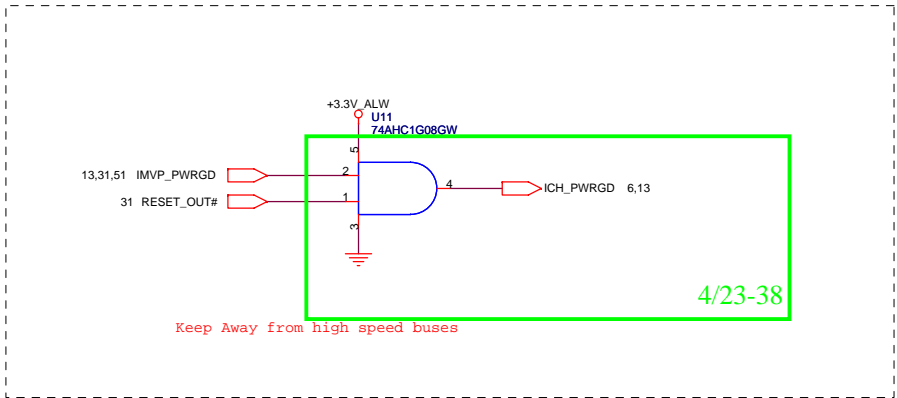
TRANSFORM TRANSFORM

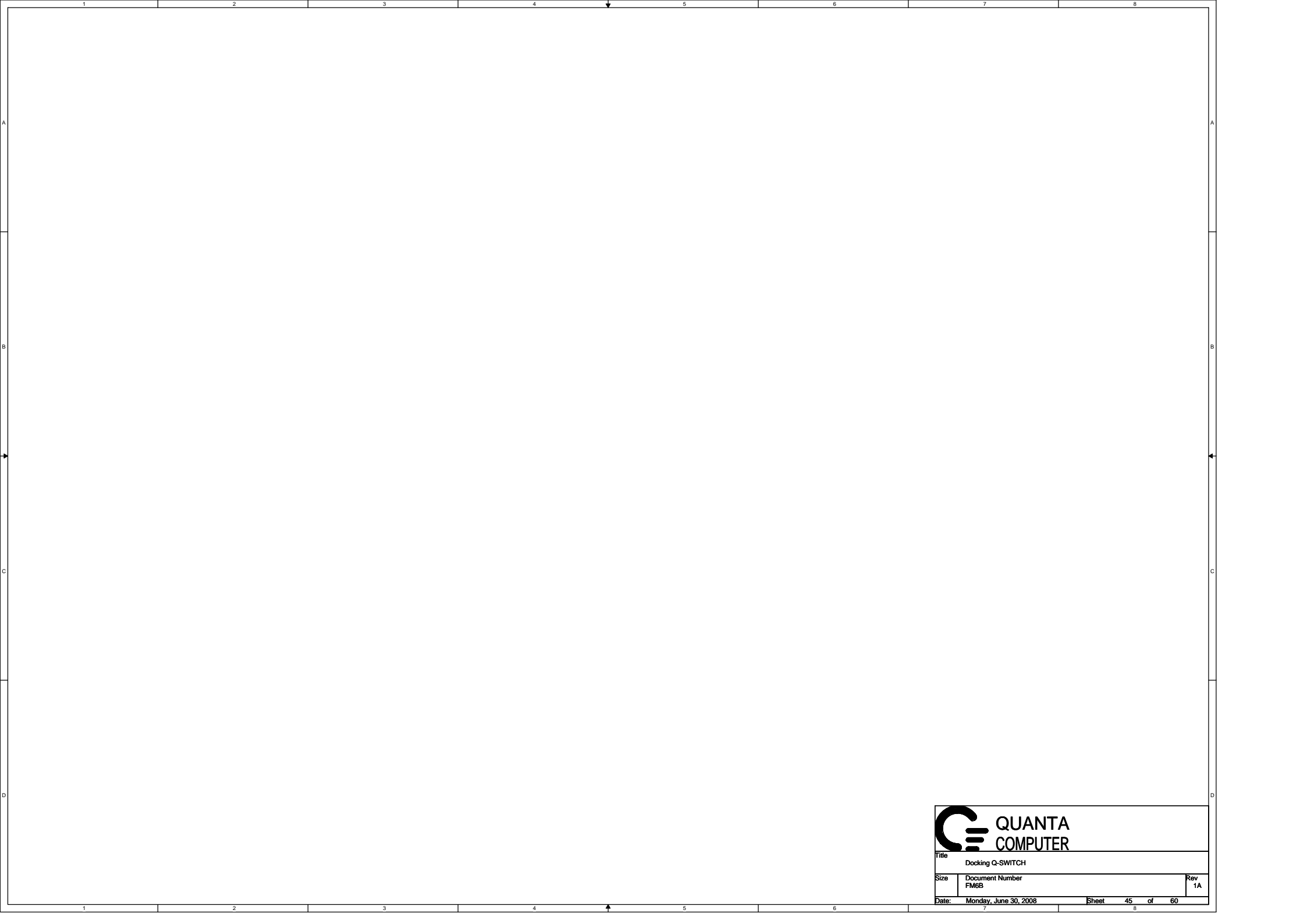


RJ-45 Connector



Title		
LAN SWITCH		
Size	Document Number	Rev
	FM7B	1A
Date:	Monday, June 30, 2008	Sheet 43 of 60





**QUANTA
COMPUTER**

Title		
Docking Q-SWITCH		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 45 of 60

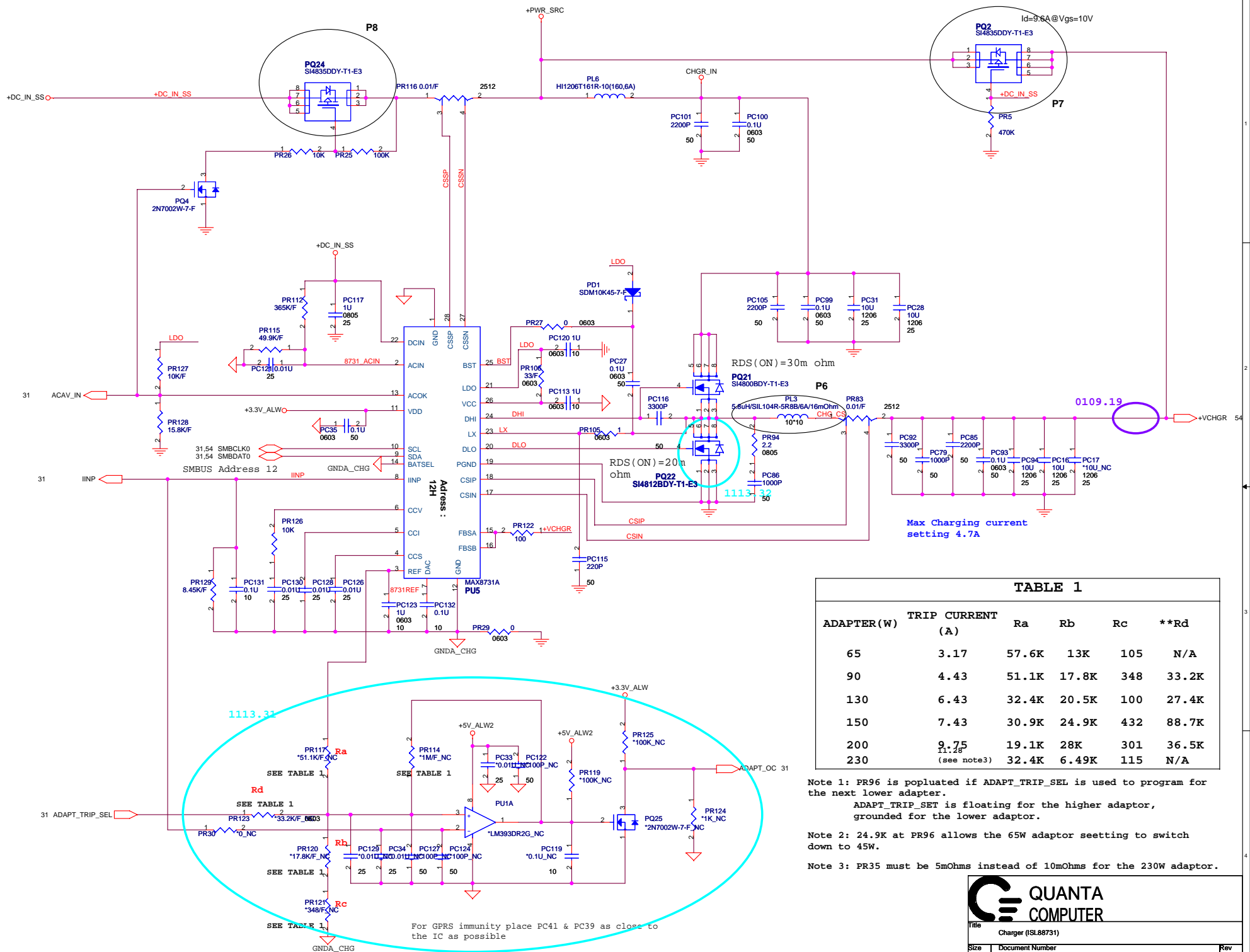


TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note 3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.
 ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.


QUANTA COMPUTER

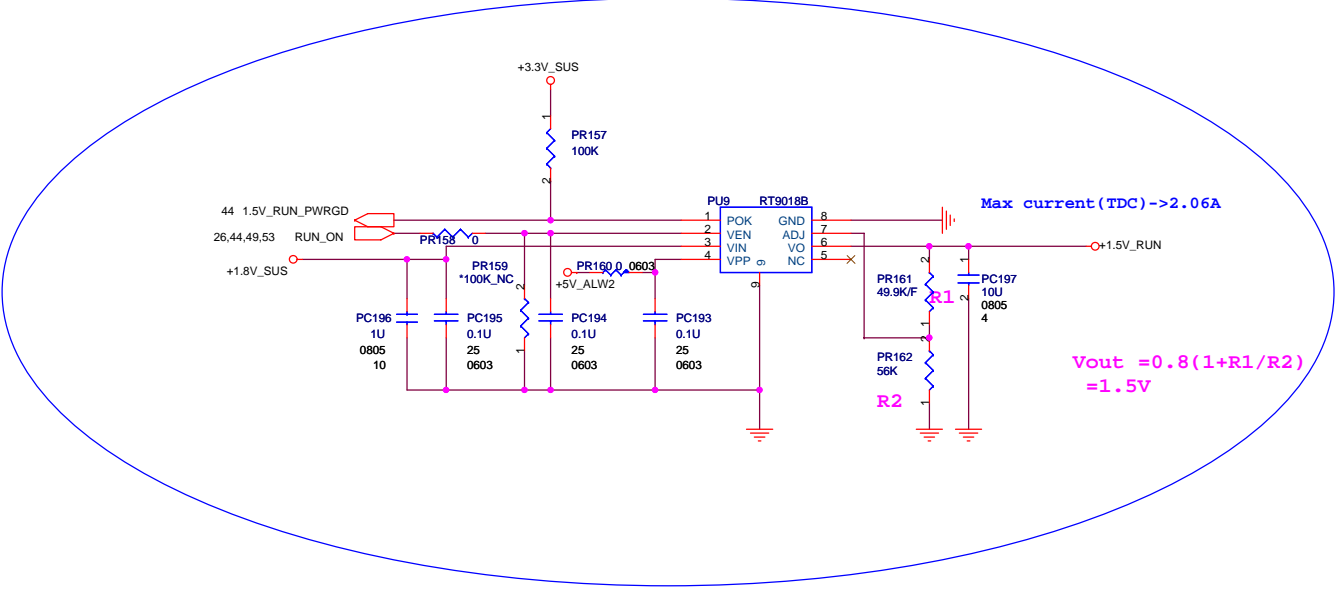
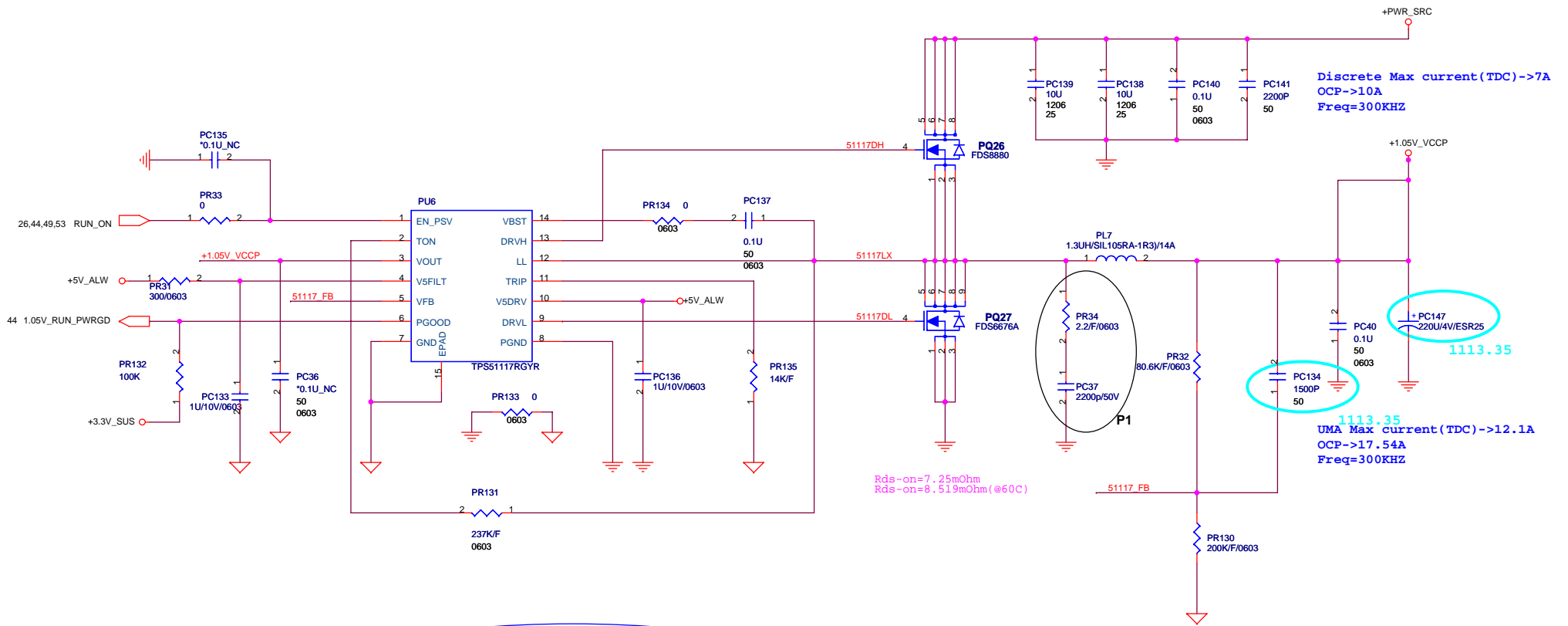
File: Charger (ISL8731)

Size: FMBB	Document Number: FMBB	Rev: 1A
Date: Monday, July 14, 2008	Sheet: 46	of 60

For GPRS immunity place PC41 & PC39 as close to the IC as possible

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number FM6B	Rev 1A
Date:	Monday, June 30, 2008	Sheet 47 of 60



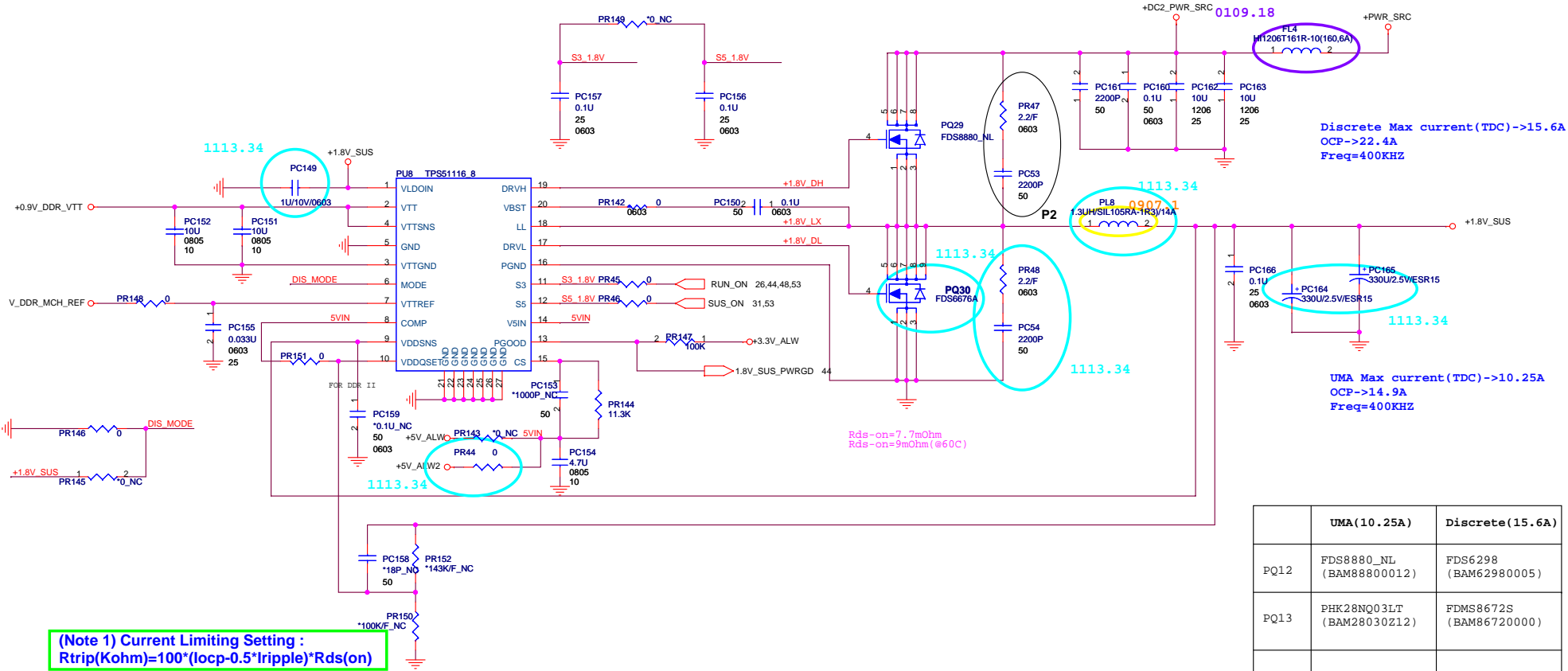
	UMA (12.1A)	Discrete (7A)
PQ22	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ25	FDS6676AS_NL (BAM66760026)	FDS6680AS (BAM66800061)
PL25	SIL105RA-1R5-R (CV-15F0M208)	SIL104R-1R5PF (DC-15A00010)
PR452		

QUANTA COMPUTER

Title: 1.05_VCCP & 1.5V_RUN

Size: Document Number FM6B Rev 1A


Date: Tuesday, July 15, 2008 Sheet 48 of 60

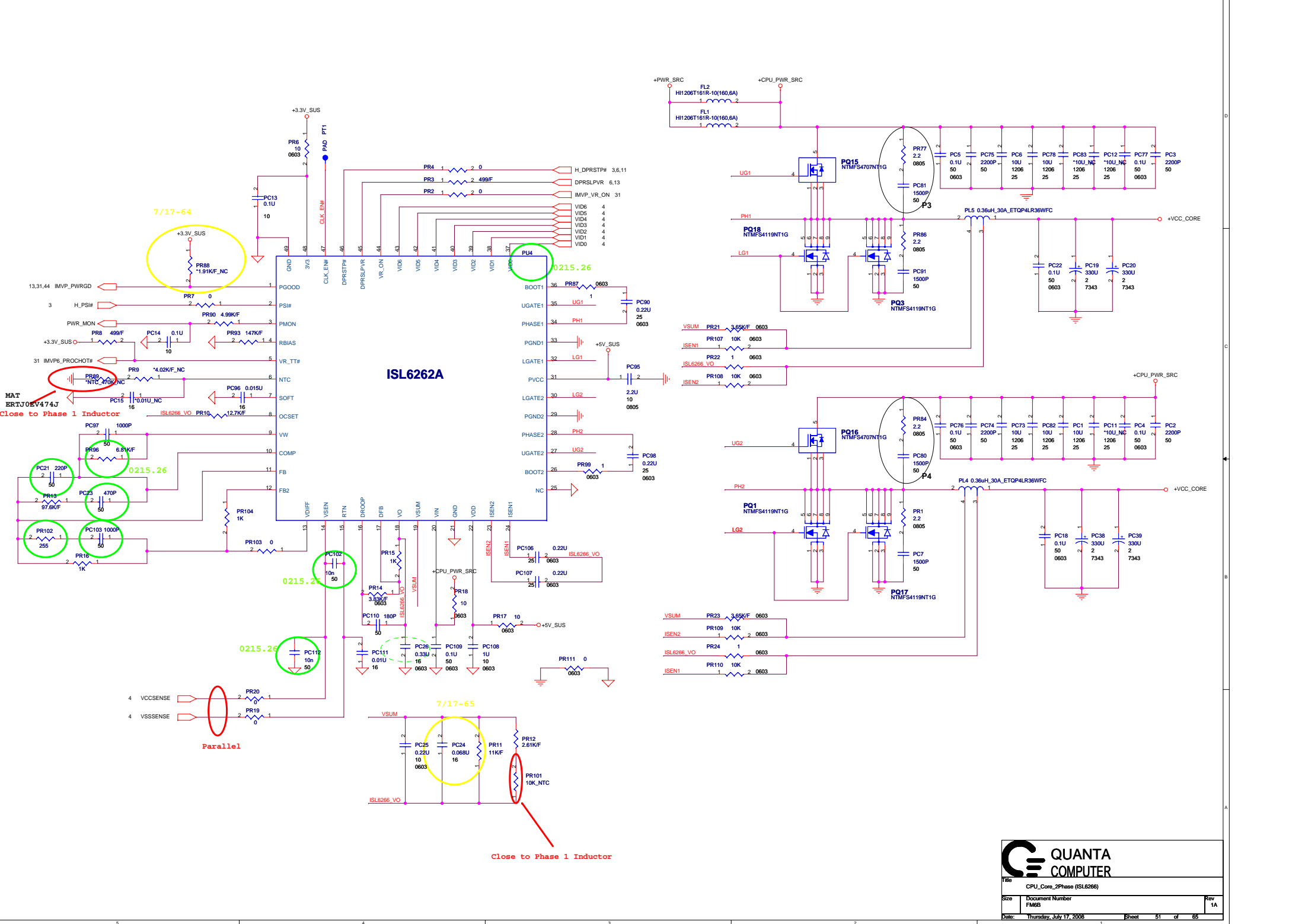


(Note 1) Current Limiting Setting :
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$

	UMA (10.25A)	Discrete (15.6A)
PQ12	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ13	PHK28NQ03LT (BAM28030212)	FDMS8672S (BAM86720000)
PR83		

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

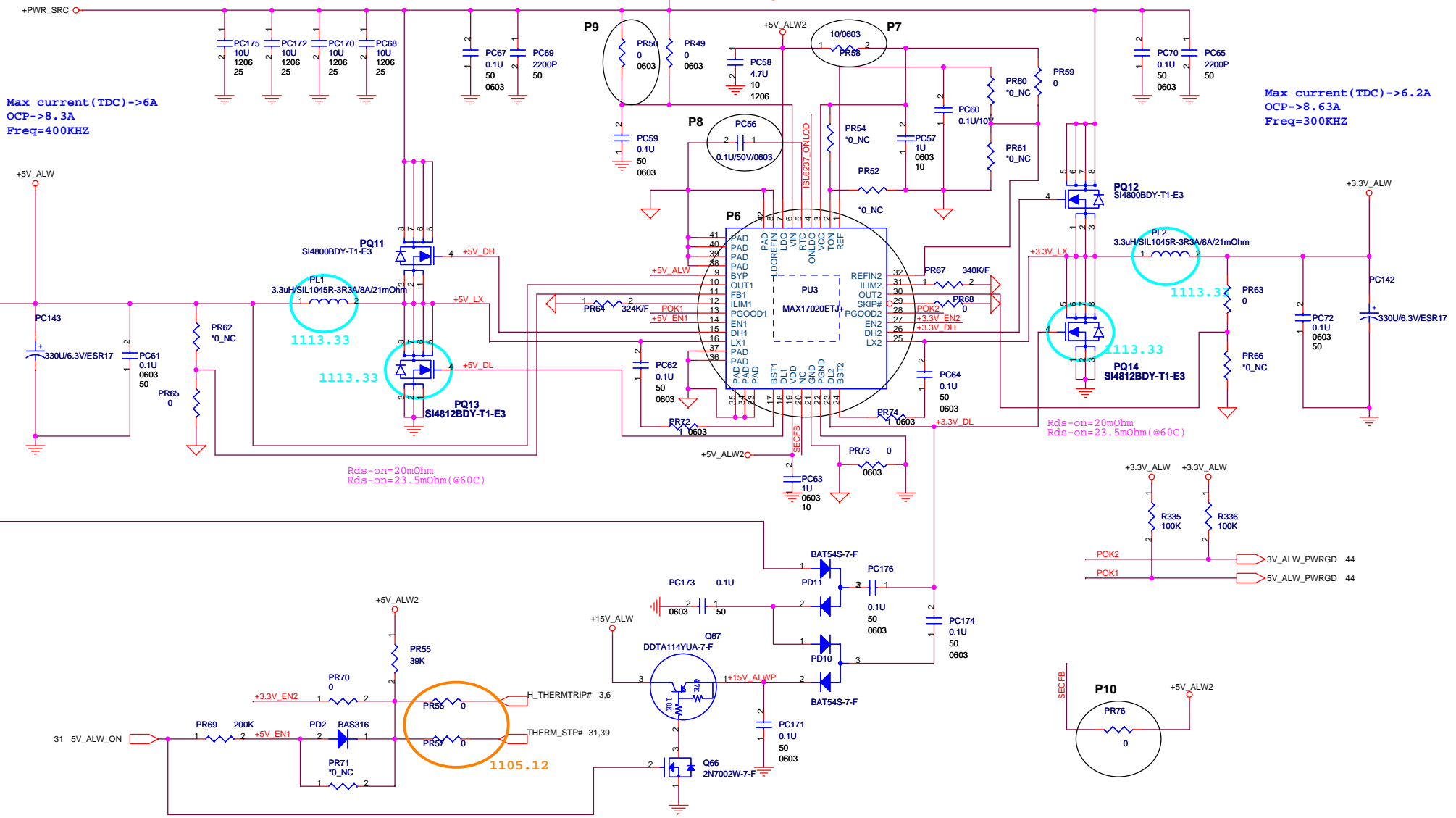
 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
	FM6B	1A
Date:	Monday, June 30, 2008	Sheet 50 of 60



DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

Place these CAPS close to FETs

Place these CAPS close to FETs



Max current (TDC) -> 6A
 OCP -> 8.3A
 Freq = 400KHZ

Max current (TDC) -> 6.2A
 OCP -> 8.63A
 Freq = 300KHZ

Rds-on = 20mOhm
 Rds-on = 23.5mOhm (@60C)

Rds-on = 20mOhm
 Rds-on = 23.5mOhm (@60C)

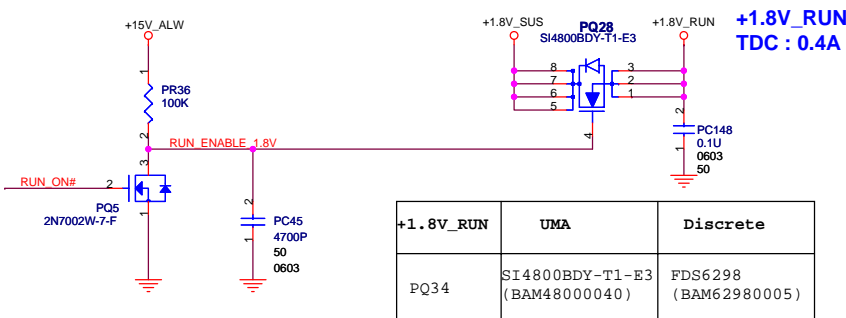
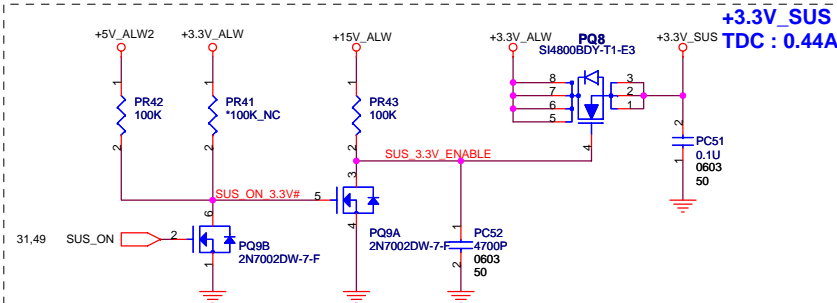
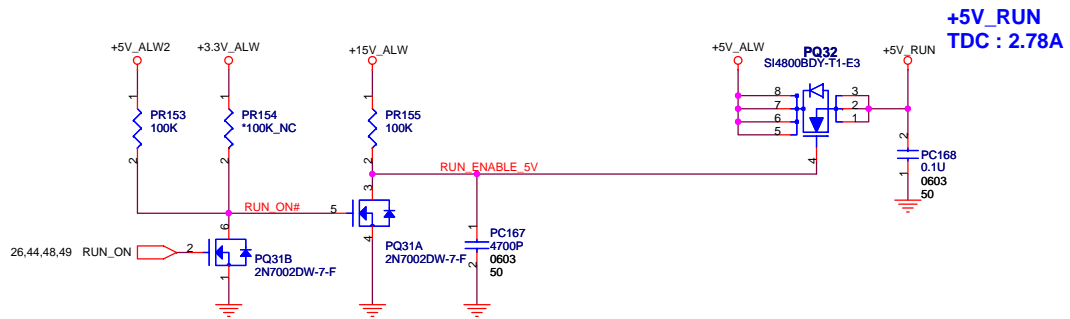
+3.3V_ALW +3.3V_ALW

POK2 3V_ALW_PWRGD 44
 POK1 5V_ALW_PWRGD 44

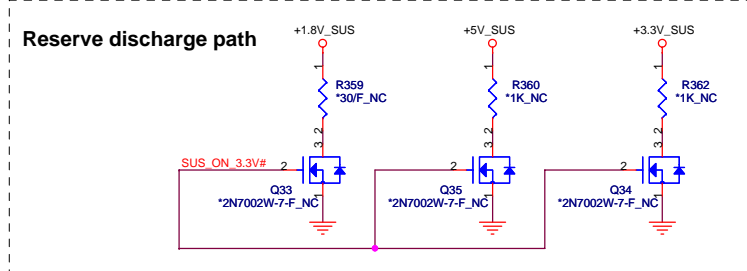
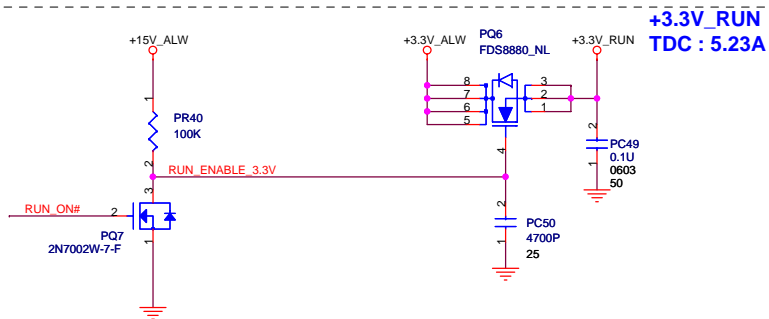
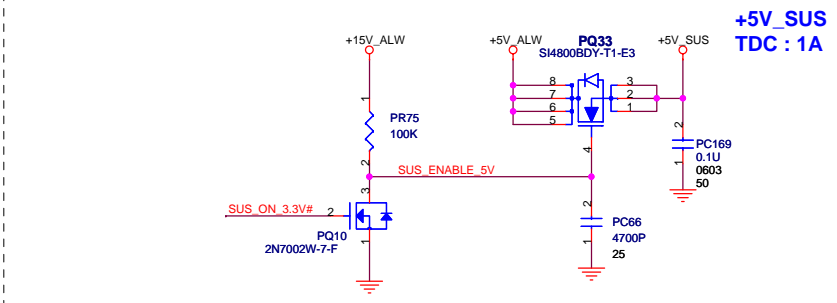
**QUANTA
COMPUTER**

Title: 3VALW.5V.3V, Power On

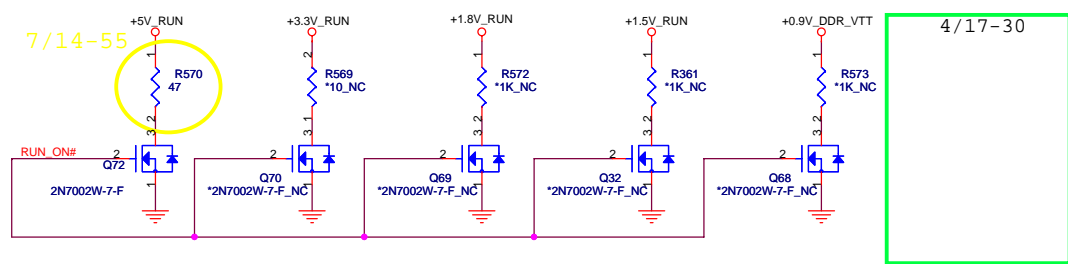
Size: Document Number FM6B	Rev: 1A
Date: Tuesday, July 15, 2008	
Sheet 52 of 60	

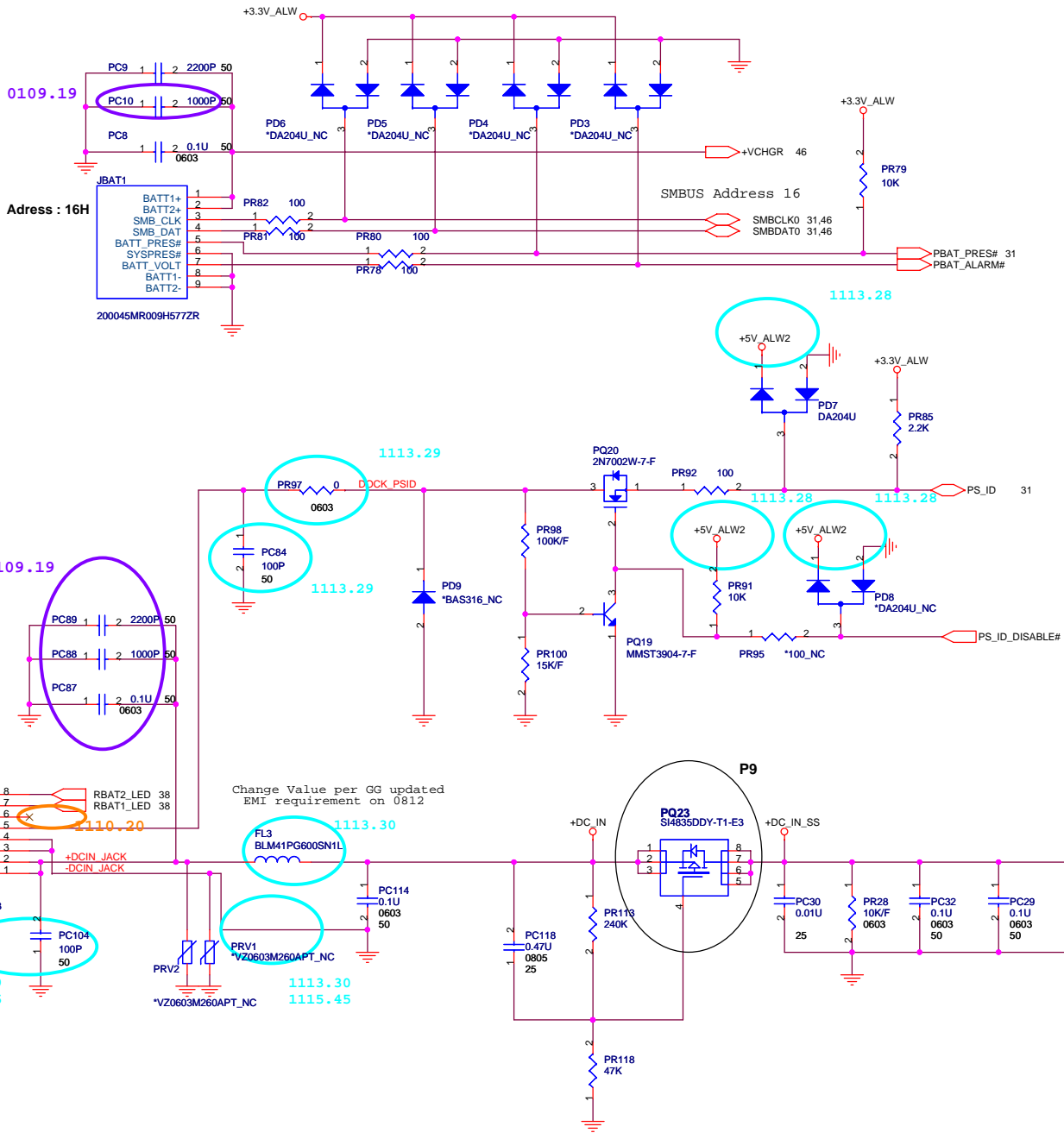


+1.8V_RUN	UMA	Discrete
PQ34	SI4800BDY-T1-E3 (BAM48000040)	FDS6298 (BAM62980005)

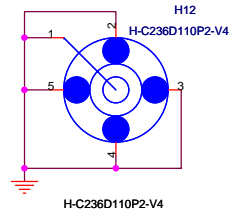
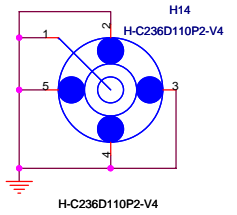
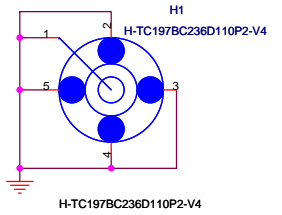
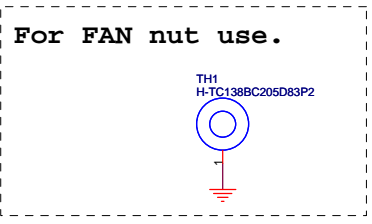
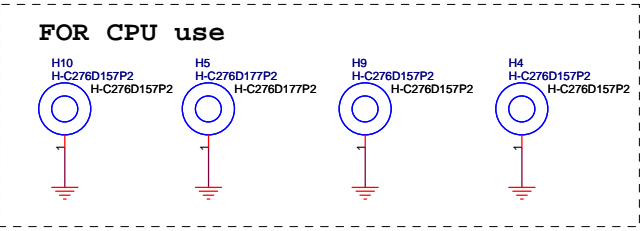
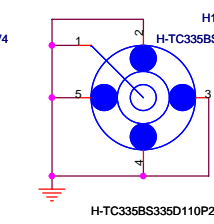
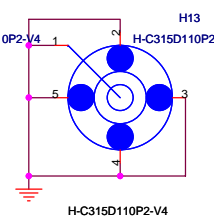
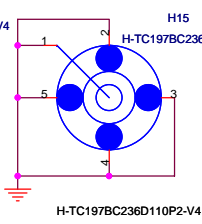
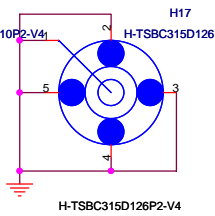
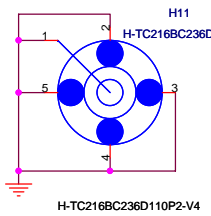
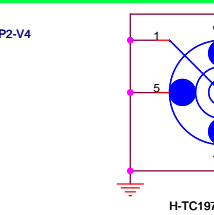
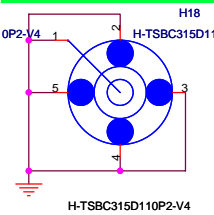
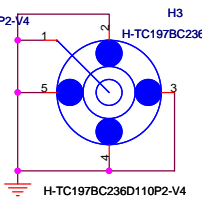
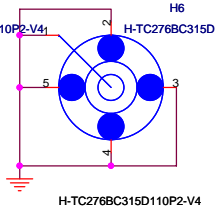
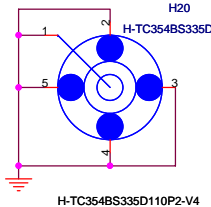
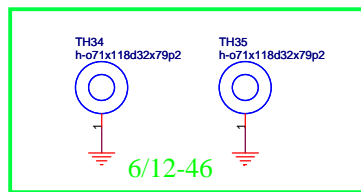
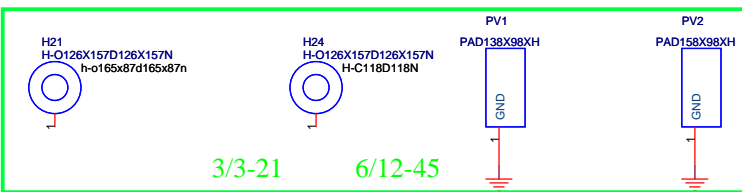
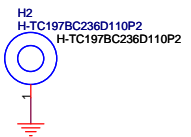
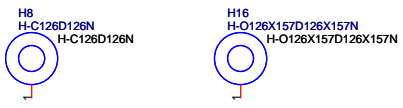


Reserve discharge path





Title DCIN, BATT CONNECTOR		
Size FM6B	Document Number FM6B	Rev 1A
Date: Wednesday, July 16, 2008	Sheet 54	of 60



**QUANTA
COMPUTER**

Title: SCREW PAD

Size	Document Number FM6B	Rev 1A
------	-------------------------	-----------

Date: Monday, June 30, 2008 Sheet 55 of 60

Reserved for EMI.

Stitching caps.

