

#### Lossless Tracking Procedure and Results Summary Reference Design: Volterra VT223 Regulator and SMT4214 TRAKKER<sup>™</sup>

#### BACKGROUND

As discussed in AN-26, Summit Microelectronic's SMT4004 also performs low level, loss-less supply voltage tracking of a discrete PWM controller often used to generate system level power. This Application Note describes another example of low-level tracking using Summit's SMT4214 Quad Tracking Manager and Volterra's VT223C-ADJ Step-Down Switching Regulator. A complete solution is provided presented using the low-level tracking technique to properly power-on a Xilinx FPGA.

#### **Typical Supply Voltage Tracking**

As depicted in Figure 1 through Figure 3, the SMT4214 typically tracks power supply voltages using series power MOSFETs. An on-board charge pump (VGG\_CAP) drives the MOSFET gate terminals well into enhancement upon command from the PWR\_ON# pin or via the l<sup>2</sup>C interface. The SMT4214 also tracks down the supplies by de-asserting the PWR\_ON# pin or by using the l<sup>2</sup>C software interface command. In addition to providing voltage tracking, the use of the series MOSFETs provides a means of quickly disconnecting the power supplies from the load using the voltage/current fault monitoring features of the SMT4214.

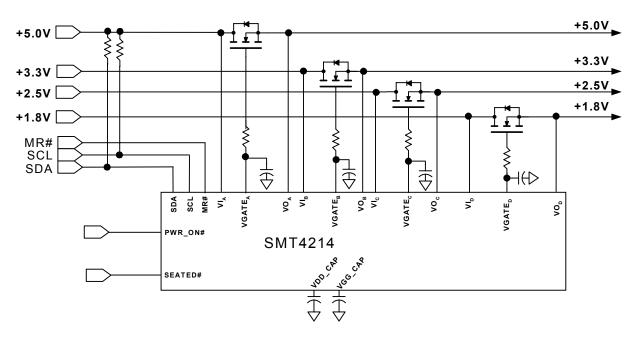
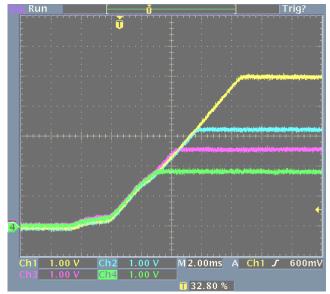


Figure 1: SMT4214 Tracking 4 Power Supplies Using Series Power MOSFETs





## Figure 2: SMT4214 Track Up Waveforms Low-Level Tracking

When PCB space is a premium, the SMT4214 can be interfaced with on-board discrete (e.g., monolithic controllers) power supplies to obtain accurate voltage tracking eliminating the series power MOSFET. For example, Volterra's VT223-ADJ step-down switching regulator is readily controlled and monitored by the SMT4214 using a simple and inexpensive 'low-level' tracking interface technique.

#### VT223-ADJ to SMT4214 Interface

The output voltage of the VT223-ADJ is set by connecting a suitable resistor from the VREF pin to ground. The formula for setting the output voltage is:

# **Application Note 35**

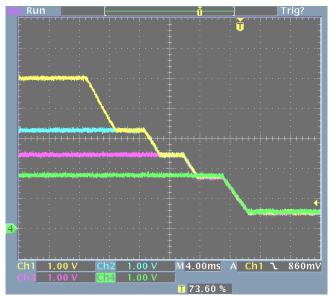


Figure 3: SMT4214 Track Down Waveforms

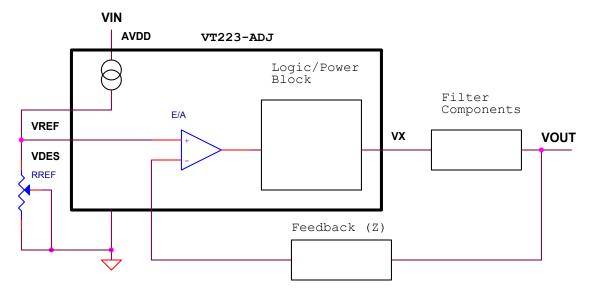
**Equation 1:** VOUT = 
$$1.23V\left(\frac{\text{RREF}}{43.2\text{k}\Omega}\right)$$

Where:

VOUT is the output voltage.

1.23V is the internal bandgap reference voltage. 43.2k $\Omega$  is the recommended RBIAS resistor value.

## The output voltage may be fixed or adjusted by varying the value of RREF (Figure 4).



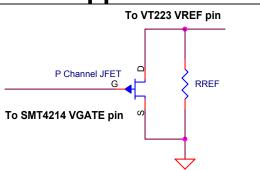
#### Figure 4: Simplified Block Diagram of VT223-ADJ with VOUT Adjustment



### **Application Note 35**

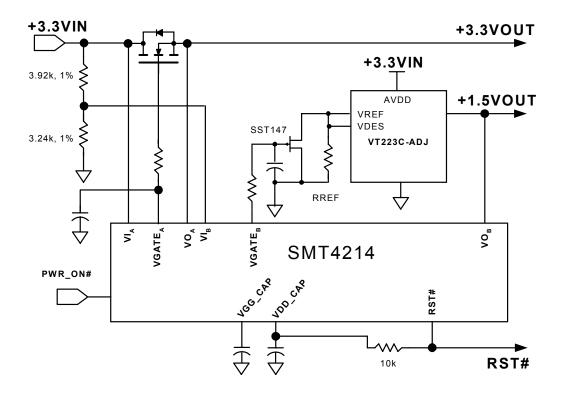
To permit the SMT4214 to control the output voltage of the VT223, an active device is employed as a 'bridge' between the SMT4214's VGATE output and the VT223's VREF input. A suitable choice is a depletion-mode, JFET transistor.

The JFET's drain to source resistance is low when its gate to source voltage is zero volts and increases to a virtual open circuit when the pinch-off voltage ( $V_{GS(off)}$ ) is reached. Figure 4 displays the electrical connections made to the VT223 using a P-channel JFET. The gate terminal is driven by the SMT4214's VGATE output.



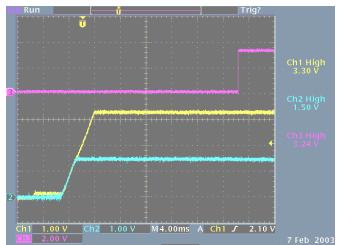
# Figure 5. SMT4214 to VT223 Active Interface

Connecting the SMT4214 to the VT223, as shown in Figure 6, results in the Track-Up and Track-Down waveforms displayed in Figures 7 and 8, respectively. Note the linearity of the waveforms provided by the SMT4214's closed loop control of the slew-rate and maximum voltage differential allowed between channels.



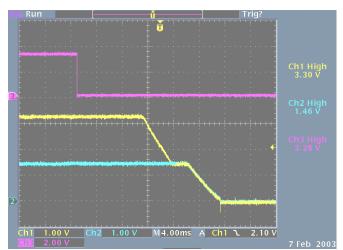
# Figure 6. SMT4214/VT223 Interface Schematic (Simplified) for Tracking 2 Voltages with Reset Control.





#### Figure 7: Power Up Event Tektronix TDS3054 Time-Base = 4mS/Div Channel 1, (Yellow) 3.3V Tracking, = 1V/Div Channel 2, (Blue) 1.5V Tracking = 1V/Div Channel 3, (Purple) RESET# output= 2V/Div

# **Application Note 35**



**Figure 8: Power Down Event** Tektronix TDS3054 Time-Base = 4mS/Div Channel 1, (Yellow) 3.3V Tracking, = 1V/Div Channel 2, (Blue) 1.5V Tracking = 1V/Div Channel 3, (Purple) RESET# output= 2V/Div



#### Powering The Xilinx Vertex E FPGA

To power the Xilinx Vertex E FPGA is the VT223 Evaluation Board is modified to:

- 1. Increase the output voltage from 1.5V to 1.8V.
- 2. Desensitize the VT223 from track down anomalies.

To increase the output voltage first determine the new value of RREF:

**Equation 2:** RREF = 
$$\frac{1.8V \times 43.2k\Omega}{1.23V} = 63.2k\Omega$$
  
Use 63.4kΩ, 1%.

The following changes to the VT223 Evaluation Board circuit were made to prevent the STAT output from being effected by the track-down event:

- 1. Increase the value of R9 from 10k to 25k.
- 2. Change C8 from 0.01uF to 1000pF.
- 3. Replace R7 (100k) with a zero ohm jumper.

Finally, the SMT4214 program settings are modified to allow the core voltage (VCCINT, 1.8V) to turn on before the I/O supply (VCCO, 3.3V).

A simplified schematic of the circuit is displayed in Figure 9. The complete schematic is shown in Figure 14.

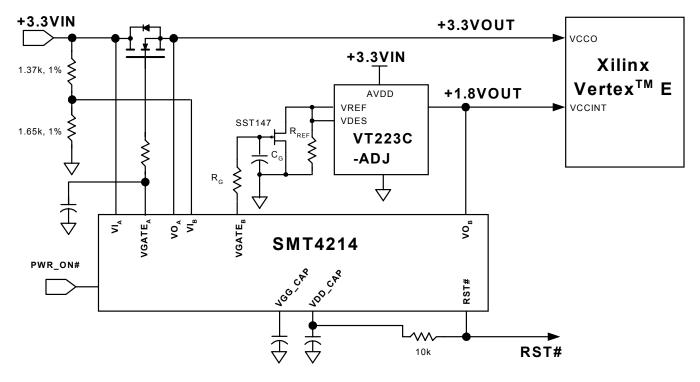


Figure 9: SMT4214/VT223 Powering the Xilinx Vertex E FPGA

#### **Performance Results**

The resulting track-up waveforms into the Xilinx FPGA are displayed in Figures 10 and 11. Note the 1.8V ramps on first followed by the 3.3V.

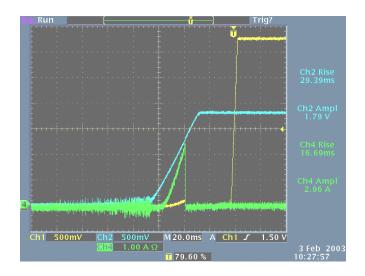
The value of  $C_G$  and the gate voltage VGATEV level directly affects the rise time of the 1.8V supply voltage as well as the delay between the 1.8V and 3.3V supplies.

The waveform in Figure 10 uses a 2uF value for the  $C_G$  capacitor and a VGATEV voltage of 10.5V while Figure 11 uses a 2uF capacitor with 14.5V and Figure 12/13 uses 3uF with 10.5/14.5V VGATEV.

Note:

The slight voltage 'lift' occurring on the 3.3V output (channel 1, yellow) is of no consequence but if deemed necessary can be reduced by adding a suitable resistive load from the 3.3V output node to ground. Start with a  $1k\Omega$ .

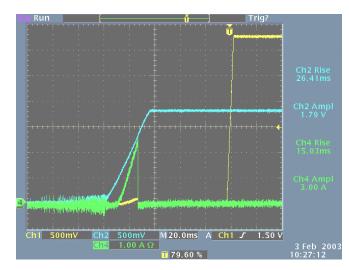




#### Figure 10: Xilinx Power-On Event CG = 2uF, VGATEV=10.5V

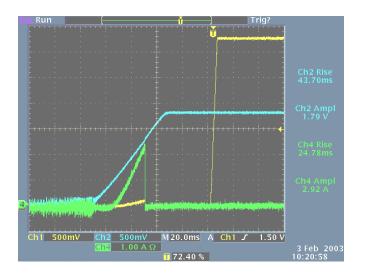
Tektronix TDS3054, Time-Base = 20mS/Div Channel 1, (Yellow) 3.3V Output = 500mV/Div Channel 2, (Blue) 1.8V Output = 500mV/Div Channel 4, (Green) 1.8V Current = 1A/Div

# **Application Note 35**



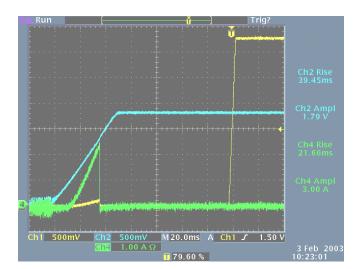
#### Figure 11: Xilinx Power-On Event CG = 2uF, VGATEV=14.5V

Tektronix TDS3054, Time-Base = 20mS/Div Channel 1, (Yellow) 3.3V Output = 500mV/Div Channel 2, (Blue) 1.8V Output = 500mV/Div Channel 4, (Green) 1.8V Current = 1A/Div



#### Figure 12: Xilinx Power-On Event CG = 3uF, VGATEV=10.5V

Tektronix TDS3054, Time-Base = 20mS/Div Channel 1, (Yellow) 3.3V Output = 500mV/Div Channel 2, (Blue) 1.8V Output = 500mV/Div Channel 4, (Green) 1.8V Current = 1A/Div



#### Figure 13: Xilinx Power-On Event CG = 3uF, VGATEV=14.5V

Tektronix TDS3054, Time-Base = 20mS/Div Channel 1, (Yellow) 3.3V Output = 500mV/Div Channel 2, (Blue) 1.8V Output = 500mV/Div Channel 4, (Green) 1.8V Current = 1A/Div



### **Application Note 35**

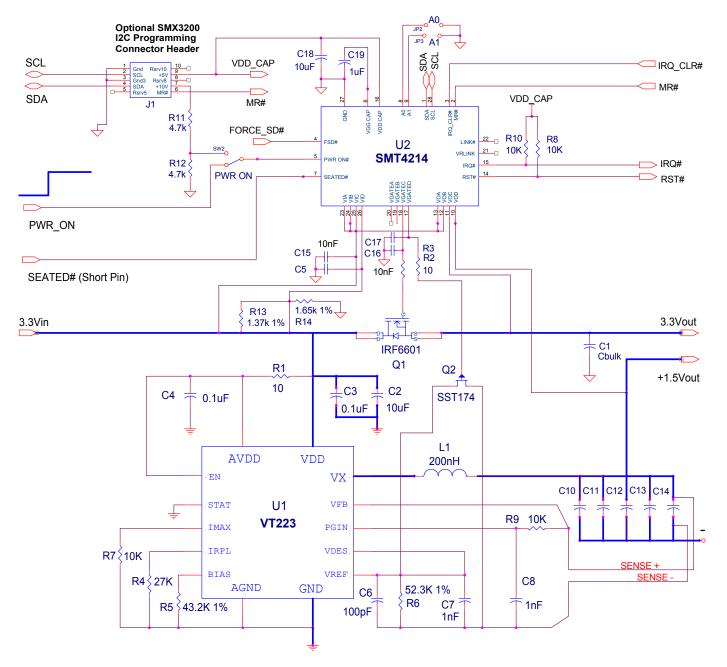


Figure 14: SMT4214/VT223 Complete Schematic



### **Application Note 35**

#### Table 1 – Bill of Materials

ltem	Description	Vendor / Part Number	Qty	Ref. Des.
Resist	tors			
1	10Ω, 1/10W, 5%, 0805, SMD	Any	3	R1, R2, R3
2	10KΩ, 1/10W, 5%, 0805, SMD	Any	4	R7, R8, R9, R10
3	4.7KΩ, 1/10W, 5%, 0805, SMD	Any	2	R11, R12
4	27KΩ, 1/10W, 5%, 0805, SMD	Any	1	R4
5	43.2KΩ, 1/10W, 1%, 0805, SMD	Any	1	R5
6	52.3KΩ, 1/10W, 1%, 0805, SMD	Any	1	R6
7	1.37KΩ, 1/10W, 1%, 0805, SMD	Any	1	R13
8	1.65KΩ, 1/10W, 1%, 0805, SMD	Any	1	R14
Capac	citors			
9	10nF, 50V, ceramic, 0805, SMD	Any	4	C5, C15, C16, C17
10	0.1µF, 50V, ceramic, 0805, SMD	Any	2	C3, C4
11	1nF, 50V, ceramic, 0805, SMD	Any	2	C7, C8
12	1µF, 50V, ceramic, 0805, SMD	Any	1	C19
13	10µF, 16V, Tantalum, Size 'B'	AVX, TAJA106M016	2	C2, C18
14	100pF, 50V, ceramic, 0805, SMD	Any	2	C6
15	Bulk capacitors	Any	6	C1, C10-C14
Induct	tors			
16	200nH	Vishay-Dale, IHLP-2525CZ-01 0.2	1	L1
Semic	conductors			
17	JFET, P-Channel, 30V,	Vishay, SST174	1	Q2
18	MOSFET, N-Channel, 30V,	International Rectifier, IRF6601	1	Q1
19	Quad Tracking Manager	Summit Microelectronics, Inc., SMT4214	1	U2
20	Step-down Switching Regulator	Volterra Semiconductor Corp, VT223.	1	U1

#### CONCLUSION

Advanced system designs demand precision control of the supply voltage power-on/off event. The required control circuitry must not use precious PCB space otherwise intended for the end product. Summit's Tracking Managers minimize PCB space while delivering precision performance in Tracking/Sequencing environments. Elimination of the series MOSFET, when used with premier voltage conversion devices such as the Volterra VT223 result in an easy to implement, reliable design. In this Application Note a single Volterra Step Down Converter was used with the SMT4214 and a series MOSFET to track/sequence another voltage (3.3V).

It must be noted that another VT223 could have generated the 3.3V supply in exactly the same manner as the 1.8V. In fact, a single SMT4214 can manage as many as four loss-less supply voltages. Using the Master/Slave capability of the SMT4214 allows up to 32 channels to be tracked and/or soft-started.

Further information is contained in the links shown in Table 2 to Summit Microelectronics', Volterra Semiconductor Corp.'s and Xilinx Inc.'s web sites.



#### Table 2 - Support material

SMX3200 Programming Kit	http://www.summitmicro.com/tech_support/program_kit/SMX3200.htm
SMT4214EV Evaluation Board	http://www.summitmicro.com/tech_support/eval_kits.htm
SMT4214 Windows GUI Software	http://www.summitmicro.com/tech_support/tech.htm#GUI
Volterra Semiconductor Corp. Web Site	http://www.volterra.com/
App Note 28 - SMT4214 Windows GUI User Guide and Configuration Register Descriptions	http://www.summitmicro.com/tech_support/notes/note28/note28.htm
App Note 26 - SMT4004 Advanced Voltage Tracking Methods Boost Efficiency, Reliability	http://www.summitmicro.com/tech_support/notes/note26.htm
App Note 31 - Xilinx Virtex <sup>™</sup> -E, Spartan <sup>™</sup> -IIE FPGA and SMT4004 TRAKKER <sup>™</sup> Supply Manager Reference Design: Procedure and Results Summary	http://www.summitmicro.com/tech_support/notes/note31/note31-00.htm
Xilinx Production Change Notification PCN2002-07	http://www.xilinx.com/partinfo/notify/pcn2002-07.htm
Powering Xilinx FPGAs	http://www.xilinx.com/xapp/xapp158.pdf

#### NOTICE

SUMMIT Microelectronics, Inc. reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. SUMMIT Microelectronics, Inc. assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein reflect representative operating parameters, and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, SUMMIT Microelectronics, Inc. shall not be liable for any damages arising as a result of any error or omission.

SUMMIT Microelectronics, Inc. does not recommend the use of any of its products in life support or aviation applications where the failure or malfunction of the product can reasonably be expected to cause any failure of either system or to significantly affect their safety or effectiveness. Products are not authorized for use in such applications unless SUMMIT Microelectronics, Inc. receives written assurances, to its satisfaction, that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; and (c) potential liability of SUMMIT Microelectronics, Inc. is adequately protected under the circumstances.

Revision 1.0 - This document supersedes all previous versions. Please check the Summit Microelectronics Inc. web site at <u>www.summitmicro.com</u> for updates.

© Copyright 2003 SUMMIT MICROELECTRONICS, Inc. Power Management for Communications™

"Xilinx" and the Xilinx logo are registered trademarks of Xilinx, Inc.

Silicon Power Solutions<sup>™</sup> and Volterra are registered trademarks of Volterra Semiconductor Corporation.

 $I^2C$  is a trademark of Philips Corporation.