

Compal Confidential

HCW50 Schematics Document

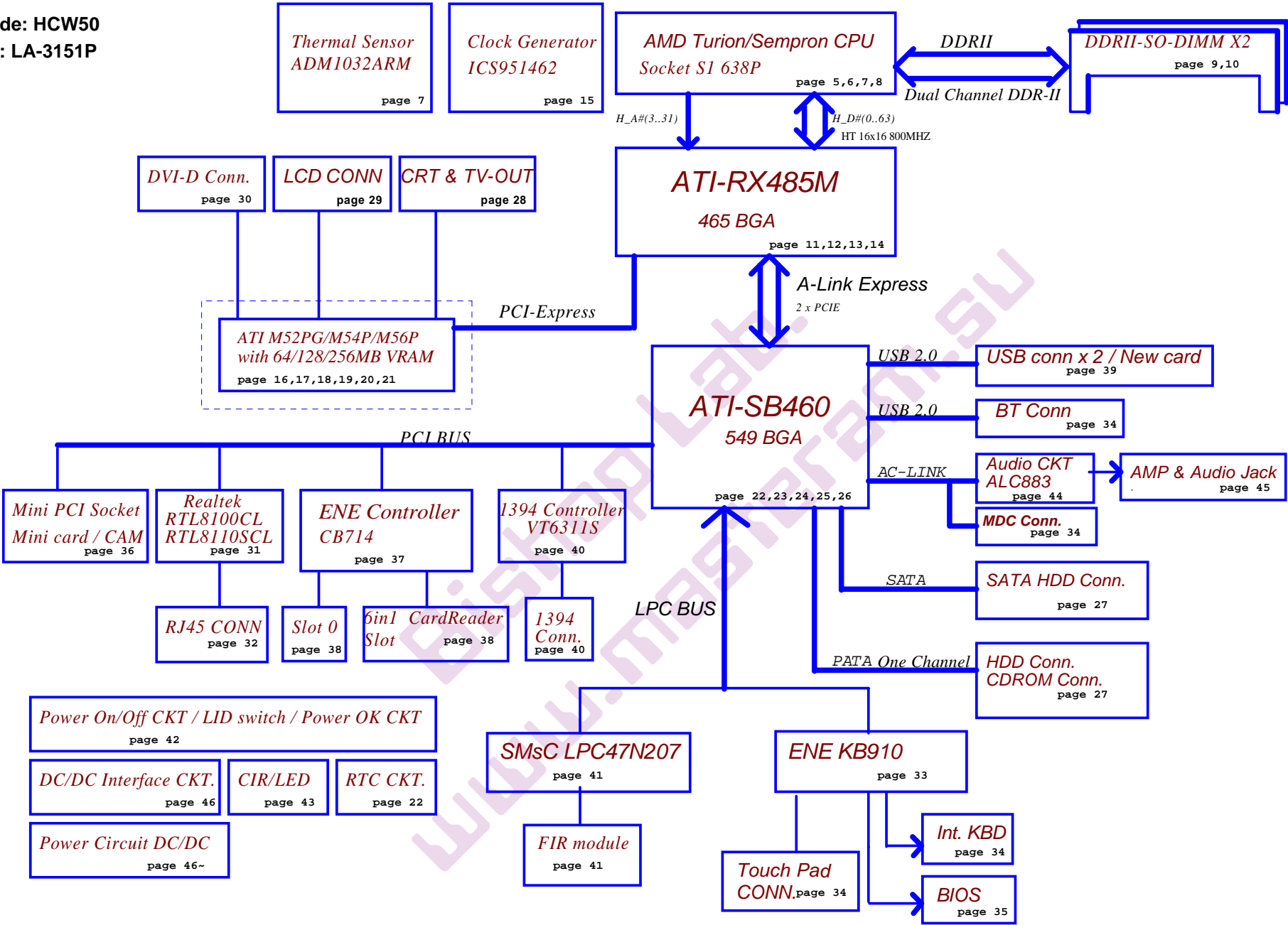
AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

2006 / 02 / 28 Rev:0.3 (For PVT)

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Issued Date	2005/05/09	Deciphered Date	2006/03/08	Title SCHEMATIC, M/B LA-3151P	
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Project Code: HCW50
File Name : LA-3151P



Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VS	VS always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0-1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

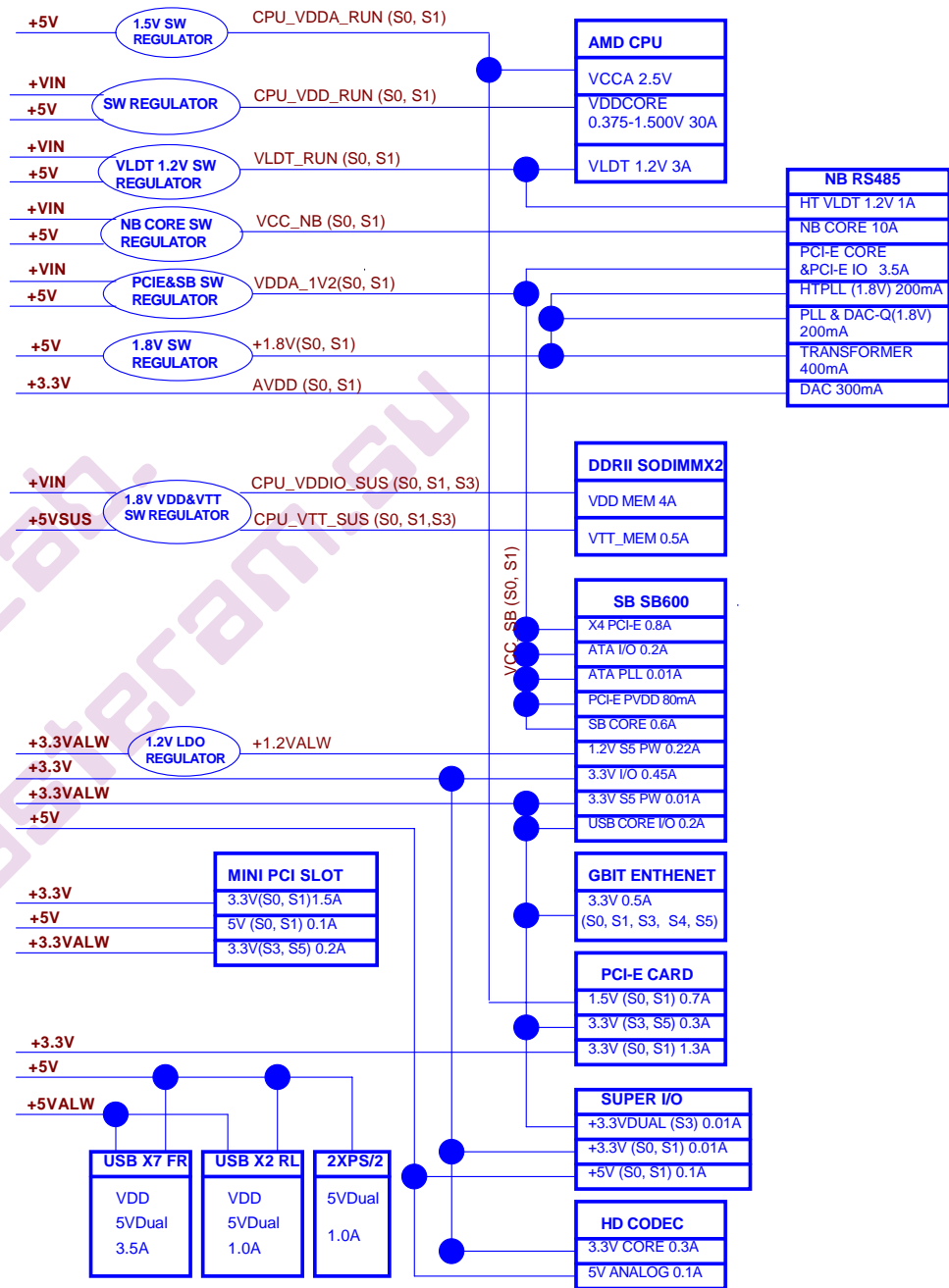
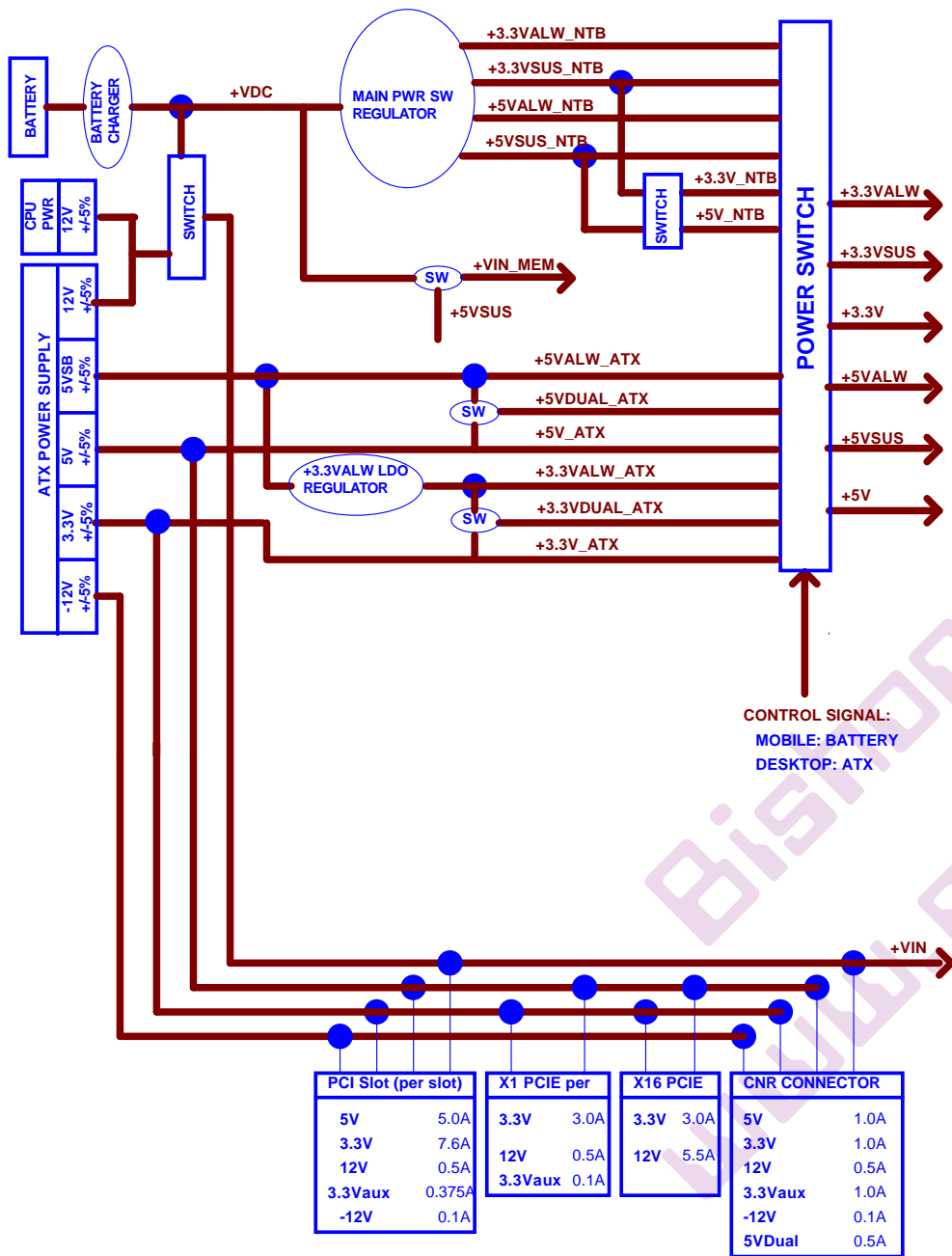
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

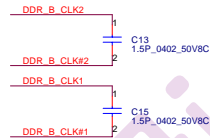
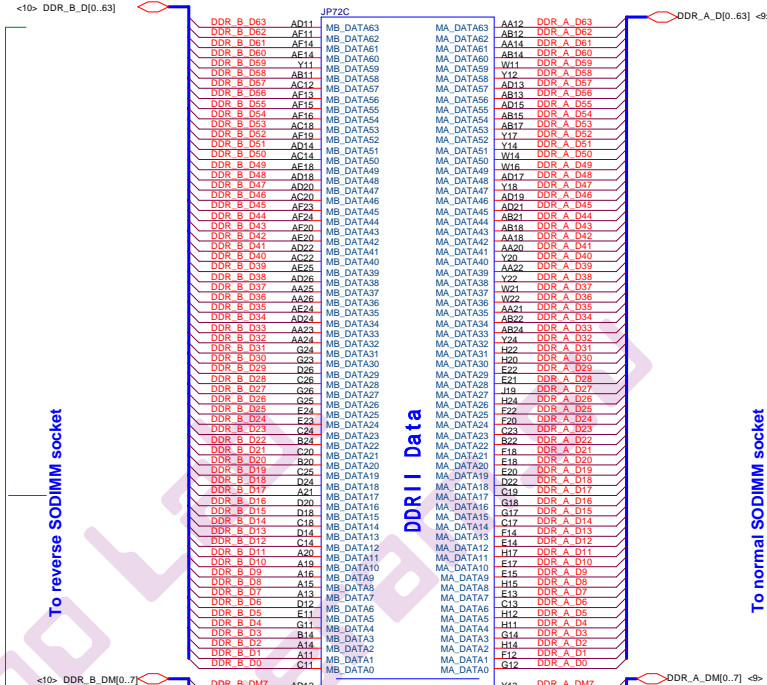
SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

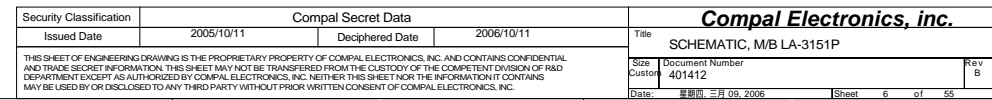
BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

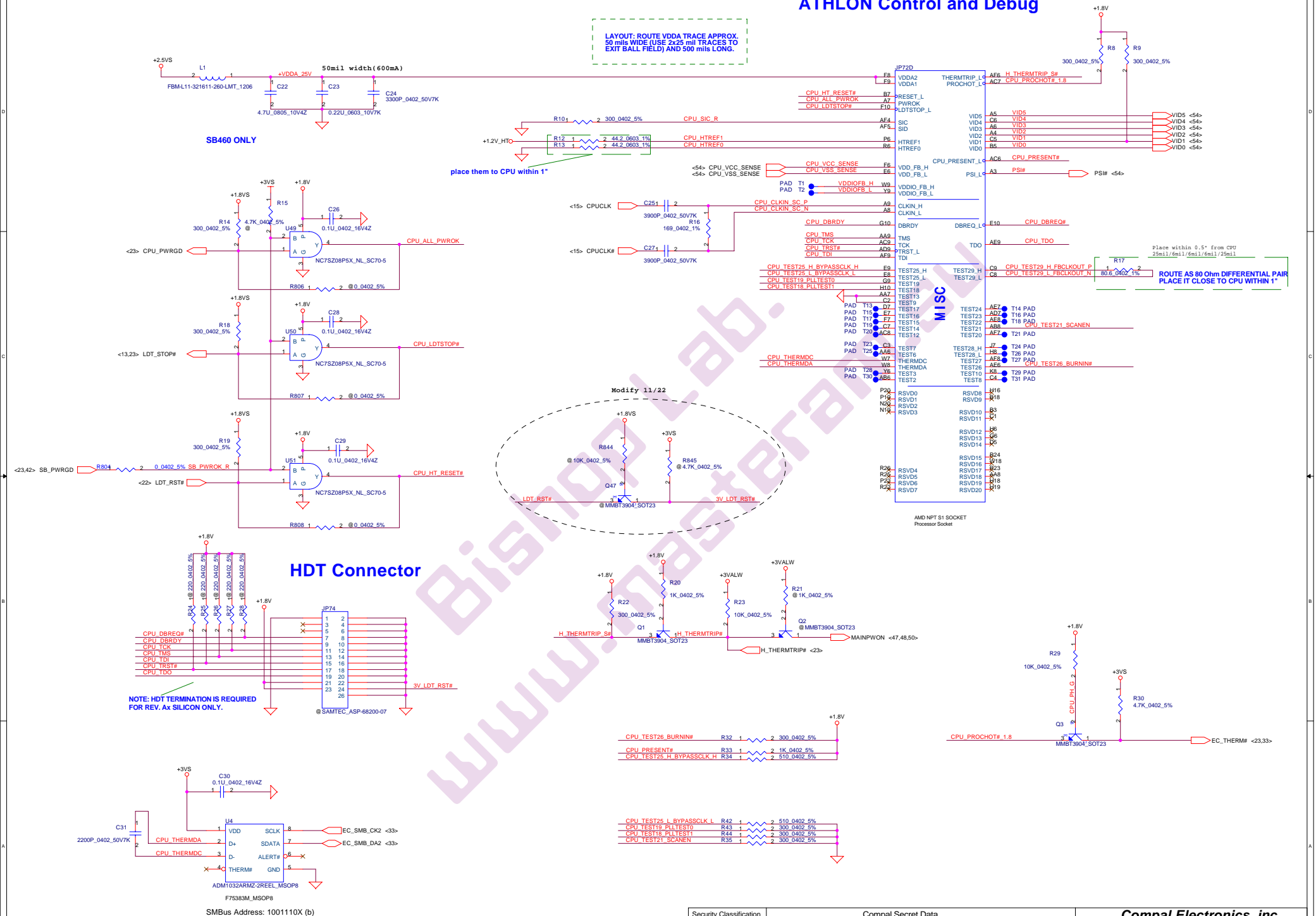




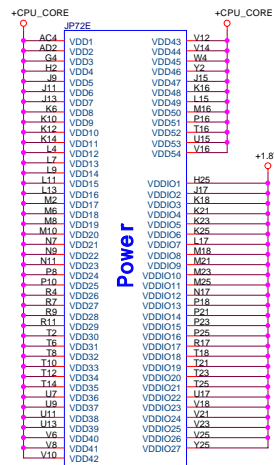
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



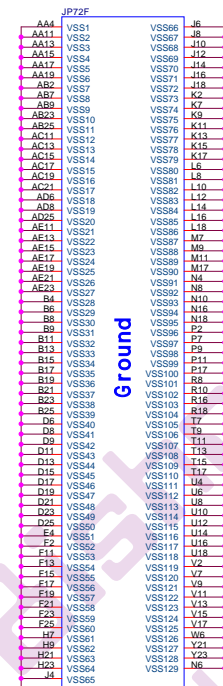
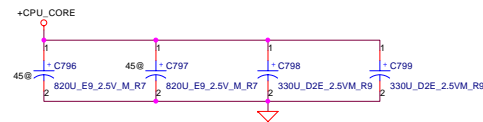
ATHLON Control and Debug



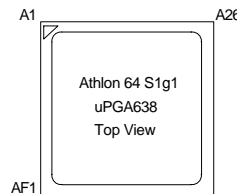
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Athlon 64 S1
Processor Socket

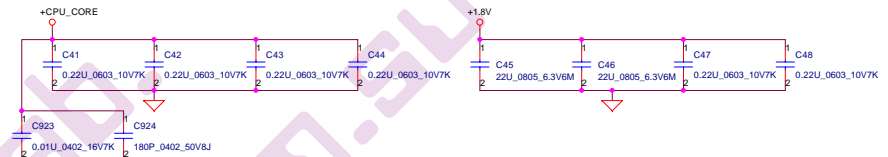
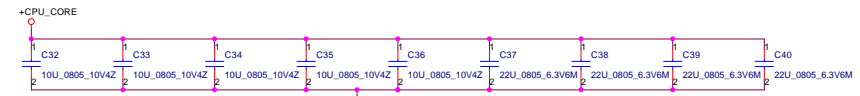


Athlon 64 S1
Processor Socket

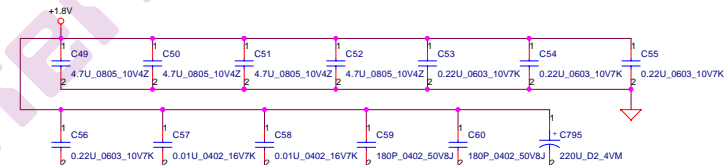


Athlon 64 S1g1
uPGA638
Top View

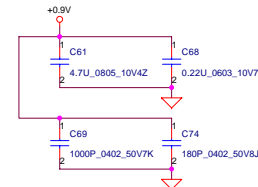
BOTTOMSIDE DECOUPLING



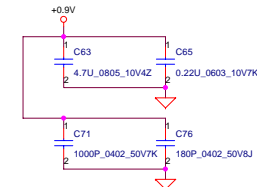
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



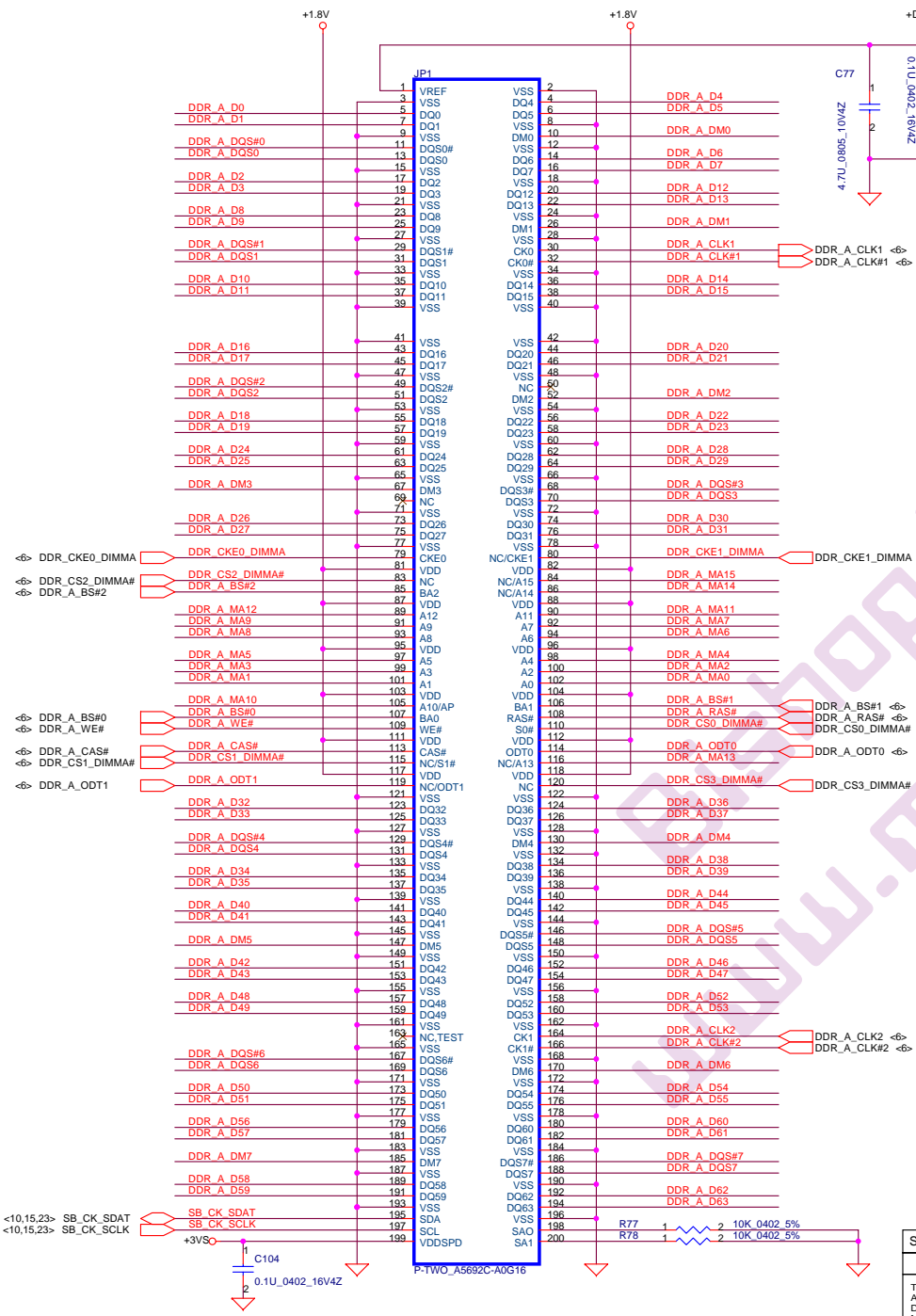
CPU left-hand side



CPU right-hand side

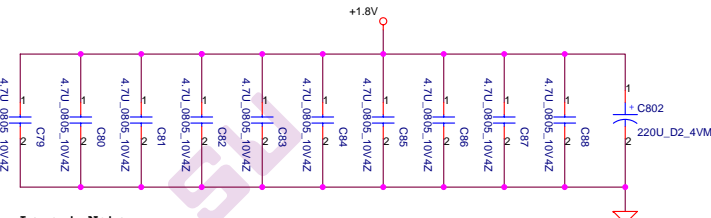


PROCESSOR POWER AND GROUND

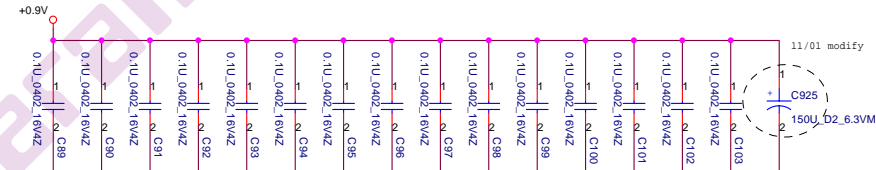


<6> DDR_A_D[0..63] <6> DDR_A_DM[0..7] <6> DDR_A_DQS[0..7] <6> DDR_A_MA[0..15] <6> DDR_A_DQS#[0..7]

DDR A D[0..63]
DDR A DM[0..7]
DDR A DQS[0..7]
DDR A MA[0..15]
DDR A DQS#[0..7]



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

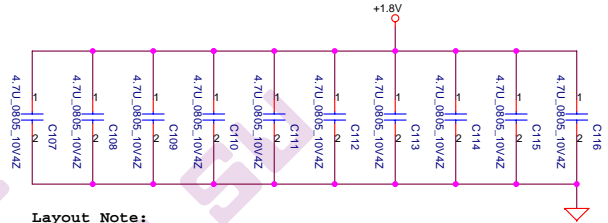
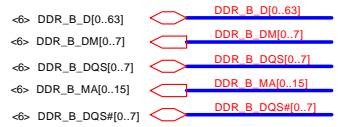
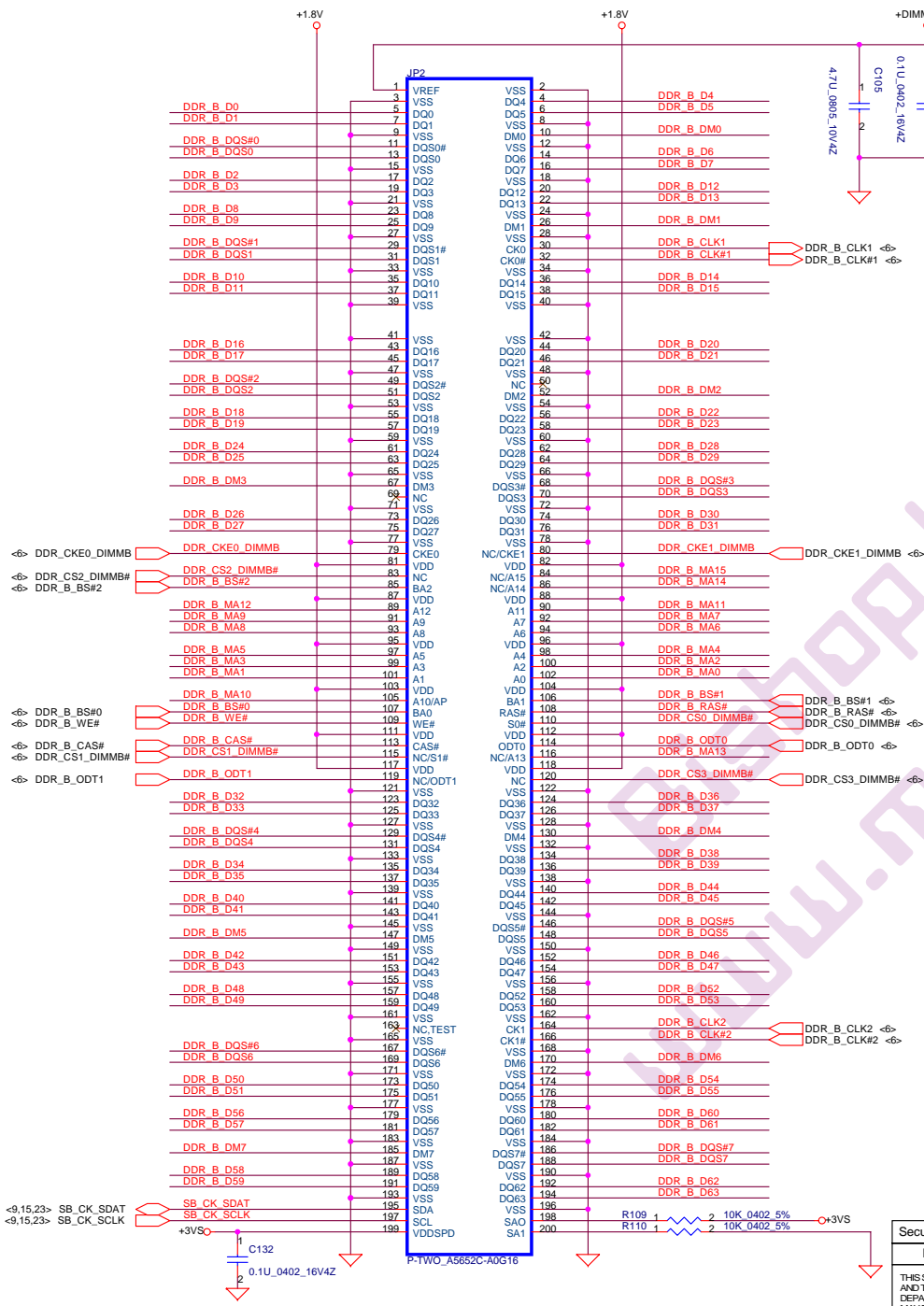


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

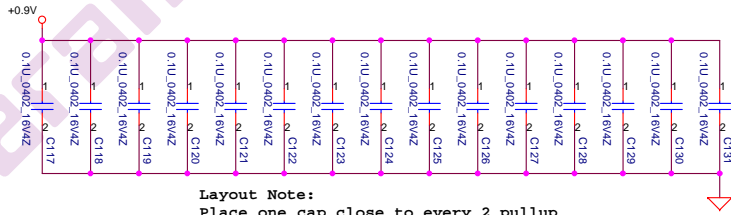
DDR_A_MA15	R47	1	2	47	0402	5%
DDR_A_MA14	R48	1	2	47	0402	5%
DDR_A_MA13	R49	1	2	47	0402	5%
DDR_A_MA12	R50	1	2	47	0402	5%
DDR_A_MA11	R51	1	2	47	0402	5%
DDR_A_MA10	R52	1	2	47	0402	5%
DDR_A_MA9	R53	1	2	47	0402	5%
DDR_A_MA8	R54	1	2	47	0402	5%
DDR_A_MA7	R55	1	2	47	0402	5%
DDR_A_MA6	R56	1	2	47	0402	5%
DDR_A_MA5	R57	1	2	47	0402	5%
DDR_A_MA4	R58	1	2	47	0402	5%
DDR_A_MA3	R59	1	2	47	0402	5%
DDR_A_MA2	R60	1	2	47	0402	5%
DDR_A_MA1	R61	1	2	47	0402	5%
DDR_A_MA0	R62	1	2	47	0402	5%
DDR_A_BS#2	R63	1	2	47	0402	5%
DDR_A_BS#1	R64	1	2	47	0402	5%
DDR_A_BS#0	R65	1	2	47	0402	5%
DDR_A_CAS#	R66	1	2	47	0402	5%
DDR_A_WE#	R67	1	2	47	0402	5%
DDR_A_RAS#	R68	1	2	47	0402	5%
DDR_CKE1_DIMMA	R69	1	2	47	0402	5%
DDR_CKE0_DIMMA	R70	1	2	47	0402	5%
DDR_CS3_DIMMA#	R71	1	2	47	0402	5%
DDR_CS2_DIMMA#	R72	1	2	47	0402	5%
DDR_CS1_DIMMA#	R73	1	2	47	0402	5%
DDR_CS0_DIMMA#	R74	1	2	47	0402	5%
DDR_A_ODT1	R75	1	2	47	0402	5%
DDR_A_ODT0	R76	1	2	47	0402	5%

11/3 Modify

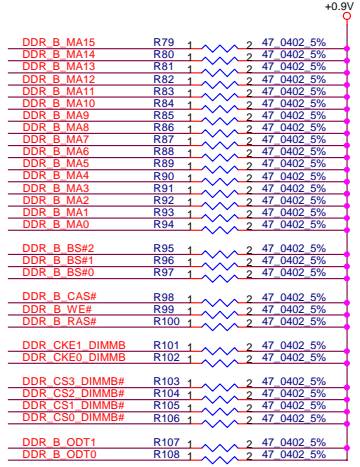
Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V



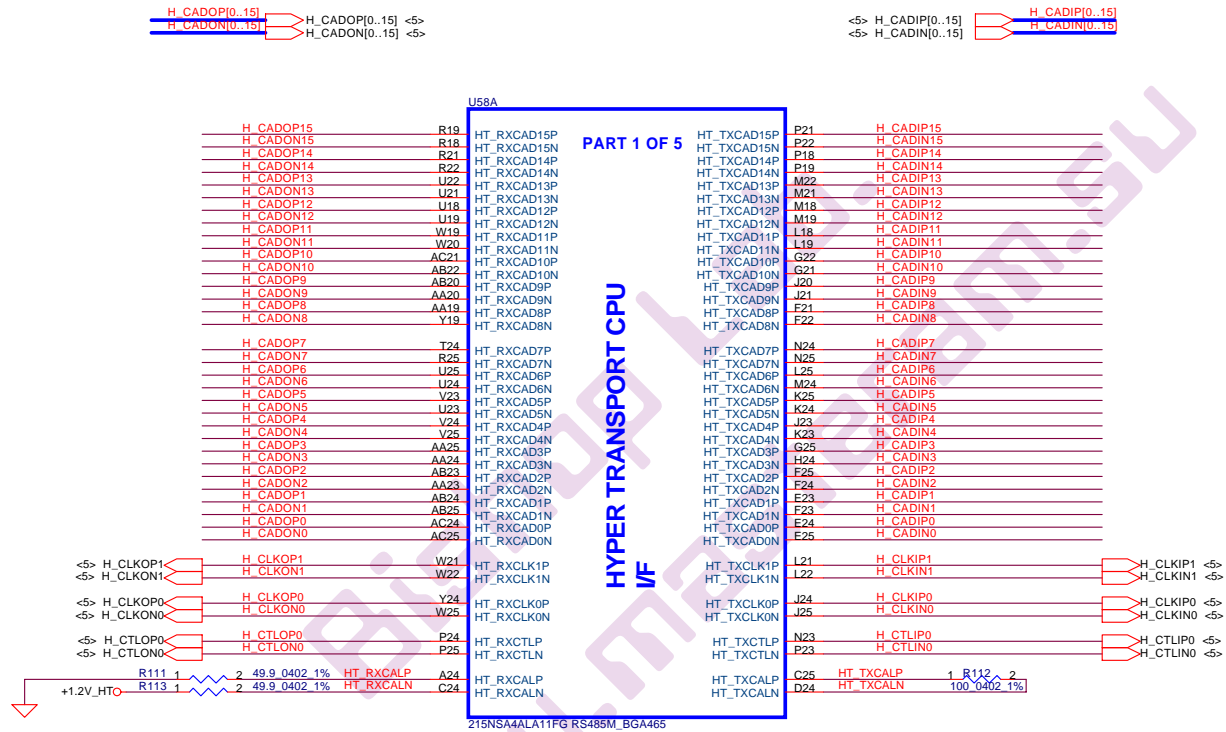
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V



11/3 Modify

Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V

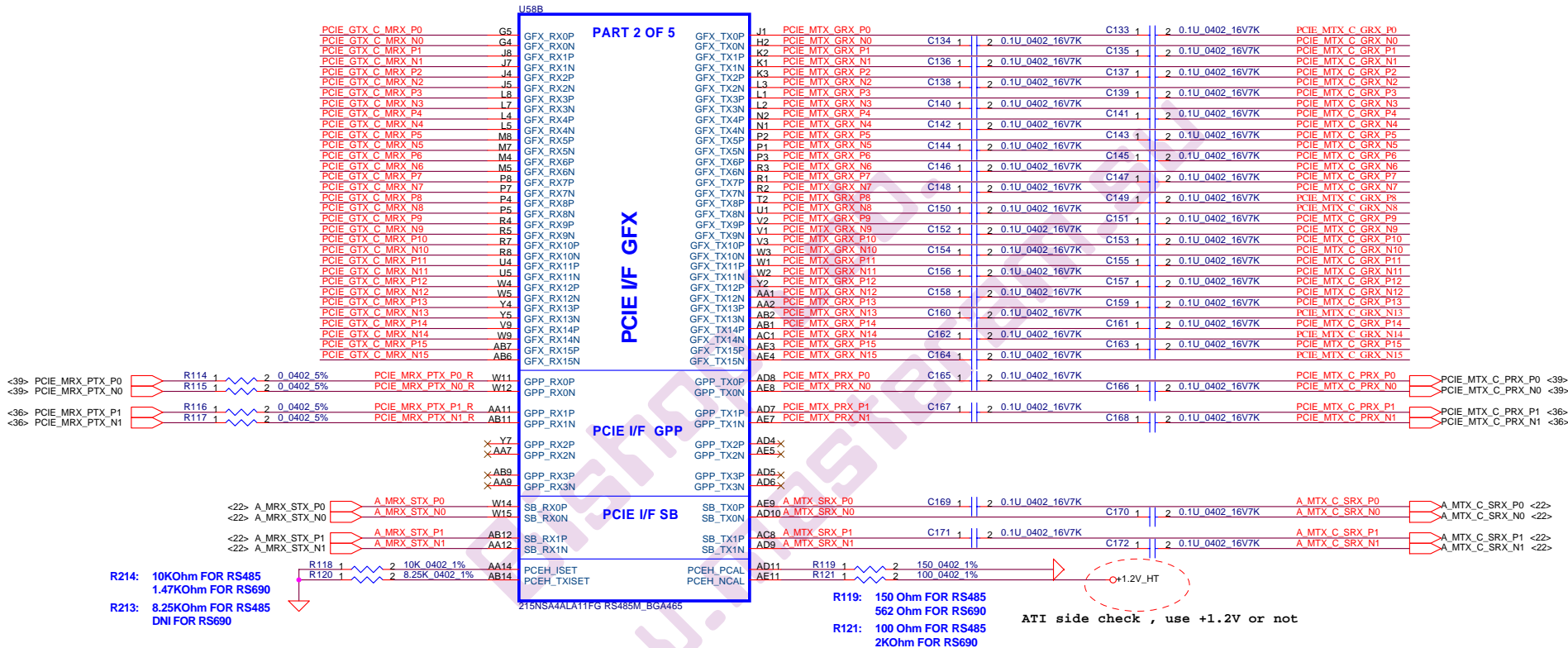
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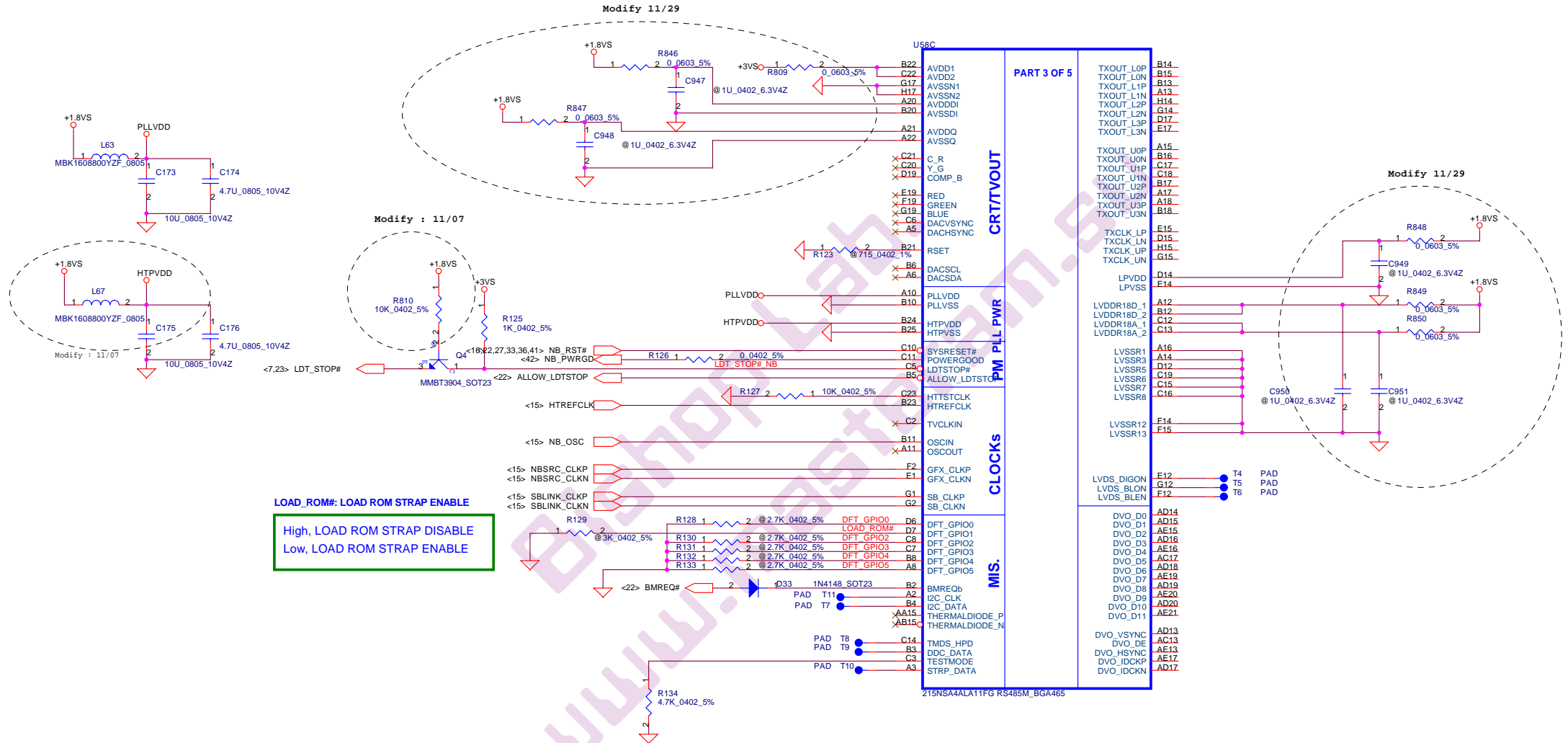
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<16> PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]
<16> PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]

<16> PCIE_MTX_C_GRX_P[0..15] PCIE MTX C GRX P[0..15]
<16> PCIE_MTX_C_GRX_N[0..15] PCIE MTX C GRX N[0..15]

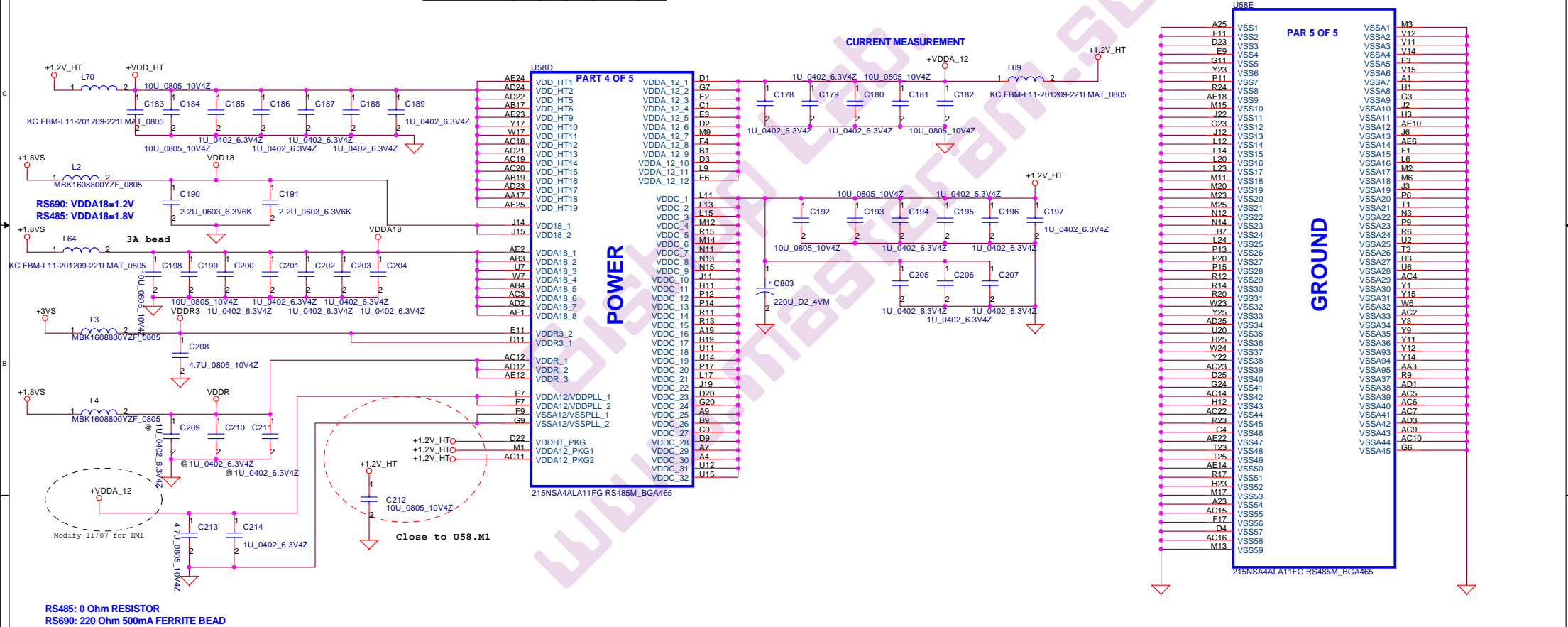


ATI check , CRT / TV/ LVDS can delete or not when I use RX485



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NB RS485 POWER STATES					
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



RS485: 0 Ohm RESISTOR
RS690: 220 Ohm 500mA FERRITE BEAD



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Parallel Resonance Crystal

$I_{oh} = 5 \cdot I_{ref}$
(2.32mA)
 $V_{oh} = 0.71V @ 60 \text{ ohm}$

EXT CLK FREQUENCY SELECT TABLE(MHZ)

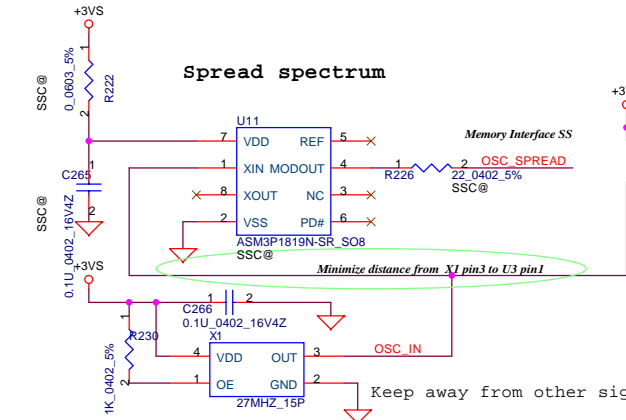
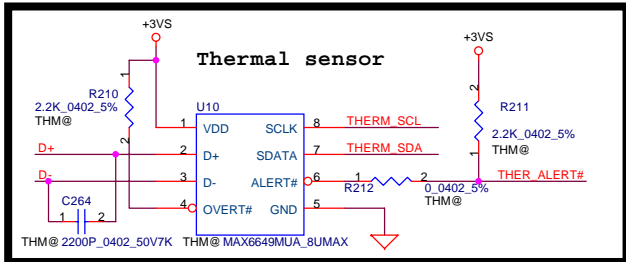
FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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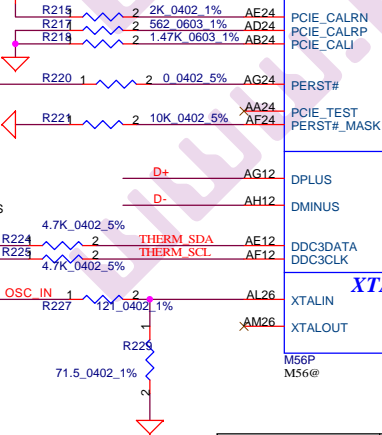
PCIE Lane Reversal

PCIE GTX_C_MRX_N15	C233	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P15	C231	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P15	C231	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N14	C234	2	0.1U_0402_16V7K
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PCIE GTX_C_MRX_N12	C237	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P12	C234	2	0.1U_0402_16V7K
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PCIE GTX_C_MRX_N10	C244	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P10	C241	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P10	C241	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N9	C244	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N9	C244	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P9	C243	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P9	C243	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N8	C249	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N8	C249	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P8	C245	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P8	C245	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N7	C249	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N7	C249	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P7	C241	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P7	C241	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N6	C251	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N6	C251	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P6	C249	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P6	C249	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N5	C254	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N5	C254	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P5	C254	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P5	C254	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N4	C255	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N4	C255	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P4	C254	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P4	C254	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N3	C251	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N3	C251	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P3	C258	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P3	C258	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N2	C259	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N2	C259	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P2	C258	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P2	C258	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_N1	C261	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_N1	C261	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P1	C269	2	0.1U_0402_16V7K
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PCIE GTX_C_MRX_N0	C263	2	0.1U_0402_16V7K	PCIE GTX_C_MRX_P0	C264	2	0.1U_0402_16V7K
PCIE GTX_C_MRX_P0	C264	2	0.1U_0402_16V7K				

<12> PCIE GTX_C_MRX_P[0..15]	PCIE GTX_C_MRX_P[0..15]
<12> PCIE GTX_C_MRX_N[0..15]	PCIE GTX_C_MRX_N[0..15]
<12> PCIE MTX_C_GRX_P[0..15]	PCIE MTX_C_GRX_P[0..15]
<12> PCIE MTX_C_GRX_N[0..15]	PCIE MTX_C_GRX_N[0..15]



PCIE MTX_C_GRX_N15	AJ31	PCIE RX0P	PCIE RX0N
PCIE MTX_C_GRX_P15	AH31	PCIE RX1P	PCIE RX1N
PCIE MTX_C_GRX_N14	AH30	PCIE RX2P	PCIE RX2N
PCIE MTX_C_GRX_P14	AG30	PCIE RX3P	PCIE RX3N
PCIE MTX_C_GRX_N13	AG29	PCIE RX4P	PCIE RX4N
PCIE MTX_C_GRX_P13	AG28	PCIE RX5P	PCIE RX5N
PCIE MTX_C_GRX_N12	AE31	PCIE RX6P	PCIE RX6N
PCIE MTX_C_GRX_P12	AE31	PCIE RX7P	PCIE RX7N
PCIE MTX_C_GRX_N11	AE30	PCIE RX8P	PCIE RX8N
PCIE MTX_C_GRX_P11	AD30	PCIE RX9P	PCIE RX9N
PCIE MTX_C_GRX_N10	AD32	PCIE RX10P	PCIE RX10N
PCIE MTX_C_GRX_P10	AC32	PCIE RX11P	PCIE RX11N
PCIE MTX_C_GRX_N9	AC31	PCIE RX12P	PCIE RX12N
PCIE MTX_C_GRX_P9	AB31	PCIE RX13P	PCIE RX13N
PCIE MTX_C_GRX_N8	AB30	PCIE RX14P	PCIE RX14N
PCIE MTX_C_GRX_P8	AA30	PCIE RX15P	PCIE RX15N
PCIE MTX_C_GRX_N7	AA32		
PCIE MTX_C_GRX_P7	Y32		
PCIE MTX_C_GRX_N6	Y31		
PCIE MTX_C_GRX_P6	W31		
PCIE MTX_C_GRX_N5	W30		
PCIE MTX_C_GRX_P5	V30		
PCIE MTX_C_GRX_N4	V32		
PCIE MTX_C_GRX_P4	U32		
PCIE MTX_C_GRX_N3	U31		
PCIE MTX_C_GRX_P3	T31		
PCIE MTX_C_GRX_N2	T30		
PCIE MTX_C_GRX_P2	R30		
PCIE MTX_C_GRX_N1	R32		
PCIE MTX_C_GRX_P1	P32		
PCIE MTX_C_GRX_N0	P31		
PCIE MTX_C_GRX_P0	N31		



U9A

GPIO

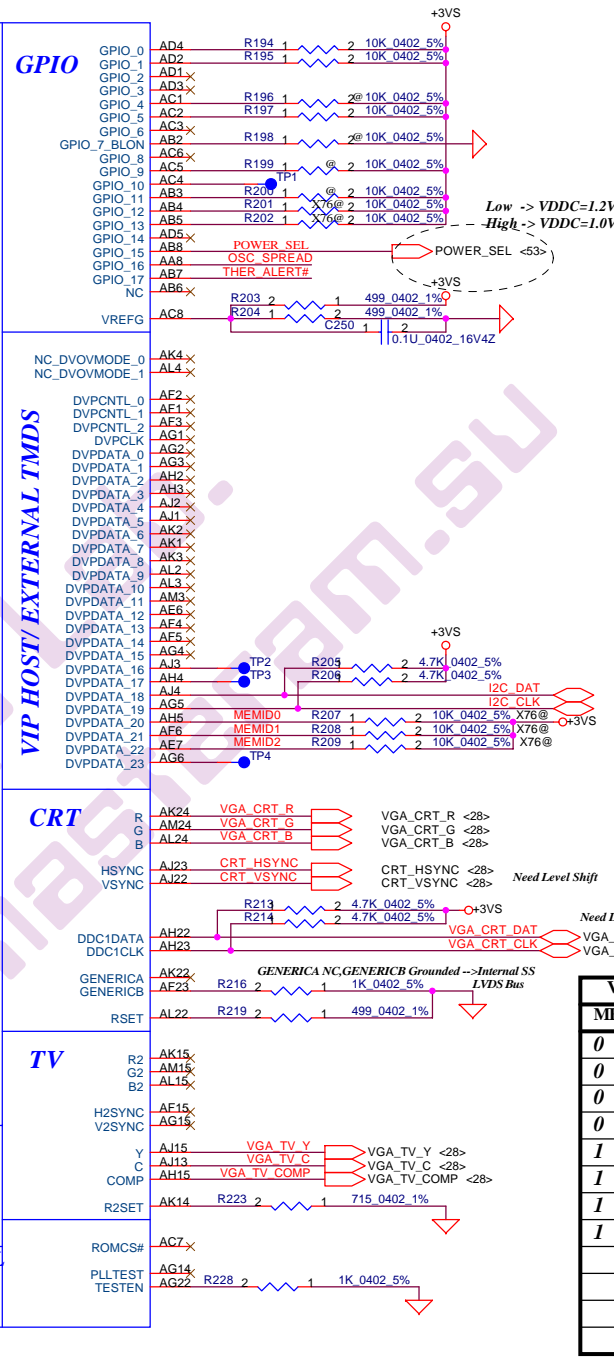
PCI EXPRESS

CRT

TV

THERMAL

XTAL



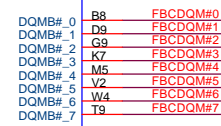
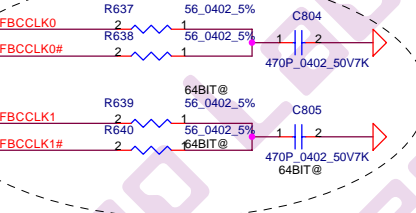
Straps: (Internal pull down)

Transmitter power saving enable	GPIO[0]	0: 50% TX output swing 1: Full TX output swing
Transmitter de-emphasis enable	GPIO[1]	0: TX de-emphasis disable 1: TX de-emphasis enable
Debug Access	GPIO[4]	0: OFF Pad must be available 1: ON
PLL_IBIAS_RD	GPIO[6,5]	Default : 01
ROM ID Config	GPIO[9, 13:11]	000X: No ROM, AP_SIZE=00 128M share 001X: No ROM memory AP_SIZE=01 256M share 010X: No ROM memory AP_SIZE=10 64M share 011X: No ROM memory AP_SIZE=11 Reserved

Vedio Memory Config. (VGA Internal PD)						
MEMID[2:0]	Size	Size	Vender	Chips	VGA	Frequence
0 0 0	64MB	16M16	Hynix	2		
0 0 1	64MB	16M16	Samsung	2		
0 1 0	128MB	16M16	Hynix	4		A-test
0 1 1	128MB	16M16	Samsung	4		
1 0 0	256MB	32M16	Hynix	4		A-test
1 0 1	256MB	32M16	Samsung	4		
1 1 0			Resreved			
1 1 1			Resreved			

TBD

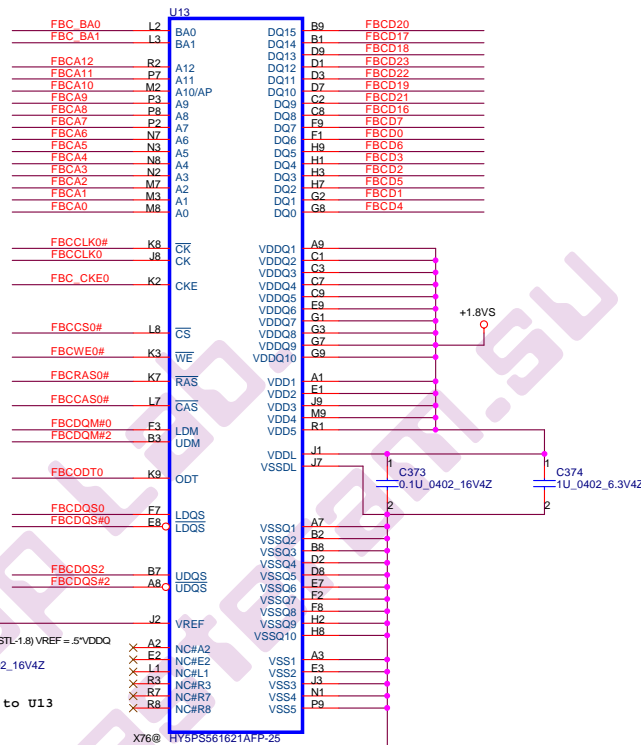
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/09/10	Deciphered Date	2006/09/10	SCHEMATIC, M/B LA-3151P	
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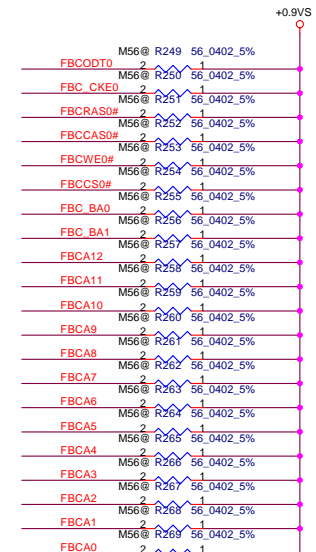
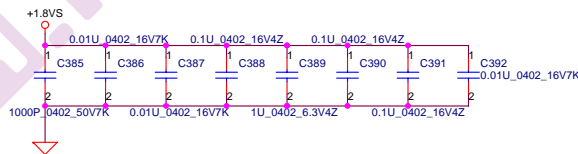
GDDR2

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2005/09/10	Deciphered Date	2006/09/10	Title SCHEMATIC, M/B LA-3151P		
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				Custom	40142	
Date:				日期	1, 三月 09, 2006	Sheet 18 of 55

11/03/05' SWAP NET



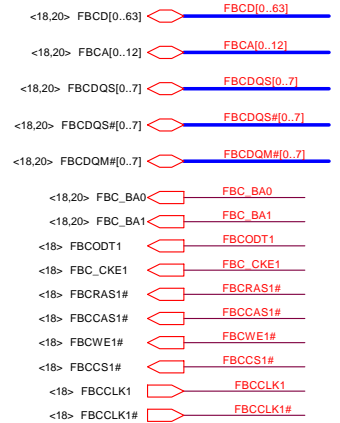
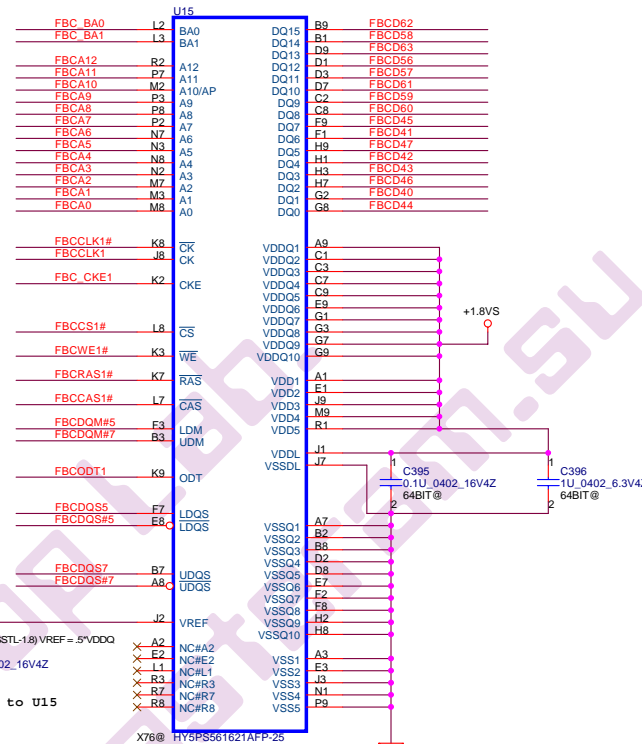
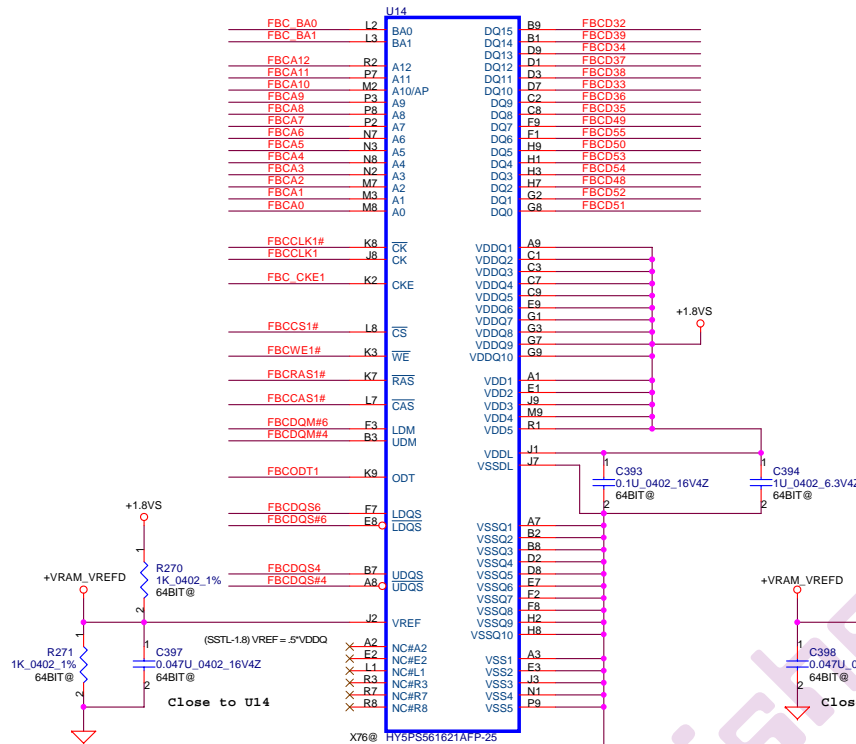
DDR2 BGA MEMORY



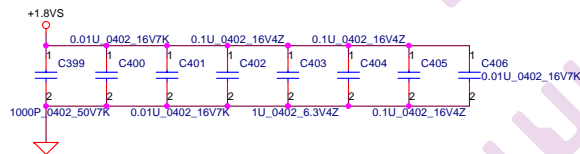
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				Custom	401412	B
				Date:	星期四, 三月 09, 2006	Sheet 20 of 55

11/03/05' SWAP NET

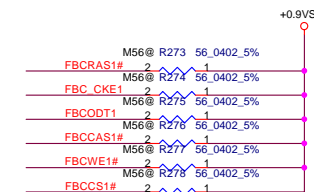
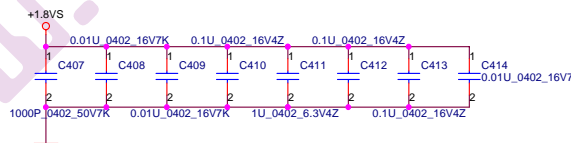
11/03/05' SWAP NET



DDR2 BGA MEMORY



DDR2 BGA MEMORY



M56 Only

PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO U600

<15> SBSRC_CLKP
<15> SBSRC_CLKN

A_MRX_STX_P0
A_MRX_STX_N0
A_MRX_STX_P1
A_MRX_STX_N1

C415 1 2 0.01U 0402 16V7K
C417 1 2 0.01U 0402 16V7K
C418 1 2 0.01U 0402 16V7K

A_MRX_C_STX_P0
A_MRX_C_STX_N0
A_MRX_C_STX_P1
A_MRX_C_STX_N1

R289 1 2 @ 49.9 0402 1% SB_TX2P
R290 1 2 @ 49.9 0402 1% SB_TX2N
R291 1 2 @ 49.9 0402 1% SB_TX2P
R292 1 2 @ 49.9 0402 1% SB_TX2N

A_MTX_C_SRX_P0
A_MTX_C_SRX_N0
A_MTX_C_SRX_P1
A_MTX_C_SRX_N1

R289 1 2 @ 49.9 0402 1% SB_TX2P
R290 1 2 @ 49.9 0402 1% SB_TX2N
R291 1 2 @ 49.9 0402 1% SB_TX2P
R292 1 2 @ 49.9 0402 1% SB_TX2N

A_MTX_C_SRX_P0
A_MTX_C_SRX_N0
A_MTX_C_SRX_P1
A_MTX_C_SRX_N1

R289 1 2 @ 49.9 0402 1% SB_TX2P
R290 1 2 @ 49.9 0402 1% SB_TX2N
R291 1 2 @ 49.9 0402 1% SB_TX2P
R292 1 2 @ 49.9 0402 1% SB_TX2N

A_MTX_C_SRX_P0
A_MTX_C_SRX_N0
A_MTX_C_SRX_P1
A_MTX_C_SRX_N1

R289 1 2 @ 49.9 0402 1% SB_TX2P
R290 1 2 @ 49.9 0402 1% SB_TX2N
R291 1 2 @ 49.9 0402 1% SB_TX2P
R292 1 2 @ 49.9 0402 1% SB_TX2N

A_MTX_C_SRX_P0
A_MTX_C_SRX_N0
A_MTX_C_SRX_P1
A_MTX_C_SRX_N1

R289 1 2 @ 49.9 0402 1% SB_TX2P
R290 1 2 @ 49.9 0402 1% SB_TX2N
R291 1 2 @ 49.9 0402 1% SB_TX2P
R292 1 2 @ 49.9 0402 1% SB_TX2N

FOR SB600 VCC_SB= 1.2V
FOR SB460 VCC_SB= 1.8V

R294 CALRP: SB600=562R 1% SB460=150R 1%
R295 CALRN: SB600=2.05K 1% SB460=150R 1%
R296 CALRN: SB600=0R 1% SB460=4.12K 1%

+1.8VS
KC FBM-L11-201209-221LMAT_0805

C608 AND C609 CLOSE
TO U600,U29

10U_0805_10V4Z
1U_0402_6.3V4Z

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

PCIE_VDDR

+1.8VS
KC FBM-L11-201209-221LMAT_0805

C423 C424 C425 C426 C427 C428

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

R303 20M_0603_5%
C429 10P_0402_50V8K

22U_0805_6.3V6M 1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

1U_0402_6.3V4Z

C429 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

C430 10P_0402_50V8K
R288 20M_0603_5%

32.768KHZ_12.5PF_6H03200468

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

32K_X1

32K_X2

SB460

Part 1 of 4

PCI EXPRESS INTERFACE

PCI INTERFACE

LPC

RTC

CPU

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

PCI CLK#

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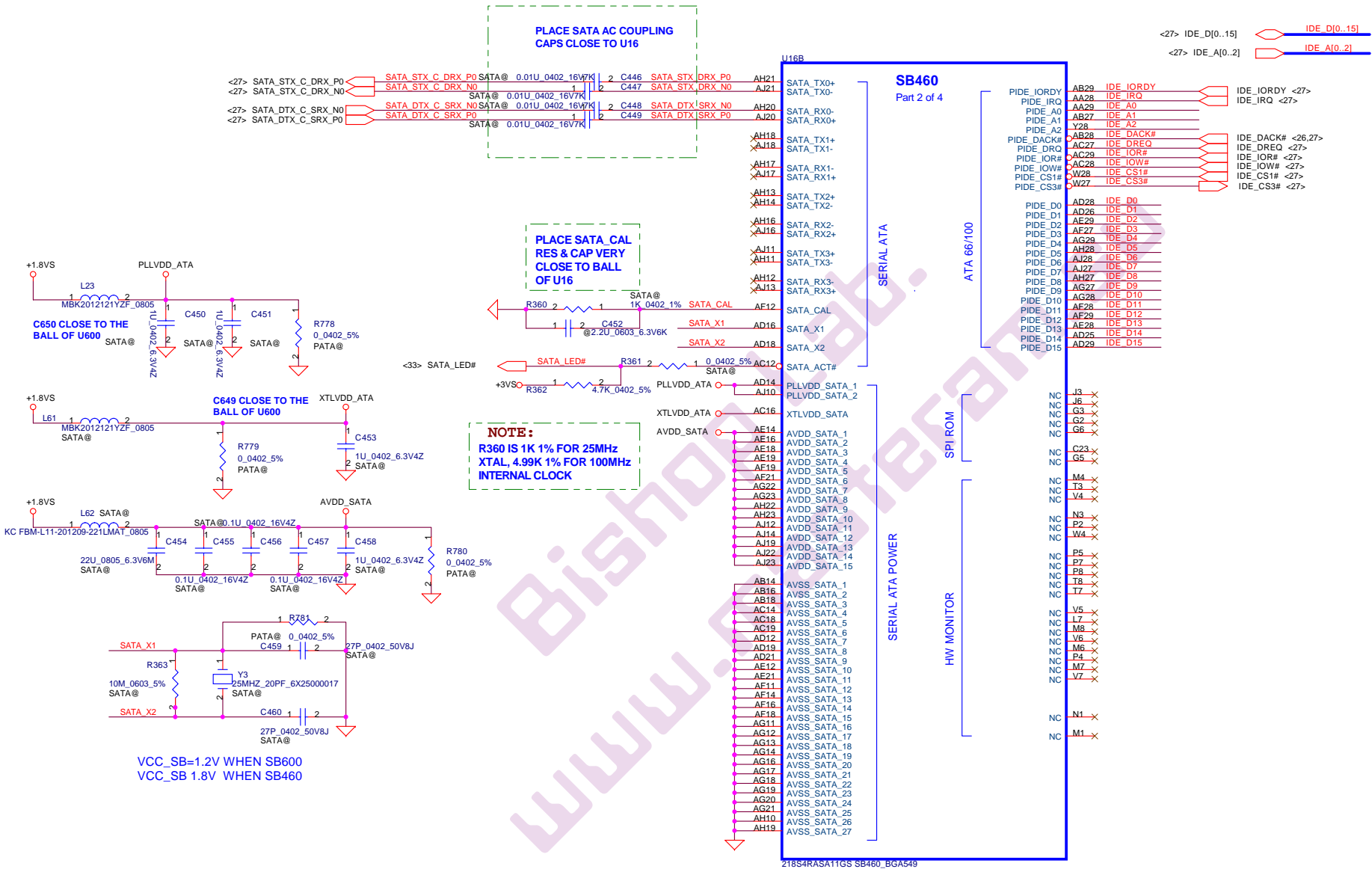
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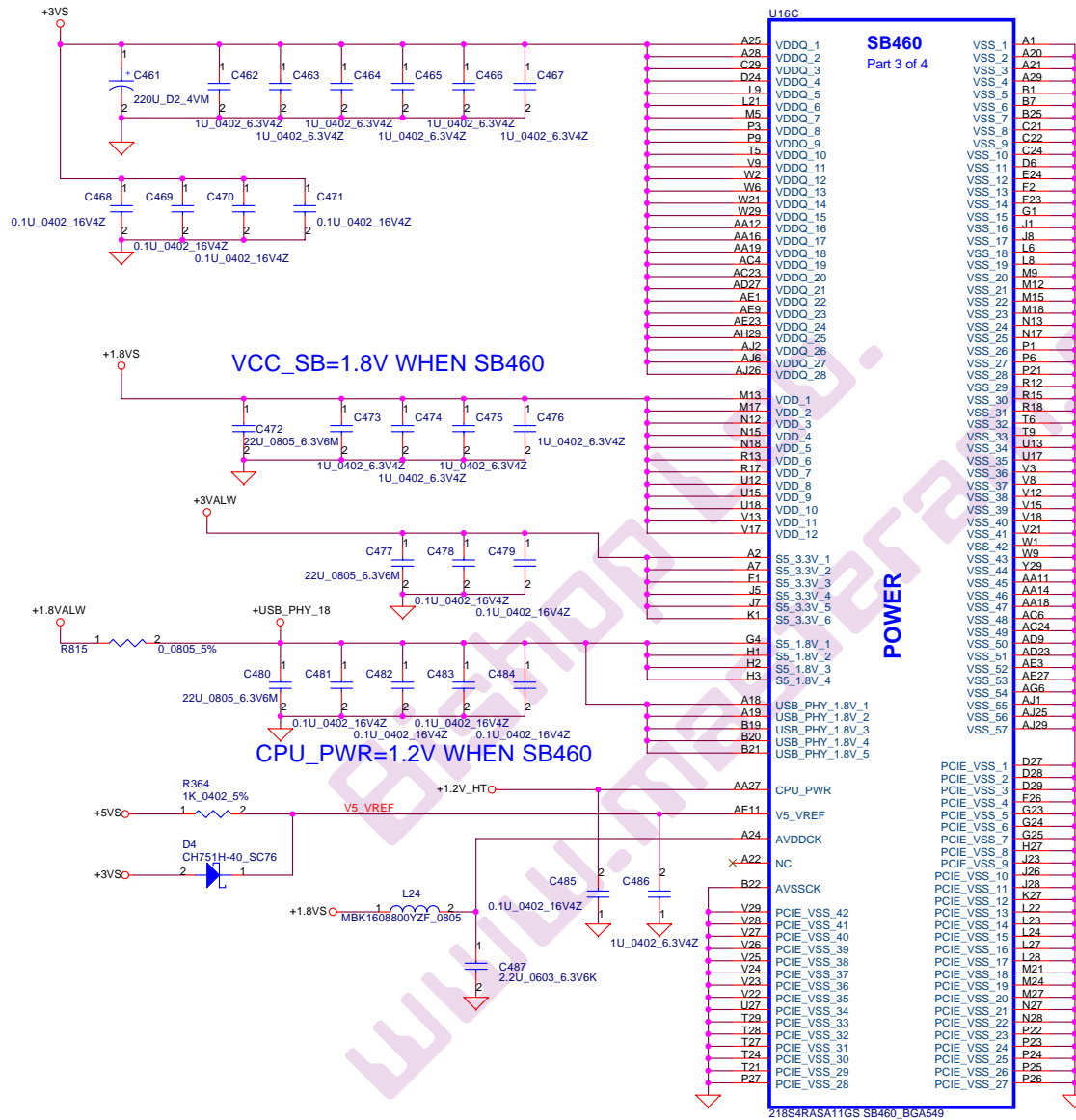
PCI CLK#

PCI CLK#

PCI CLK#

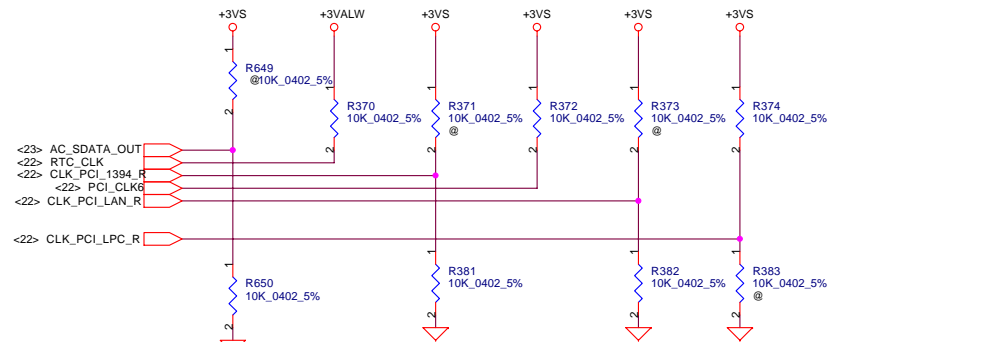
PCI CLK





REQUIRED STRAPS

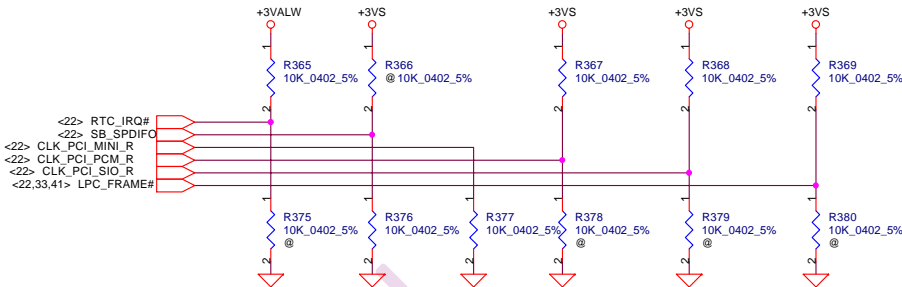
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



		SB600				SB460	
PULL HIGH	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC	PCI_CLK0 CLK_PCI_LAN
	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCI_CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]		

NOTE: R365 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB460
TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY



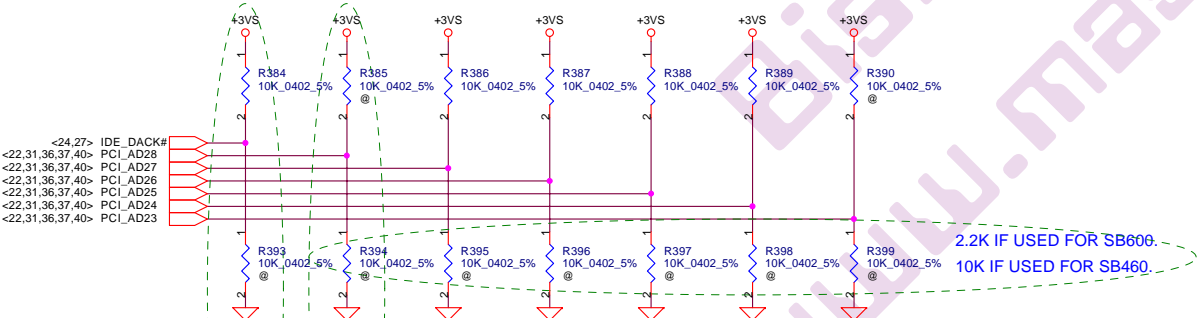
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
	RTC_IRQ#	SB_SPDIFO	CLK_PCI_MINI	CLK_PCI_PCM	CLK_PCI_SIO	LPC_FRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR
SB460,
PCI_AD23 IS
RESERVED

<24> IDE_D[0..15] IDE_D[0..15]
<24> IDE_A[0..2] IDE_A[0..2]

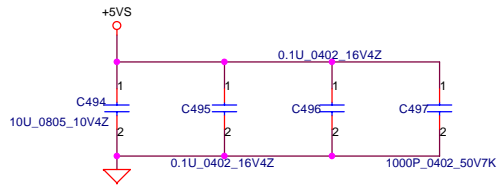


Diagram illustrating the SATA connector pinout (J17) for the SATA@ OCTEK SAT-22SG16-NR (NEW) device. The diagram shows the connection of SATA signals and power pins to the device's internal components.

SATA Signals:

- SATA STX_C, DRX_P0** (Pin 1)
- SATA STX_C, DRX_N0** (Pin 2)
- SATA DTX_C, SRX_N0** (Pin 5)
- SATA DTX_C, SRX_P0** (Pin 6)

Power and Ground:

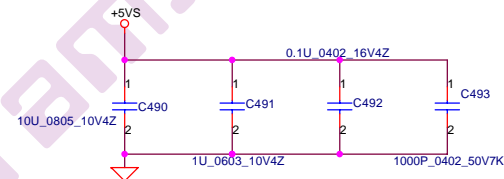
- GND** (Pin 7)
- VCC3.3** (Pin 8)
- VCC3.3** (Pin 9)
- VCC3.3** (Pin 10)
- GND** (Pin 11)
- GND** (Pin 12)
- GND** (Pin 13)
- VCC5** (Pin 14)
- VCC5** (Pin 15)
- VCC5** (Pin 16)
- GND** (Pin 17)
- RESERVED** (Pin 18)
- GND** (Pin 19)
- VCC12** (Pin 20)
- VCC12** (Pin 21)
- VCC12** (Pin 22)

Internal Components:

- R816** (Resistor, 0.0805, 5%) connected to **+3VS** (Pin 1)
- R817** (Resistor, 0.0805, 5%) connected to **+5VS** (Pin 1)

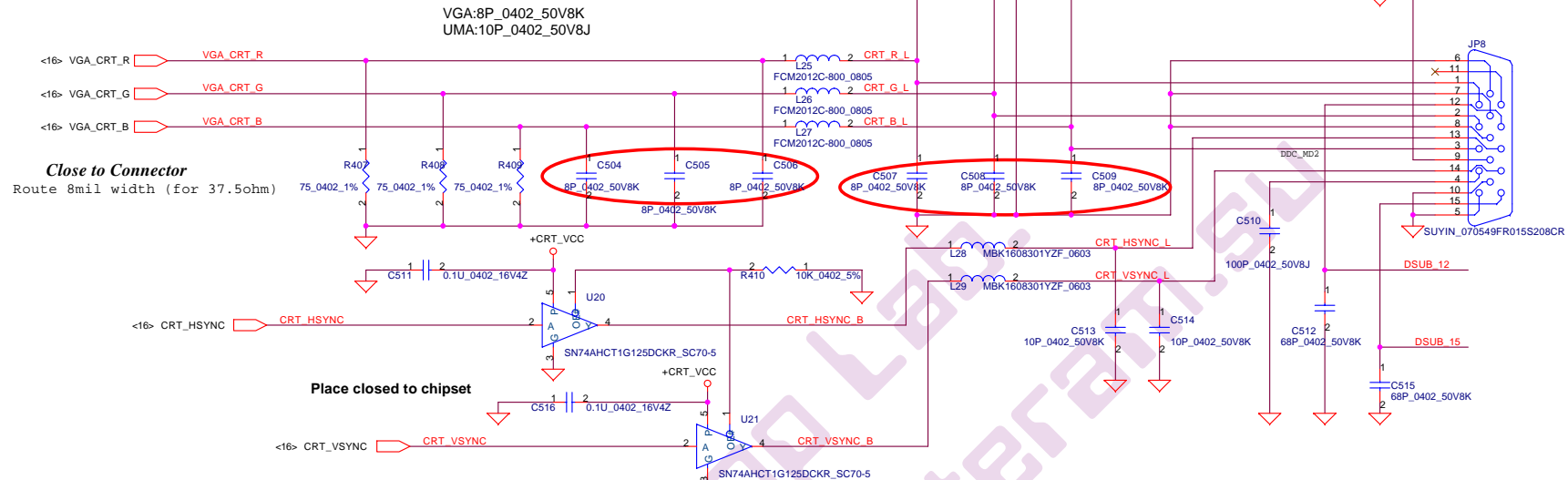
Notes:

- Modify 11/07 for EMI

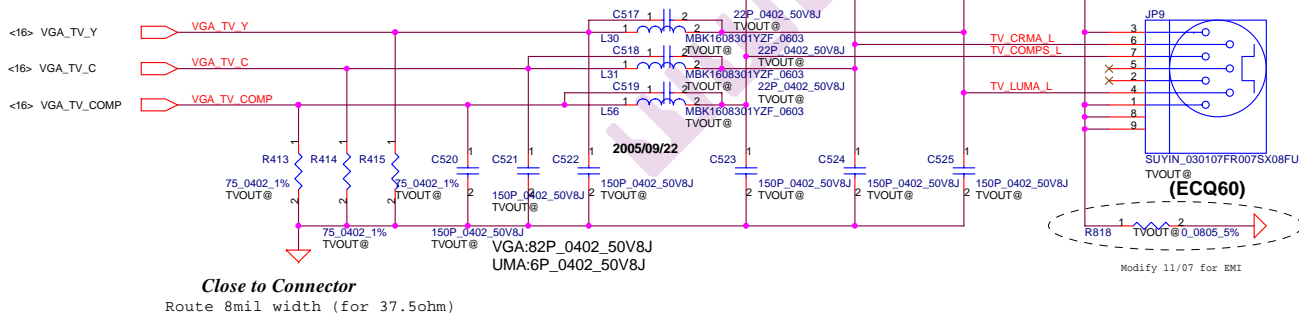
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CRT Connector



TV-OUT Conn.



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				Date: 星期四, 三月 09, 2006	Sheet 28 of 55

5 4 3 2 1

D

C

B

A

LCD POWER CIRCUIT

07/07/'05

Modify 11/22

W=60mils

W=60mils

LCD/PANEL BD. Conn.

(SAME AS ACES_87216-4016)

Security Classification: Compal Secret Data

Issued Date: 2005/03/08

Deciphered Date: 2006/03/08

Title: SCHEMATIC, MB LA-3151P

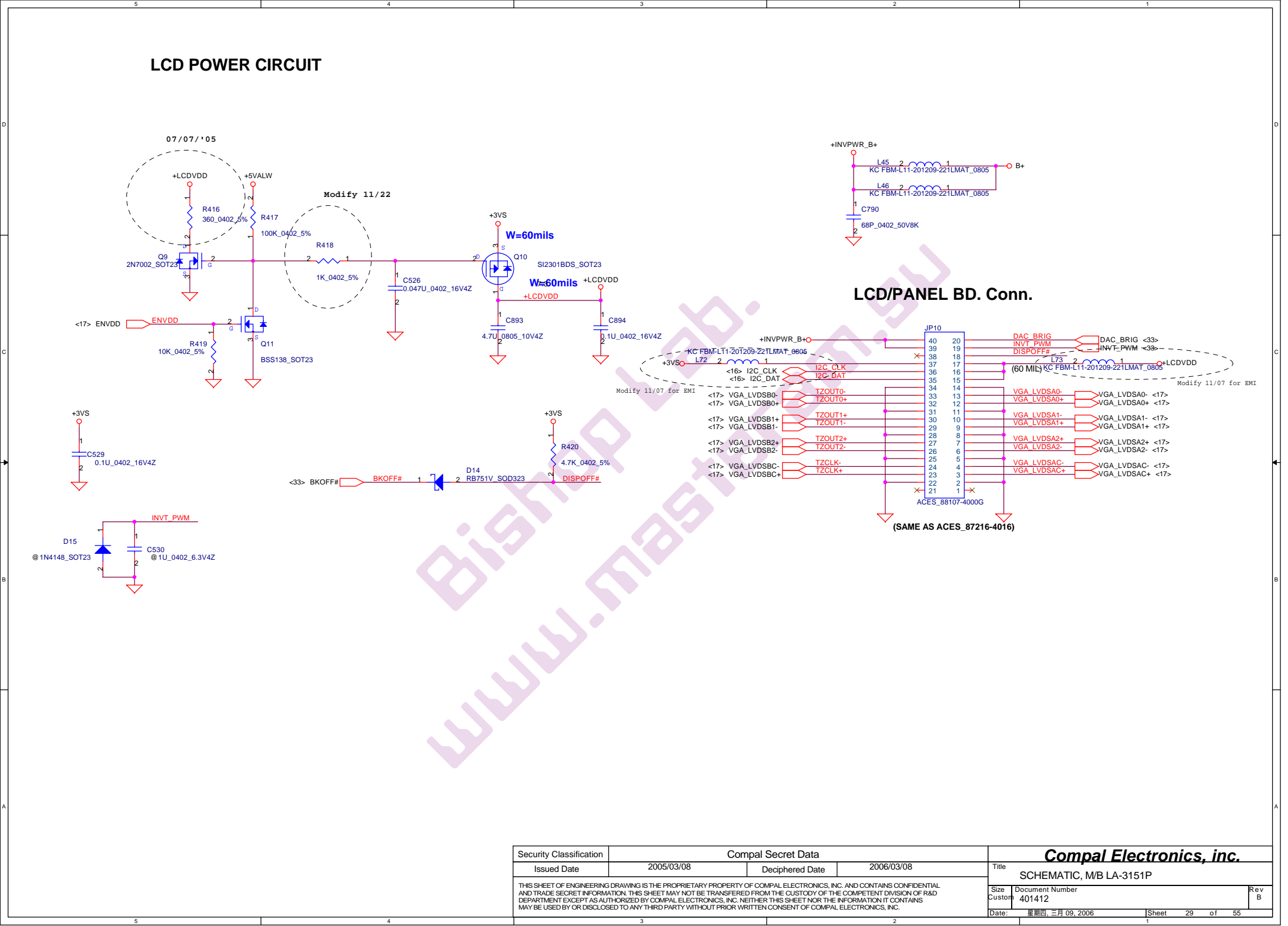
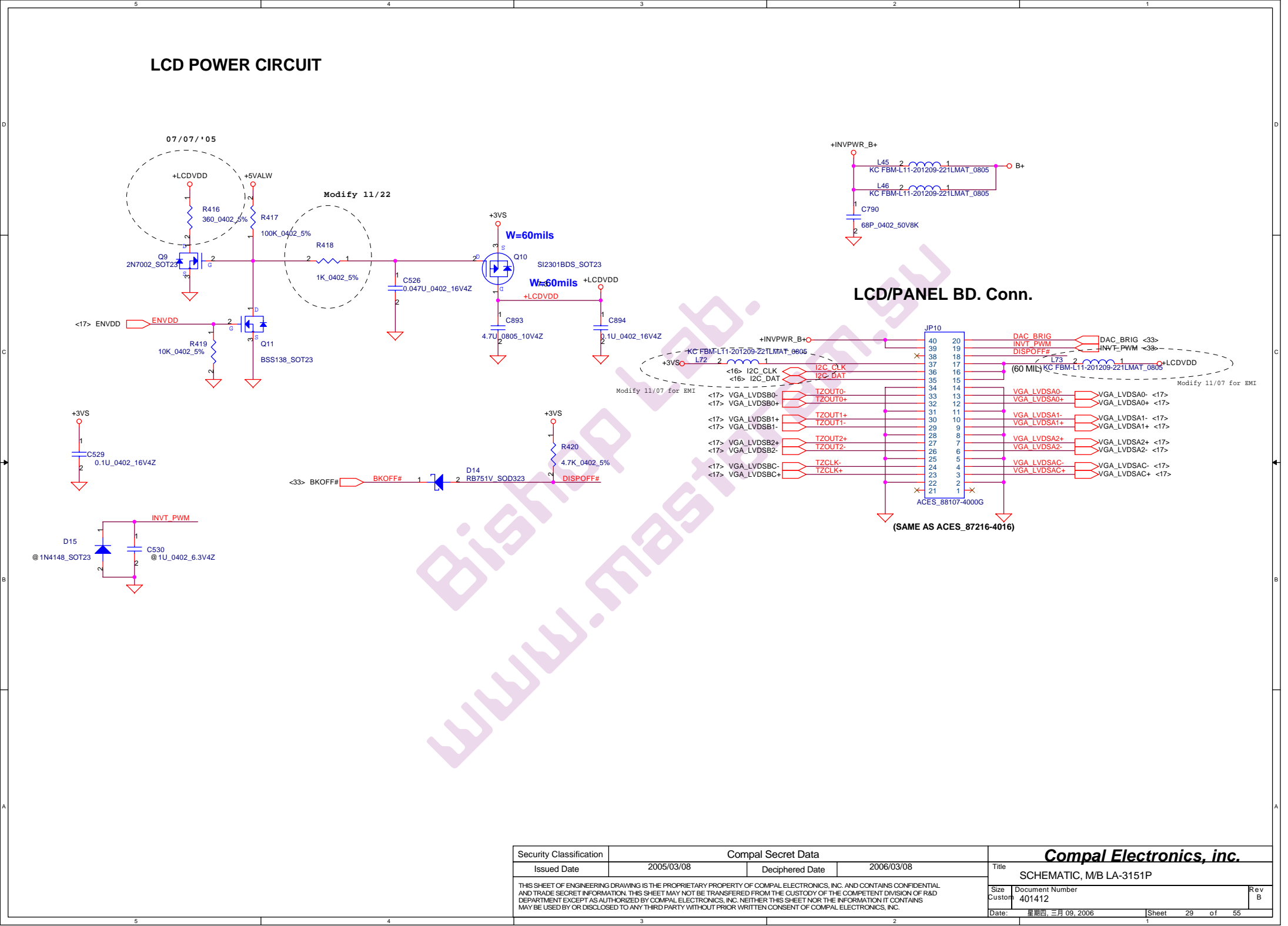
Size: Custom

Document Number: 401412

Date: 星期四, 三月 09, 2006

Sheet: 29 of 55

Rev: B



5 4 3 2 1

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B

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LCD POWER CIRCUIT

07/07/'05

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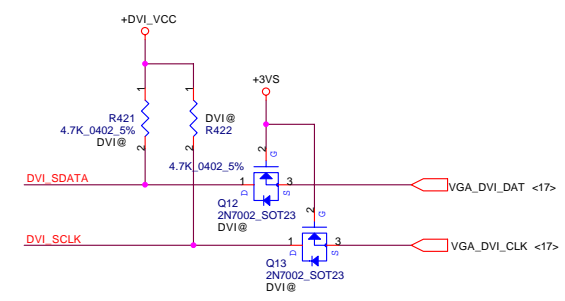
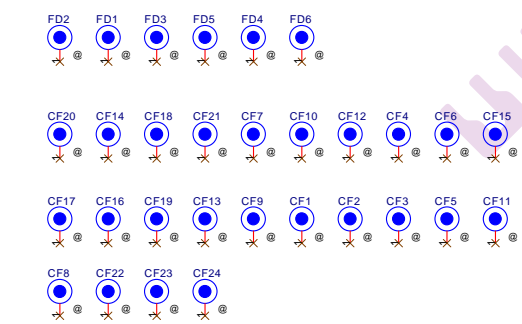
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Document Number: 401412

Date: 星期四, 三月 09, 2006

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				B	401412	B
				Date:	星期三, 三月 09, 2006	Sheet 30 of 55

<22,26,36,37,40> PCI_AD[0..31]

PCI AD0 104
PCI AD1 103
PCI AD2 102
PCI AD3 98
PCI AD4 97
PCI AD5 96
PCI AD6 95
PCI AD7 93
PCI AD8 90
PCI AD9 87
PCI AD10 89
PCI AD11 86
PCI AD12 85
PCI AD13 83
PCI AD14 82
PCI AD15 79
PCI AD16 59
PCI AD17 58
PCI AD18 57
PCI AD19 55
PCI AD20 53
PCI AD21 50
PCI AD22 49
PCI AD23 47
PCI AD24 43
PCI AD25 42
PCI AD26 40
PCI AD27 39
PCI AD28 37
PCI AD29 36
PCI AD30 34
PCI AD31 33

<22,36,37,40> PCI_CBE#0
<22,36,37,40> PCI_CBE#1
<22,36,37,40> PCI_CBE#2
<22,36,37,40> PCI_CBE#3

PCI_AD17 1
R434 2 100_0402_5%

<22,36,37,40> PCI_PAR 76
<22,36,37,40> PCI_FRAME# 61
<22,36,37,40> PCI_IRDY# 63
<22,36,37,40> PCI_TRDY# 67
<22,36,37,40> PCI_DEVSEL# 68
<22,36,37,40> PCI_STOP# 69

<22,36,37,40> PCI_PERR# 75
<22,36,37> PCI_SERR# 29
<22> PCI_REQ#3 30
<22> PCI_GNT#3 25

<22> PCI_PIRQ# 31
<33> LAN_PME# 27
<22,36,37,39,40> PCI_RST# 28

<22> CLK_PCI_LAN 65
<22,36,41> PM_CLKRUN# 65

CLK_PCI_LAN 1
R786 2 10_0402_5%

C911 1 18P_0402_50V8J

GND/VSS 4
GND/VSS 17
GND/VSS 128

GND/VSSPST 21
GND/VSSPST 38
GND/VSSPST 51
GND/VSSPST 66
GND/VSSPST 81
GND/VSSPST 91
GND/VSSPST 101
GND/VSSPST 119

GND 35
GND 52
GND 80
GND 100

RTL8110SBL change to Ver.D

U22

AD0

AD1

AD2

AD3

AD4

AD5

AD6

AD7

AD8

AD9

AD10

AD11

AD12

AD13

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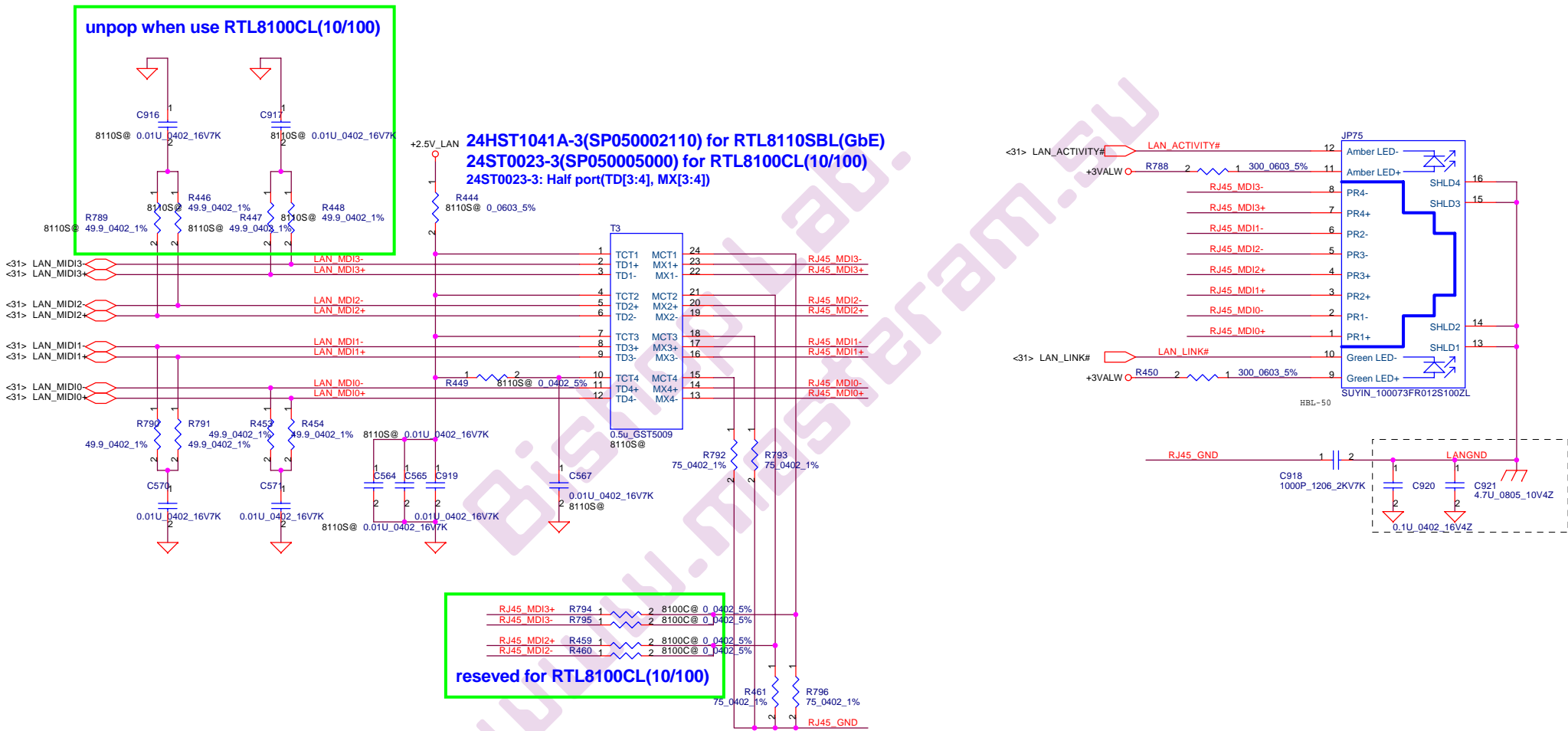
AD283

AD284

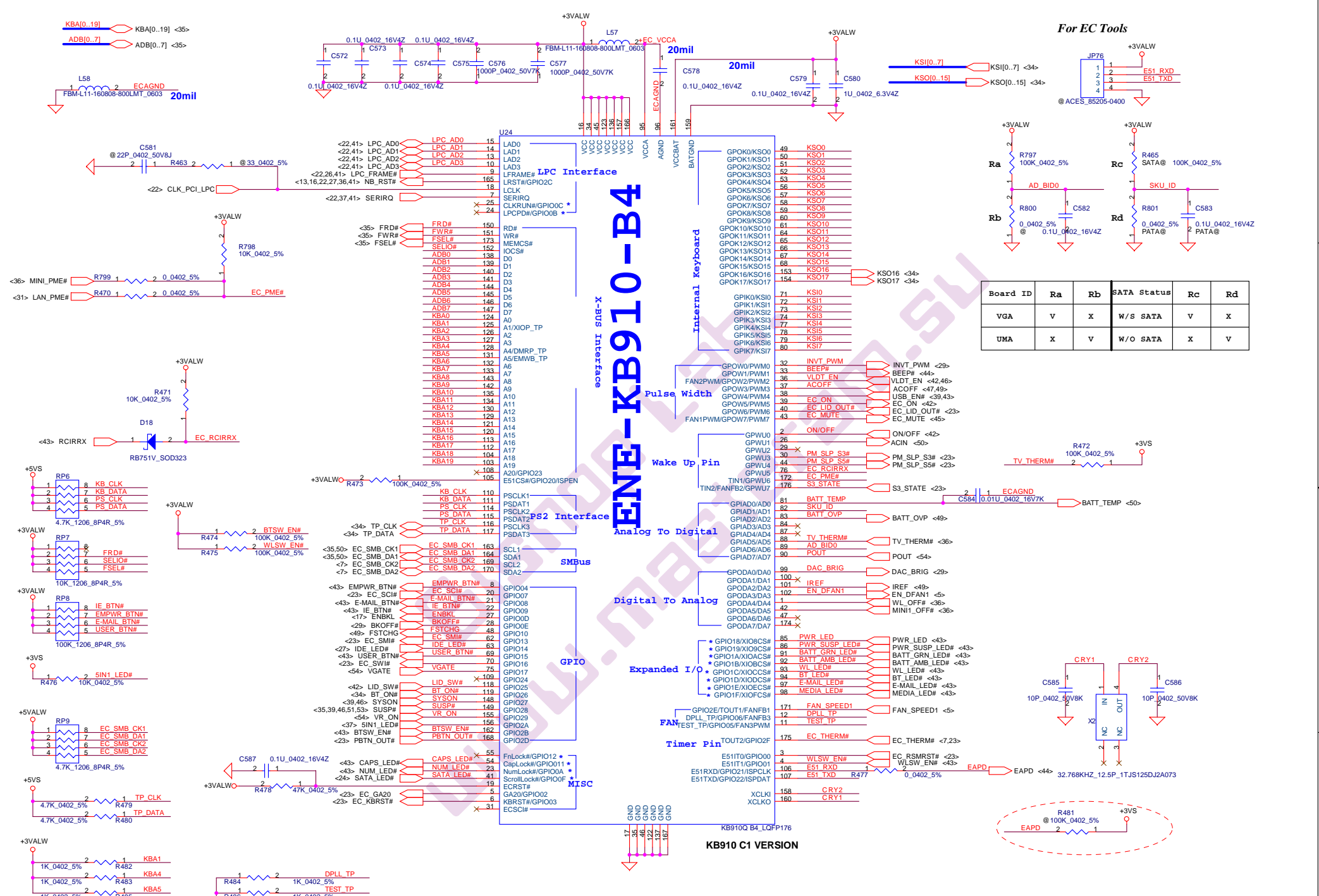
AD285

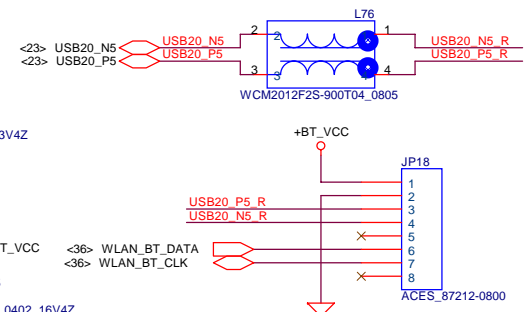
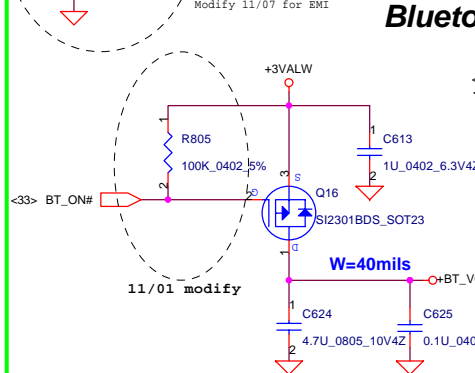
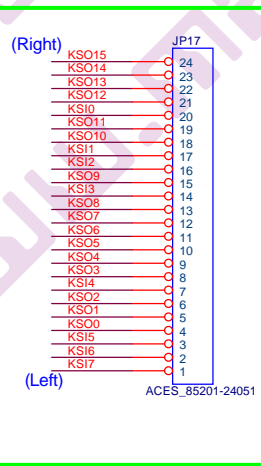
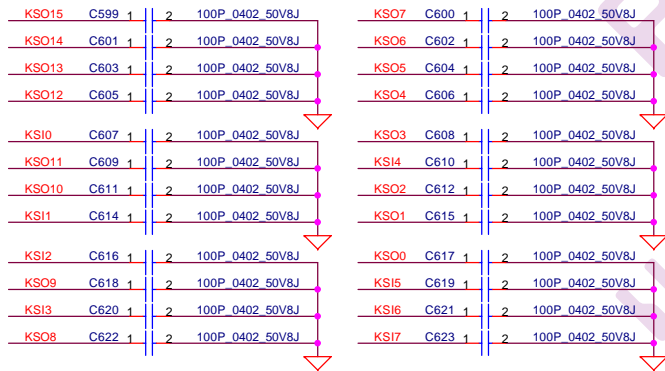
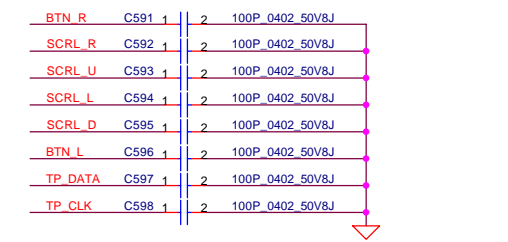
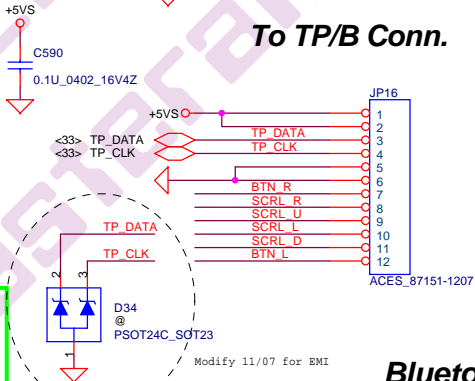
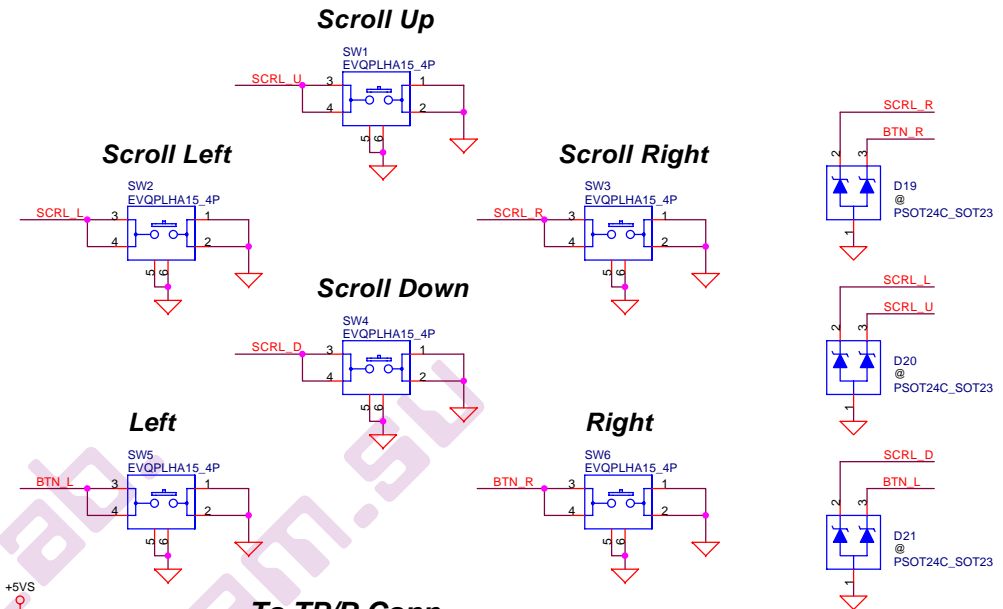
AD286

LAN RTL8110SBL/RTL8100CL





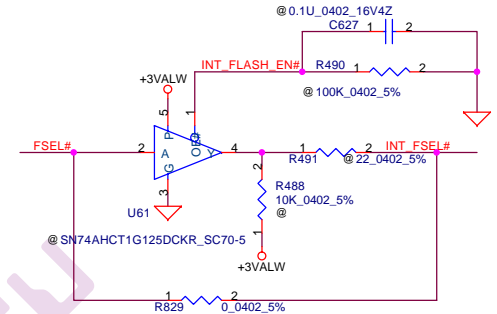
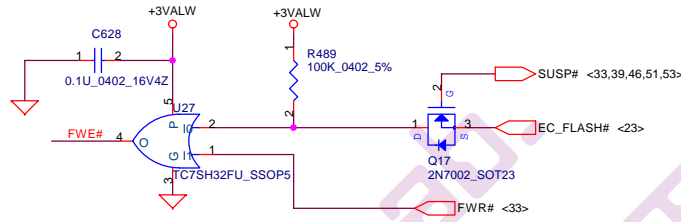
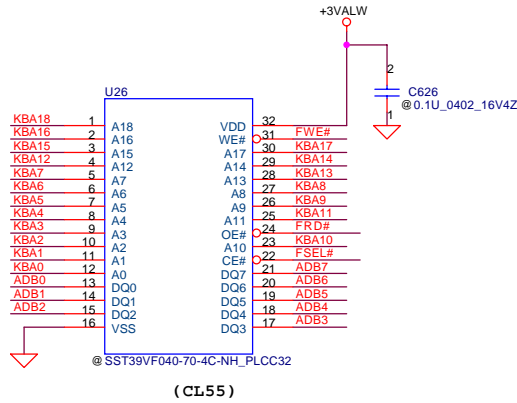
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		Size B	Document Number						Rev B
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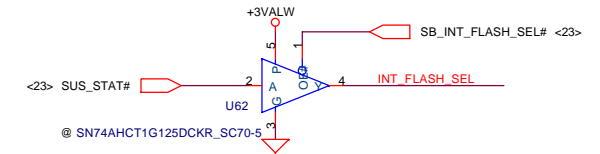


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						Size Custom
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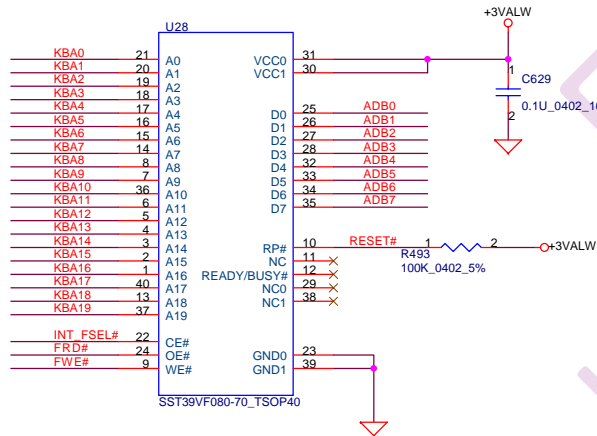
<33> KBA[0..19]  KBA[0..19]
<33> ADB[0..7]  ADB[0..7]



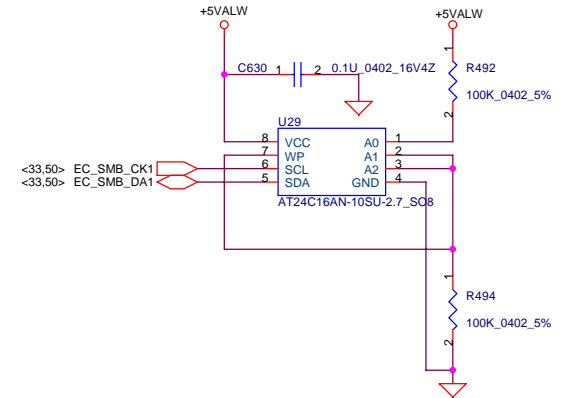
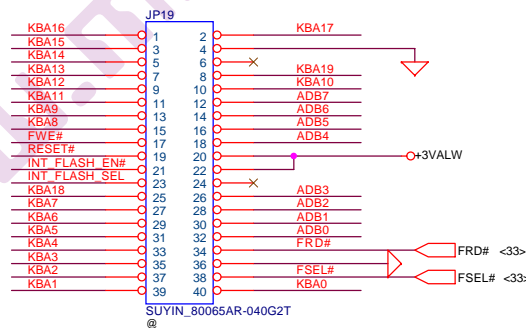
FOR DEBUG ONLY



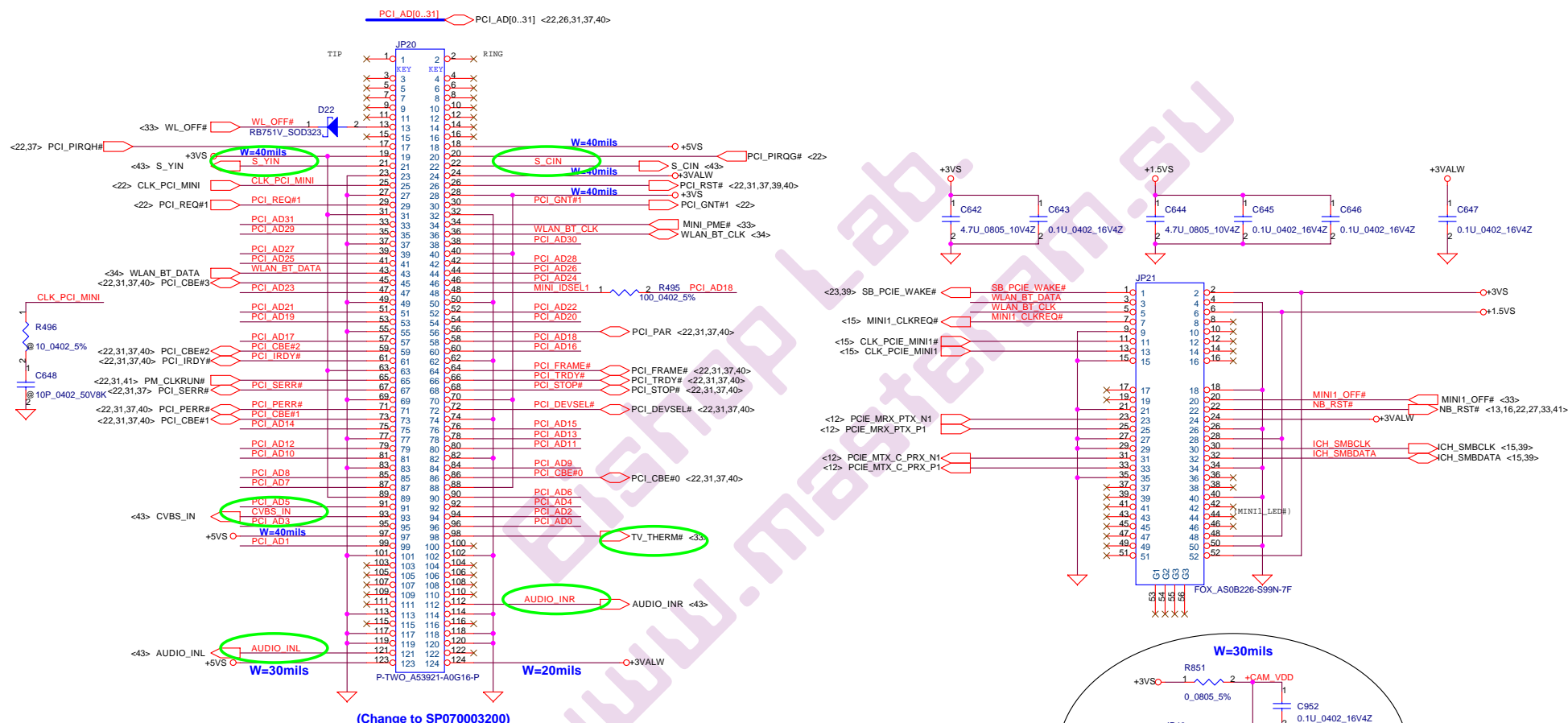
1MB Flash ROM



1MB Flash ROM

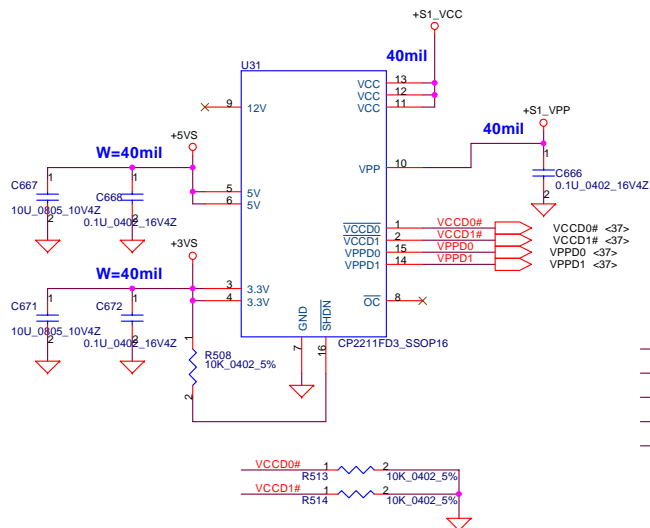


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Date: 星期四, 三月 09, 2006				Sheet	35	of 55

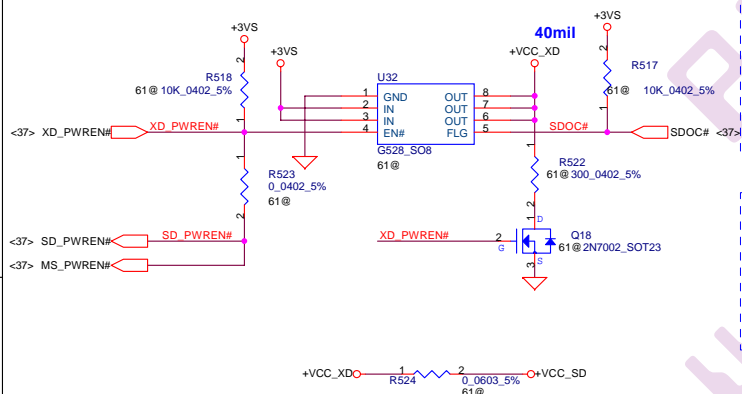


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

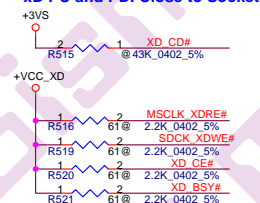
PCMCIA Power Control



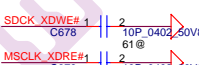
SD/MS Power Control
XD Power Control



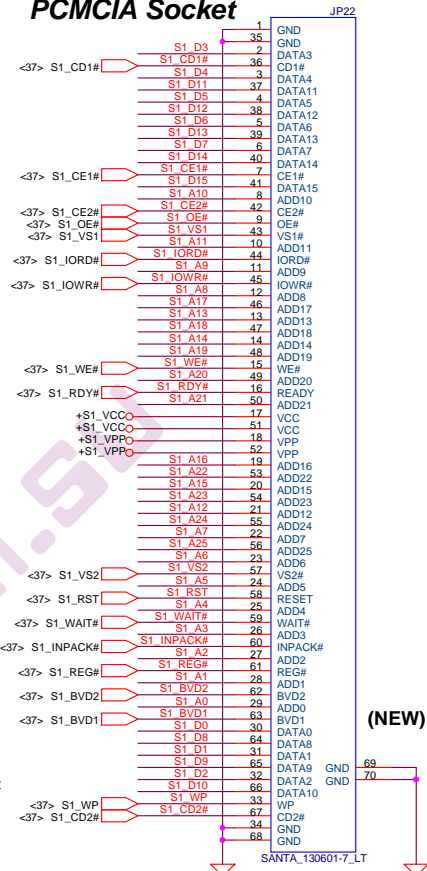
xD PU and PD. Close to Socket



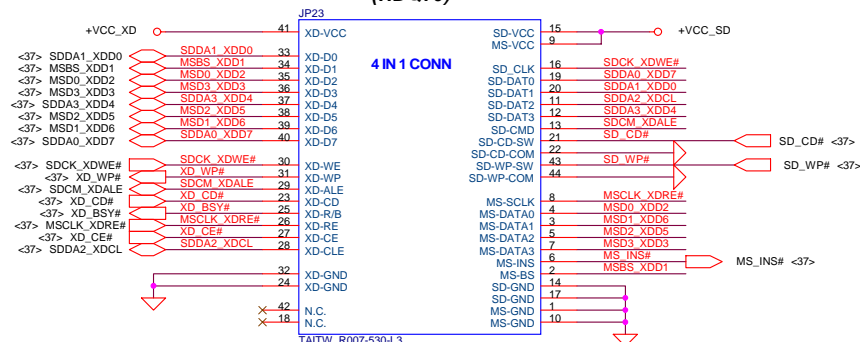
Reserve for SD,MS CLK.
Close to Socket



PCMCIA Socket

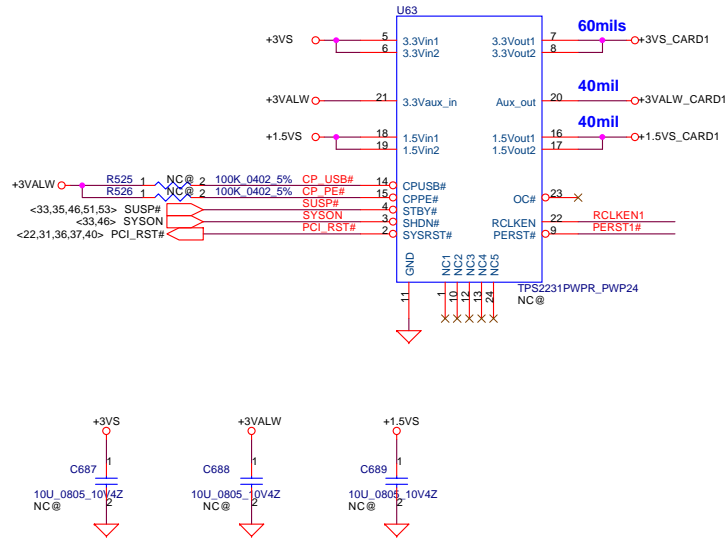


4 IN 1 Socket (HDQ70)

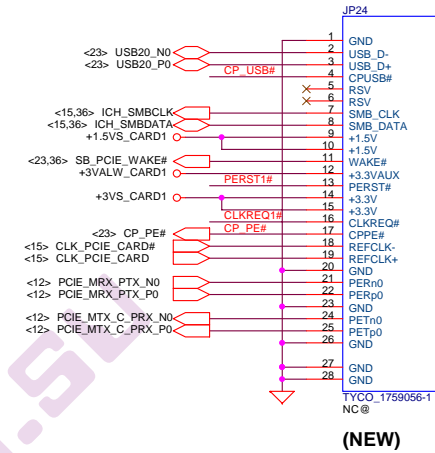


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				Size	Document Number	Rev B
				401412		
Date: 華語日, 三月 09, 2006				Sheet	38	of 55

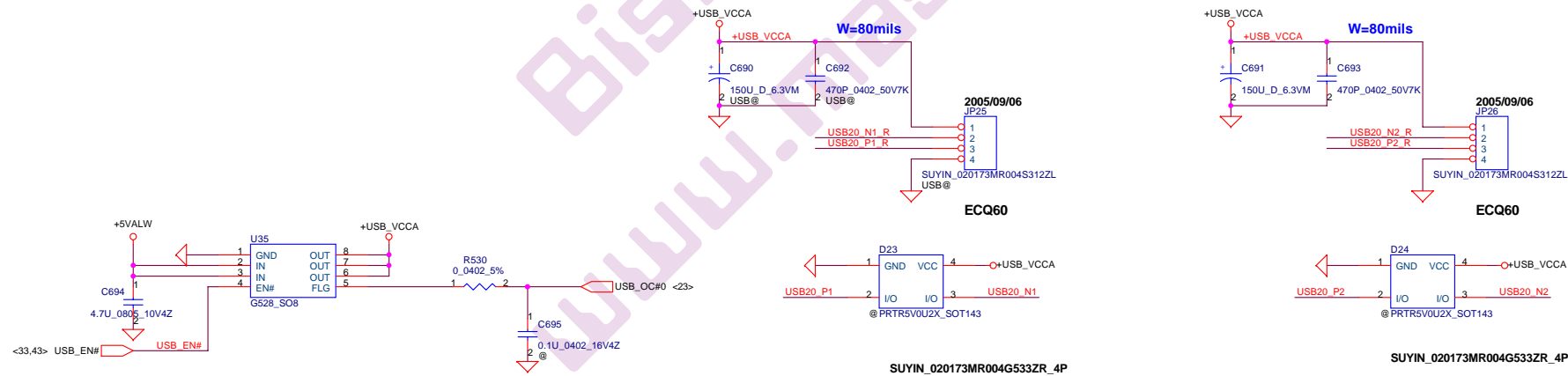
New Card Power Switch



New Card Socket (Left)



USB CONN. 1 & 2



Security Classification

Compal Secret Data

Issued Date 2005/06/20

Deciphered Date 2006/06/20

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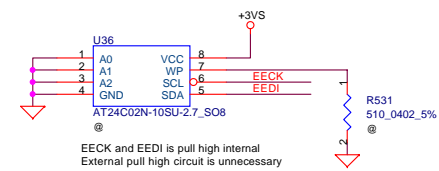
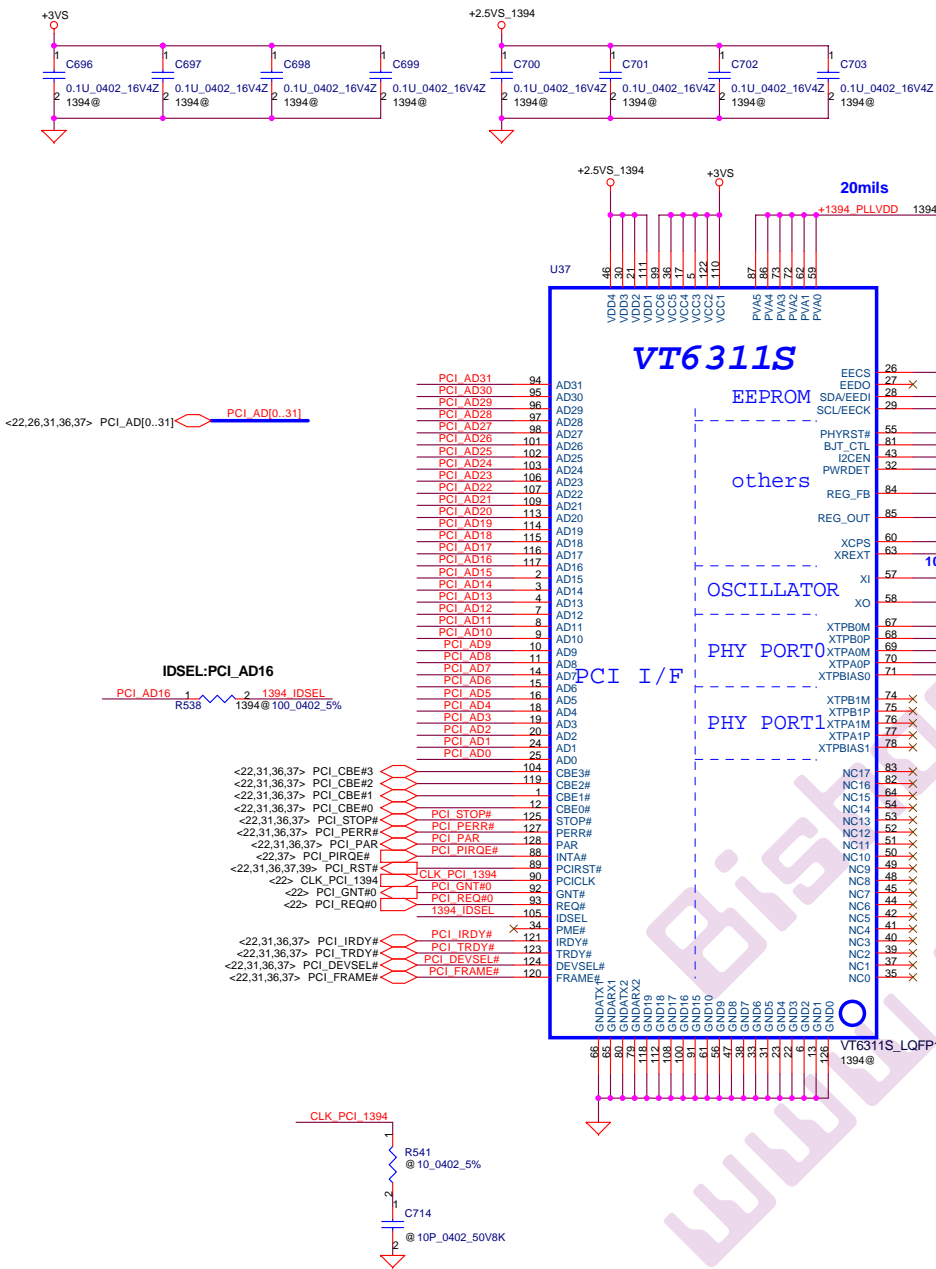
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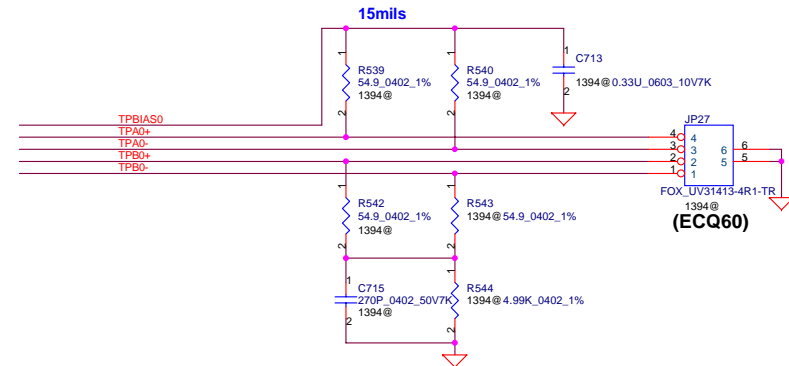
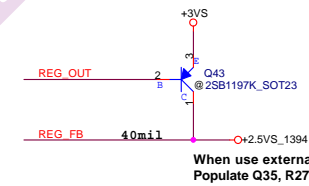
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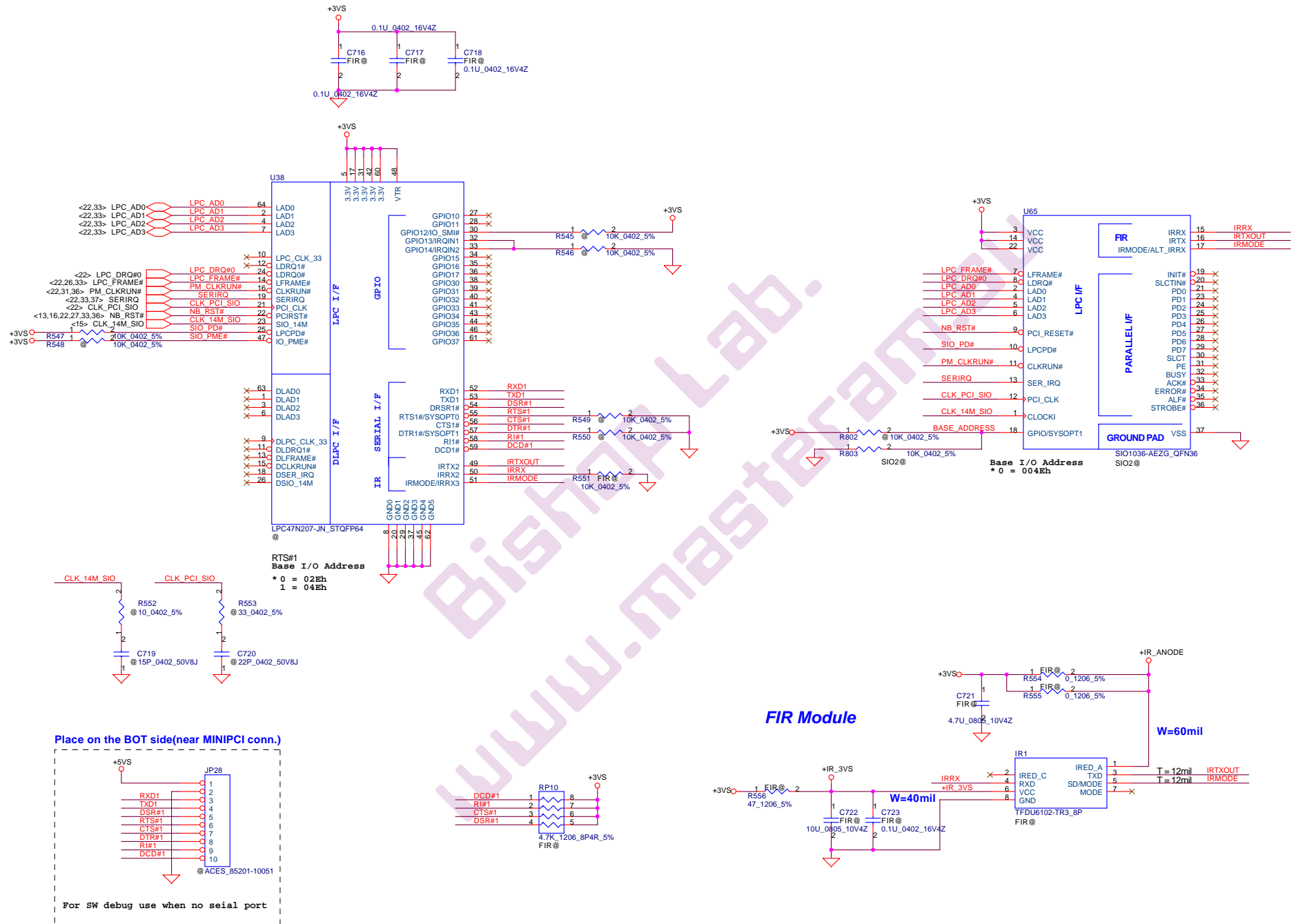


When use external EEPROM
Populate U14, R246, R253
Un-populate R261



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SUPER I/O SMsC LPC47N207



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note: T1 minimum 15ms, T2 minimum 15ms
 SUSP# goes to low after SB_PWRGD down.

Timing diagram for the 1.8V power-up sequence. The diagram shows the relationship between VLDLT_EN, NB_PWRGD, SB_PWRGD, and SUSP# signals relative to a +1.8V supply. VLDLT_EN is high during the initial power-up. NB_PWRGD and SB_PWRGD are low until the power is stable. SUSP# is high until the power is stable. The diagram is divided into two regions by vertical dashed lines labeled T1 and T2. T1 marks the point where VLDLT_EN falls and NB_PWRGD rises. T2 marks the point where SB_PWRGD rises and SUSP# falls.

Power Button

Bottom Side

TOP Side

J2 2 1 @JOPEN

J3 2 1 @JOPEN

+3VALW

R562 100K_0402_5%

D25

DAN202U_SC70

ON/OFFBTN#

ON/OFF <33>

51ON#

51ON# <47>

C727 1000P_0402_50V7K

D27 RLZ20A_LL34

EC_ON

EC_ON <33>

R564 10K_0402_5%

Q44 2N7002_SOT23

Lid Switch

Change P/N : SN111000207

SW7

MPU-101-81_4P

R563
100K_0402_5%

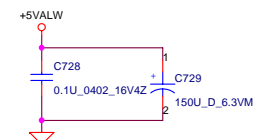
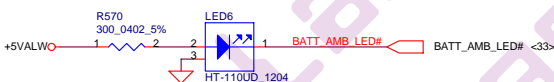
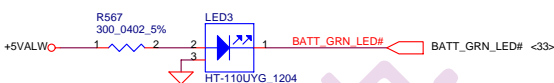
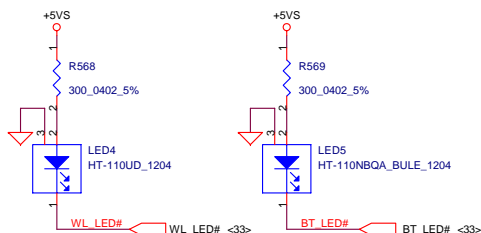
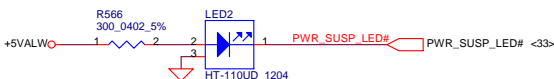
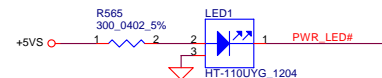
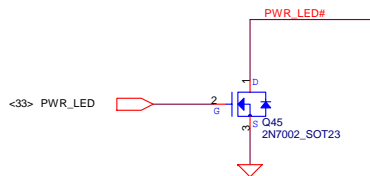
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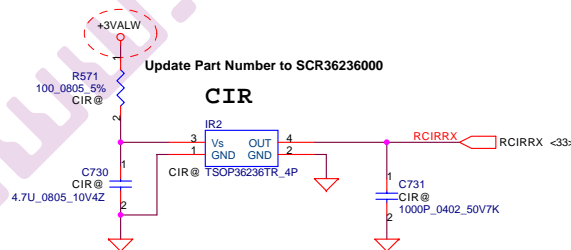
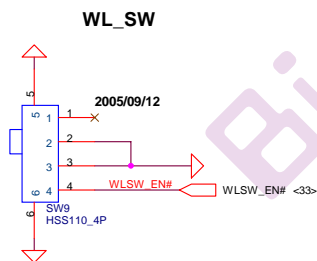
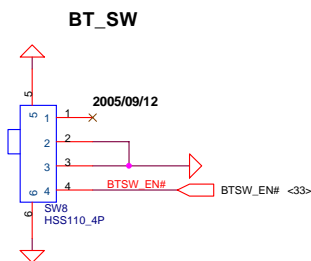
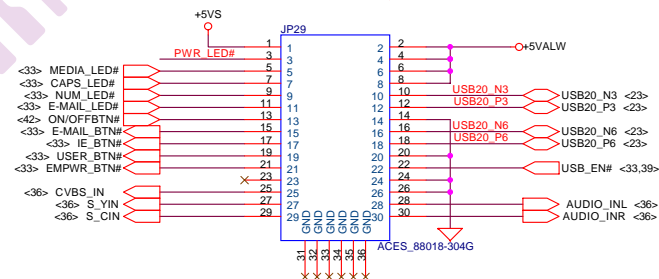
D26
@
PSOT24C_SOT23

2005/09/04

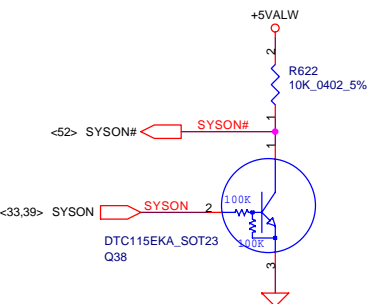
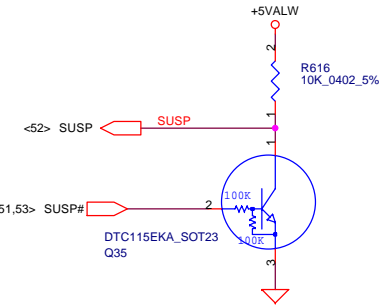
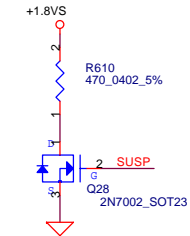
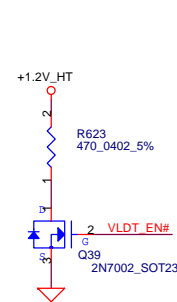
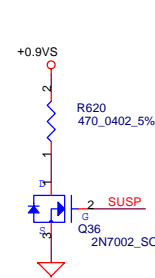
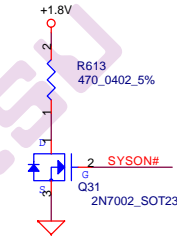
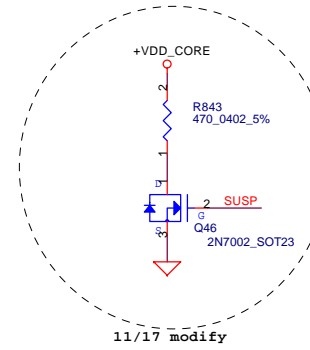
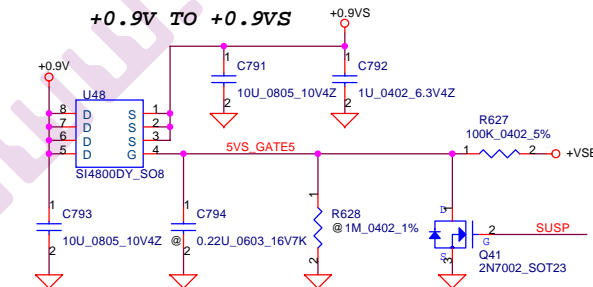
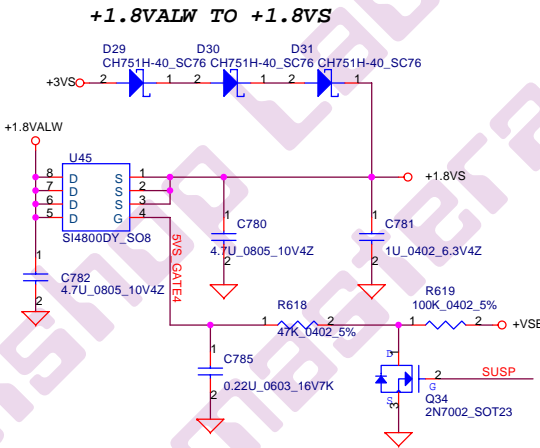
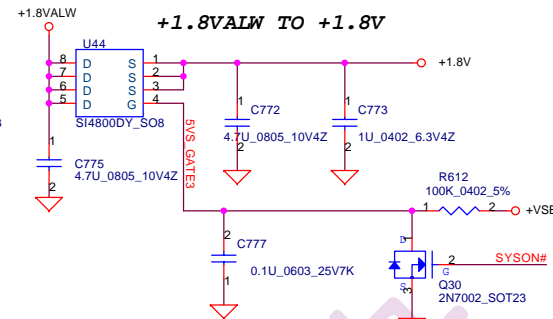
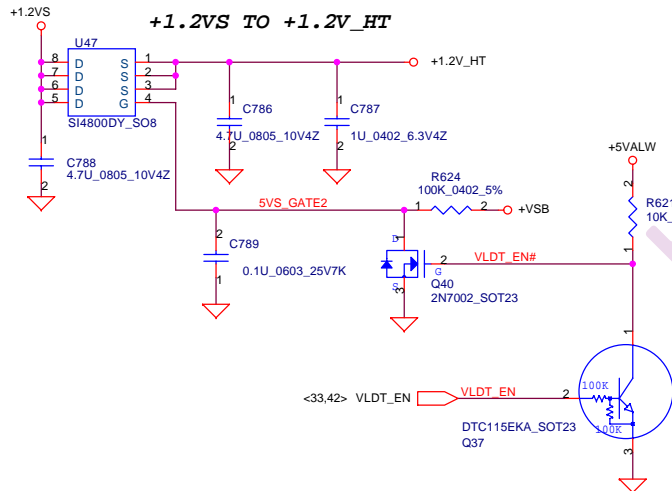
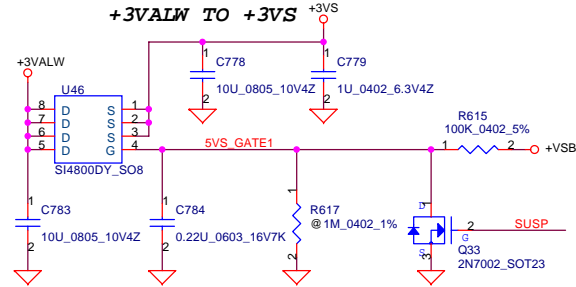
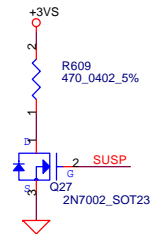
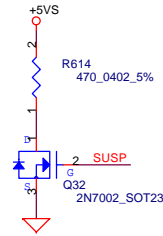
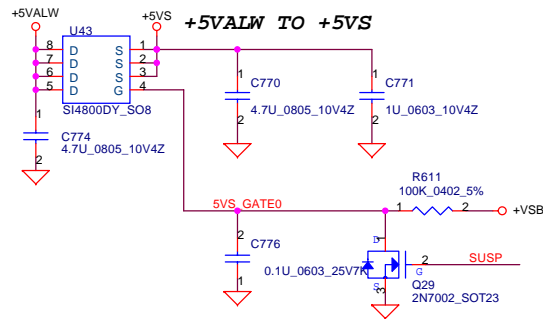
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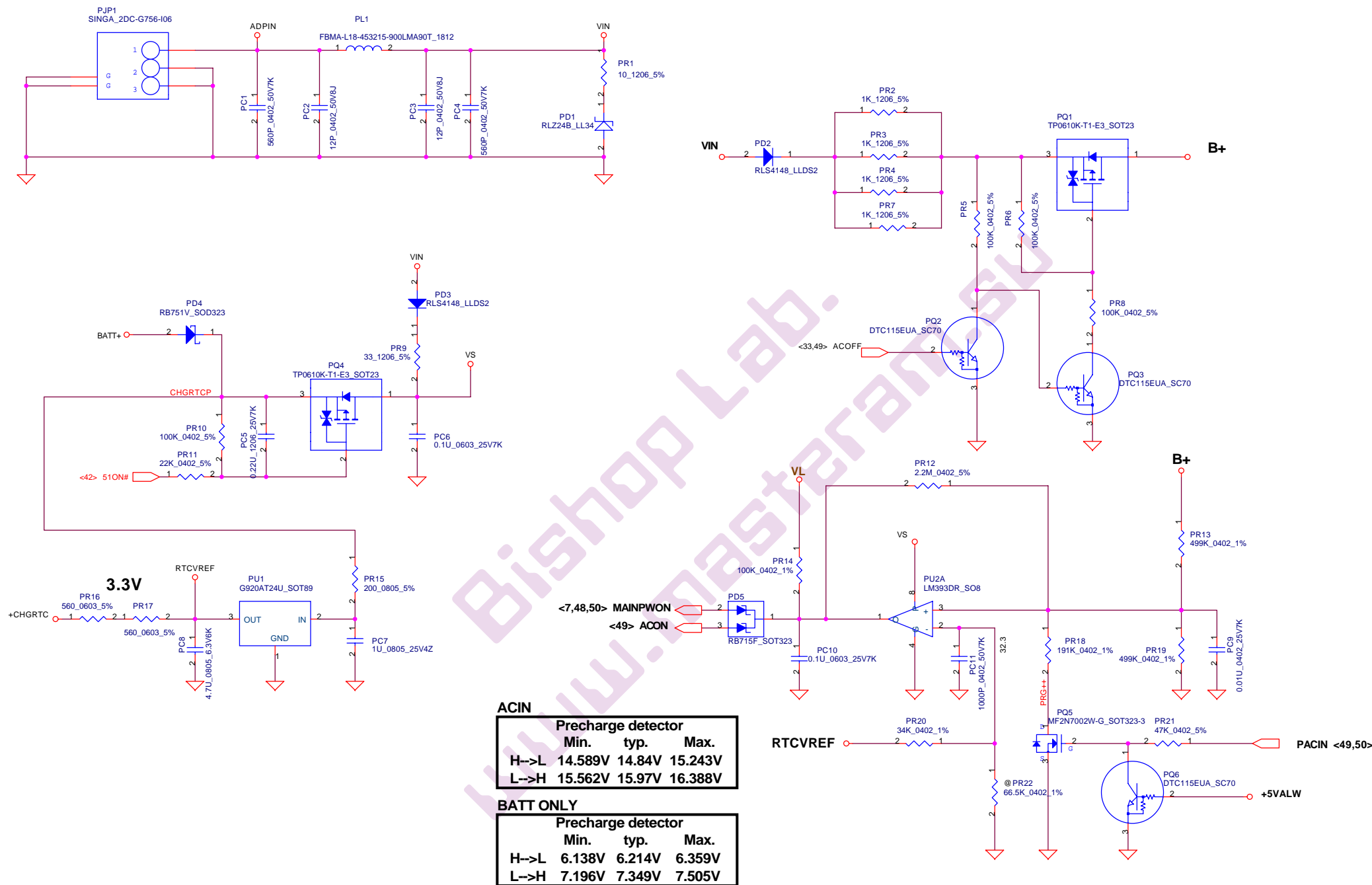
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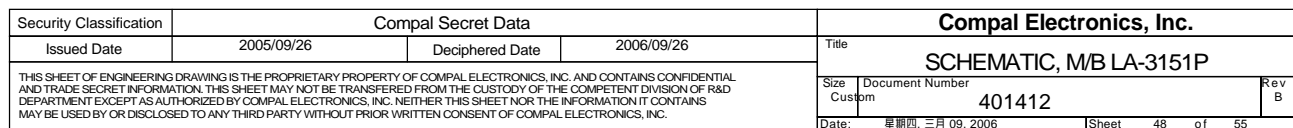


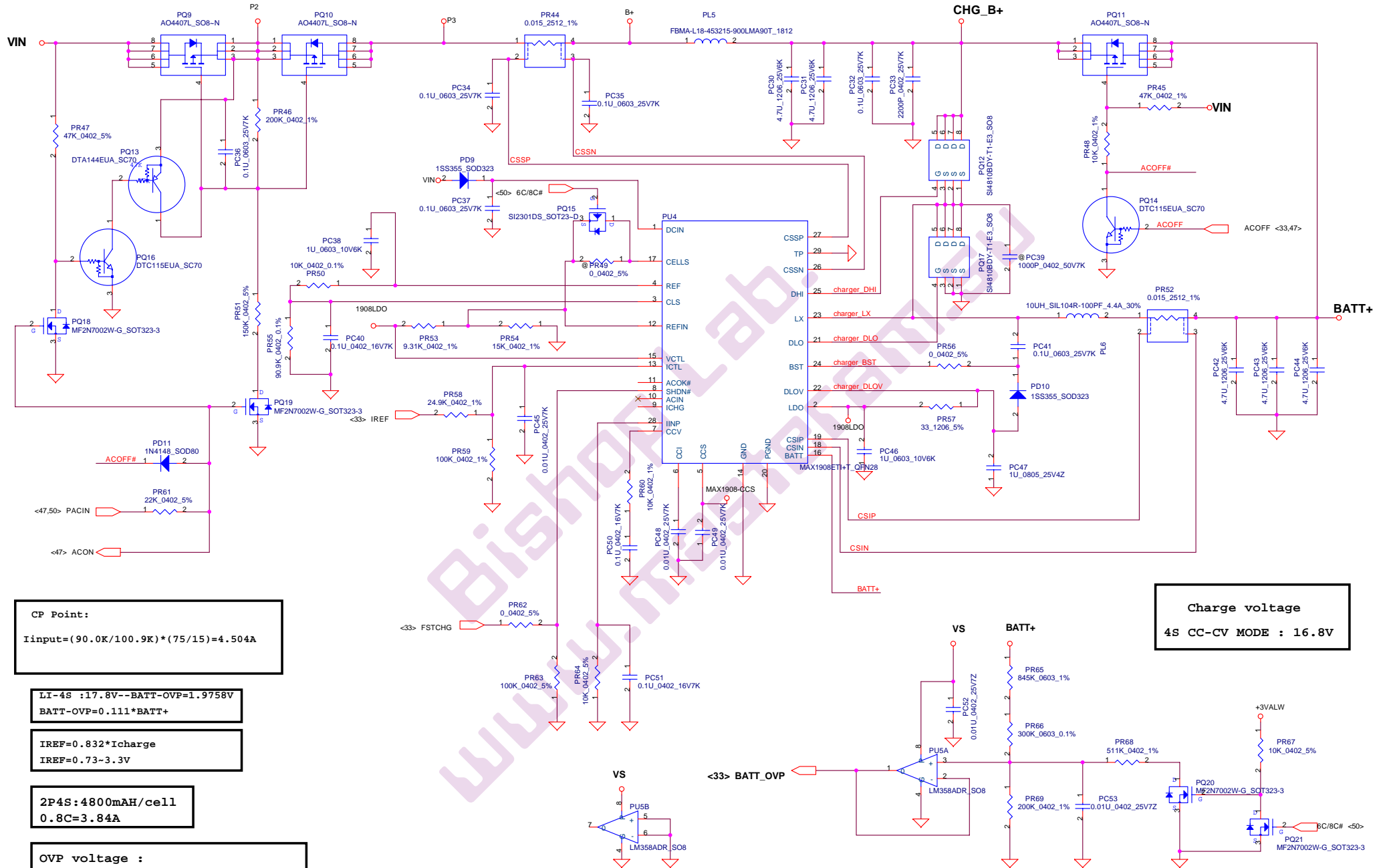
Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER	KSI2	PLAY	
KSI3	STOP		KSI3	STOP	VOL_UP
KSI4	NEXT		KSI4	NEXT	VOL_DOWN
KSI5	REV		KSI5	REV	ARCADE_TV
KSI6		RECORD			



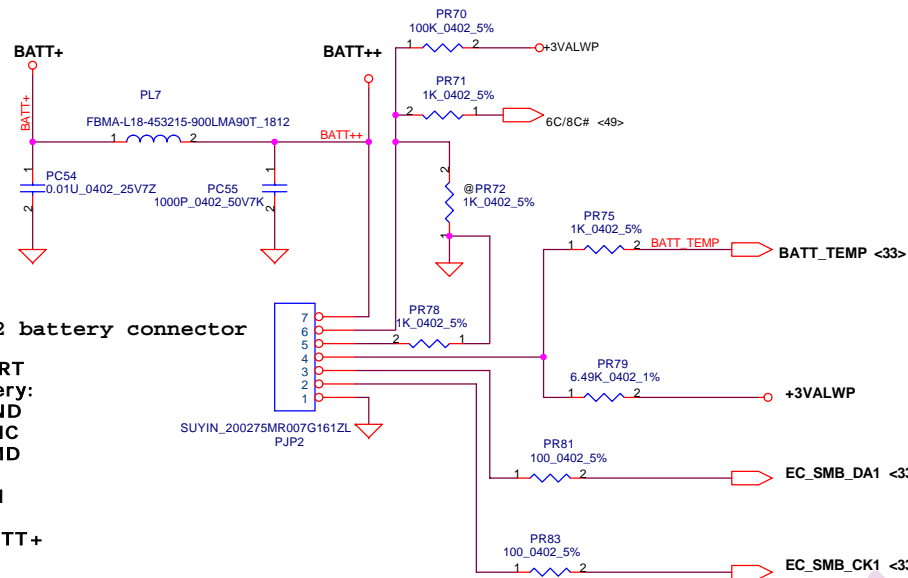
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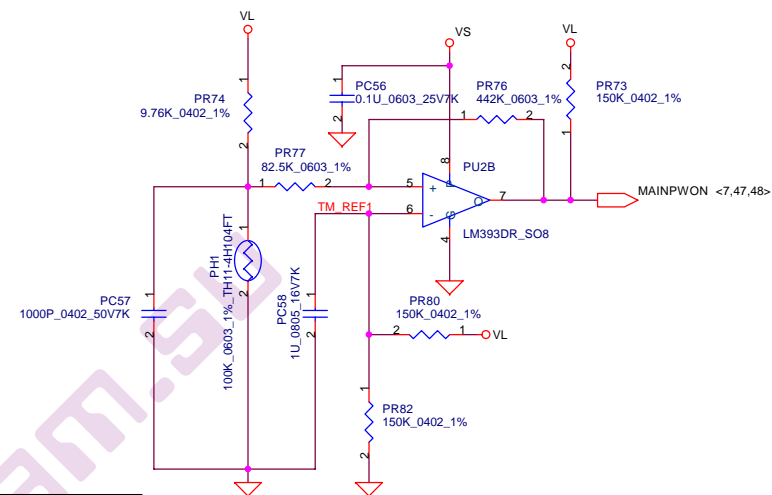


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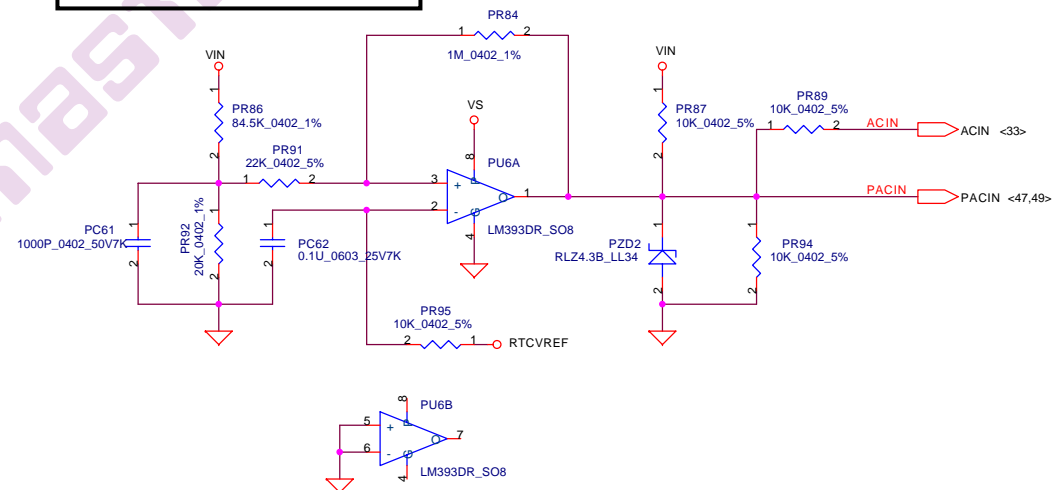
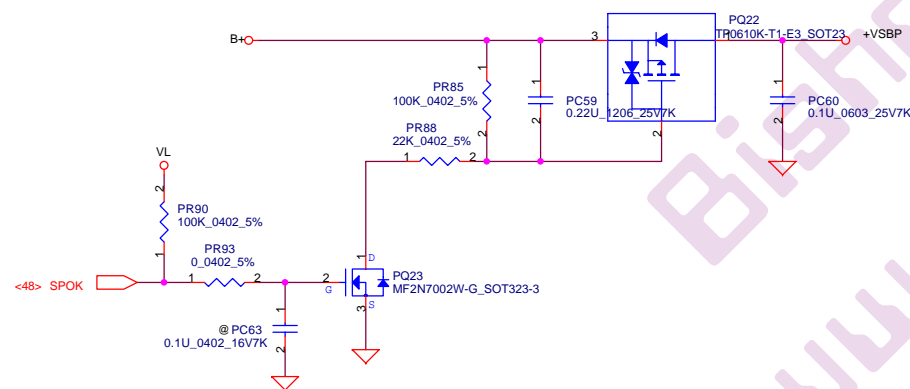
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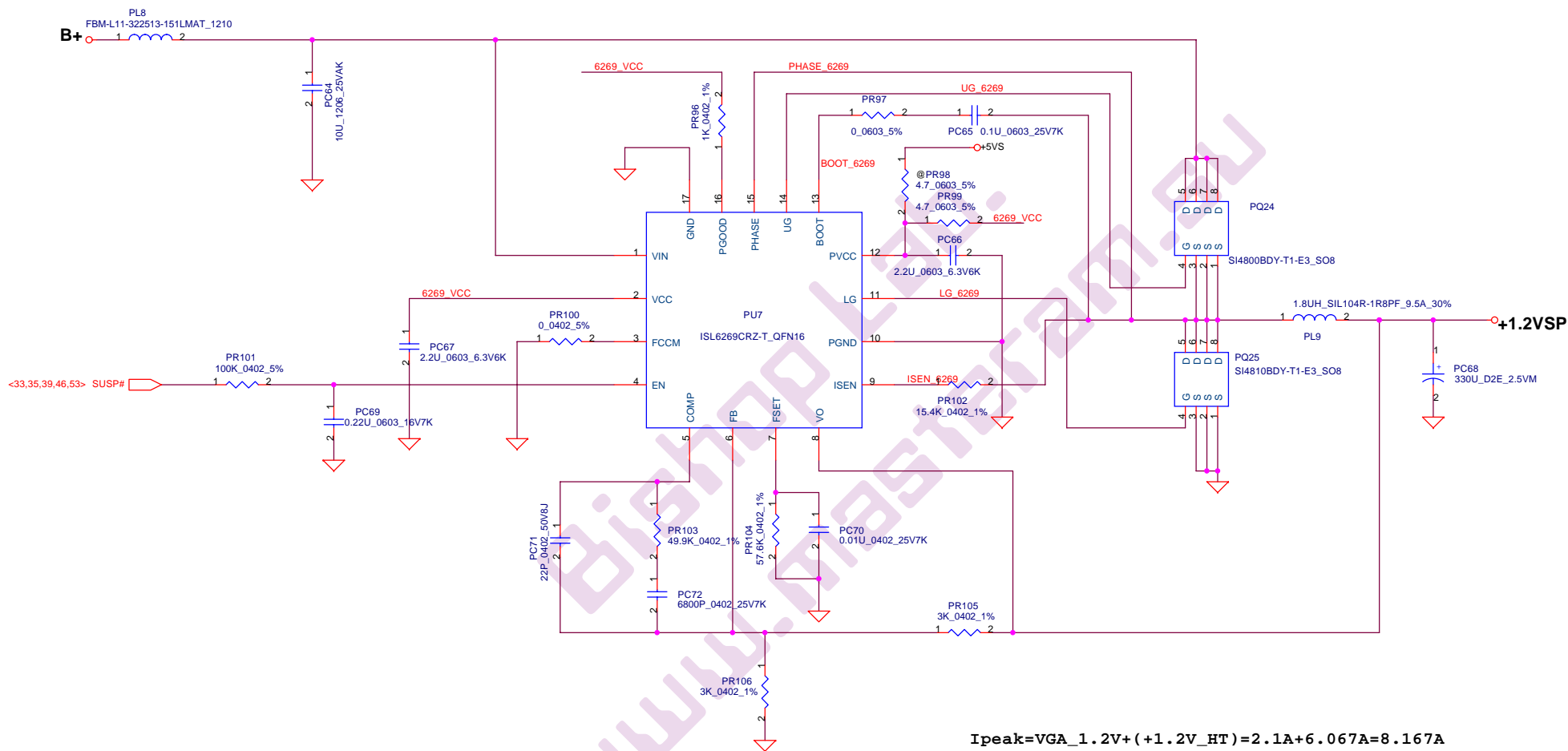
PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C



	Vin Detector		
	Min.	typ.	Max.
H->L	16.976V	17.257V	17.728V
L->H	17.430V	17.901V	18.384V



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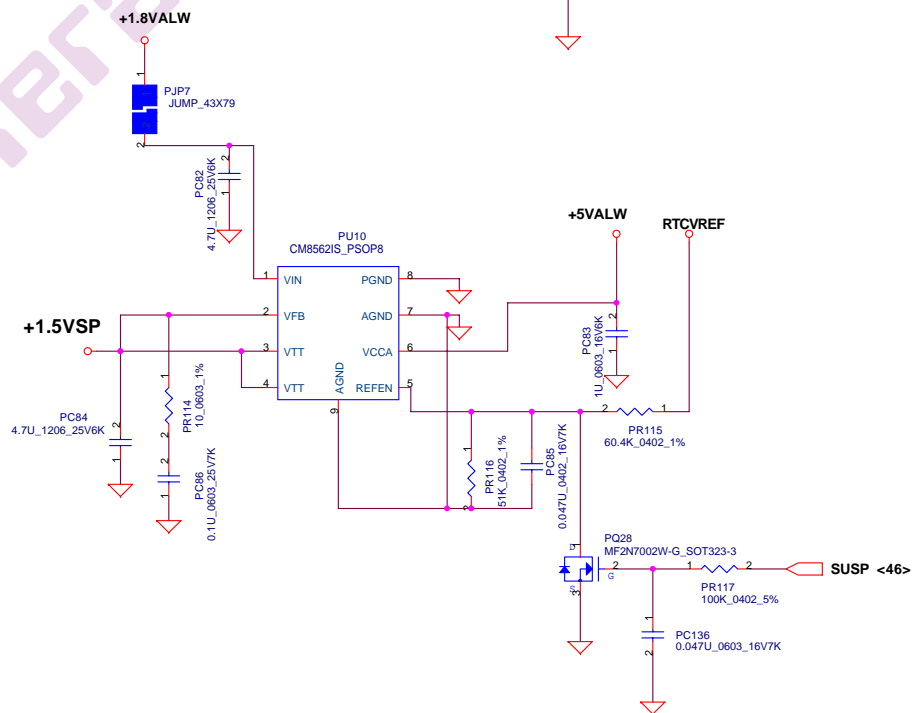
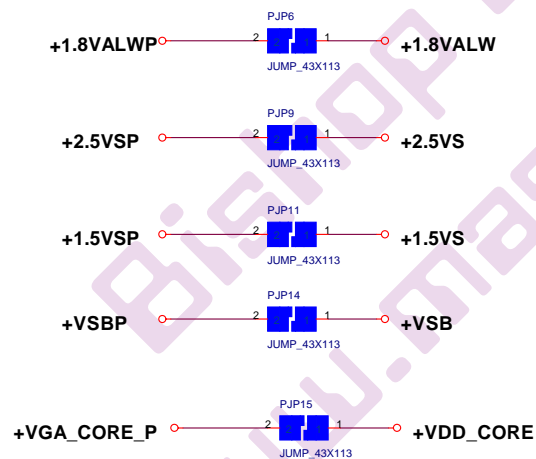
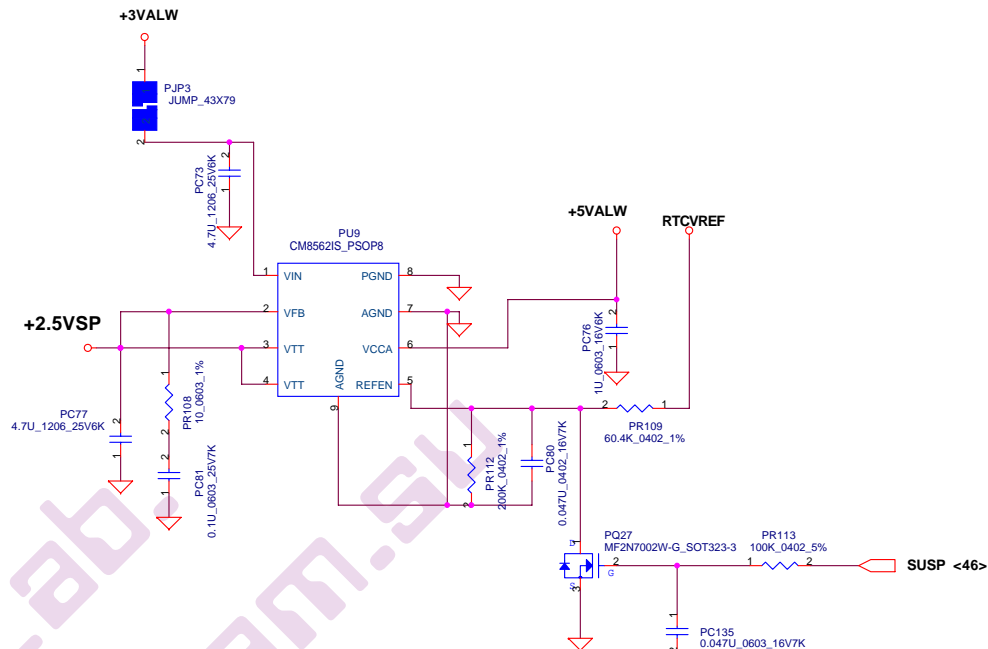
$$I_{peak} = VGA_1.2V + (+1.2V_HT) = 2.1A + 6.067A = 8.167A$$

$$I_{max} = 5.7A$$

$$I_{ocmin} = 9.23A$$

$$I_{ocmax} = 19.23A$$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1							
2							
3							
4							
5							
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