PC POWER-SUPPLY SUPERVISORS

FEATURES

- **Over-Voltage Protection and Lockout: 12V, 5V, and 3.3V Supplies**
- **Over-Current Protection and Lockout: 12V, 5V, and 3.3V Supplies**
- **Under-Voltage Protection and Lockout: 12V Supplies**
- **Under-Voltage Detect: 5V and 3.3V Supplies**
- **Fault-Protection Output with Open-Drain Output Stage**
- **Open-Drain, Power-Good Output Signal: Monitors Power-Good Signal Input 3.3V and 5V Supplies**
- **300ms Power-Good Delay**
- **75ms Delay: 5V, 3.3V Power-Supply Short-Circuit Turn-On Protection**
- **2.3ms $\overline{\text{PSON}}$ Control To $\overline{\text{FPO}}$ Turn-Off Delay**
- **38ms $\overline{\text{PSON}}$ Control Debounce**
- **Wide Supply Voltage Range: 4.5V to 15V**

DESCRIPTION

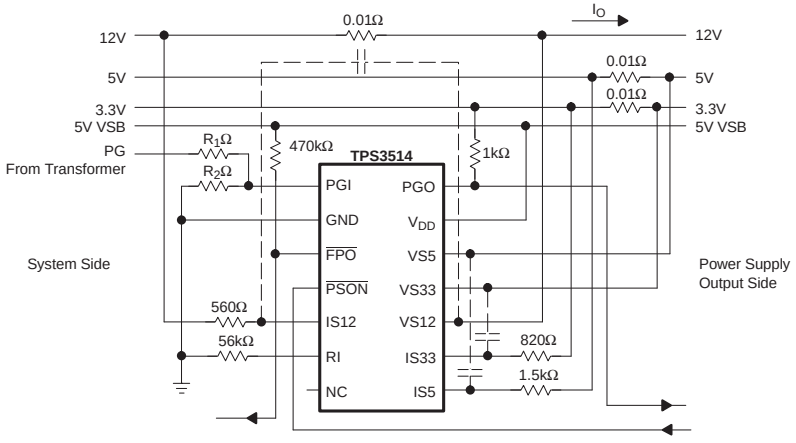
The TPS3514 is a PC switching power-supply system monitor with minimum external components. It provides under-voltage lockout (UVLO), over-voltage (OV), under-voltage (UV), over-current (OC) protection circuits, power-good indicator, and on/off control.

UVLO thresholds are 4.45V (on) and 3.65V (off). Over-current protection (OCP) and over-voltage protection (OVP) monitor 3.3V, 5V, and 12V supplies. When an OC or OV condition is detected, the power-good output (PGO) is asserted low and the fault protection output ($\overline{\text{FPO}}$) is latched high. $\overline{\text{PSON}}$ from low-to-high resets the latch. The OCP function will be enabled 75ms after $\overline{\text{PSON}}$ goes LOW with PGI HIGH and a debounce of typically 38ms. A built-in 2.3ms delay with 38ms debounce from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$ output is enabled at turn-off.

An external resistor is connected between the RI pin and the GND pin. This will program a precise $I_{(REF)}$ for OCP function. The programmable $I_{(REF)}$ range is from 12.5µA to 62.5µA. Three OCP comparators and the $I_{(REF)}$ section are supplied by VS12. The current draw from the VS12 pin is less than 1mA.

The power-good feature monitors PGI, the 3.3V and 5V supplies, and issues a power-good signal when the output is ready.

The TPS3514 is characterized for operation from –40°C to +85°C. The TPS3514 is available in DIP-14 and SO-14 packages.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR (1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS3514	SO-14	D	40°C to +85°C	TPS3514	TPS3514D	Rails, 50
					TPS3514DR	Tape and Reel, 2500
	DIP-14	N			TPS3514N	Rails, 25

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

	UNIT
Supply Voltage, VDD	16V
Voltage on $\overline{\text{PSON}}$, IS5, IS33, PGI	8V
Voltage on VS33, VS5	16V
Voltage on $\overline{\text{FPO}}$	16V
Voltage on PGO	8V
All Other Pins	–0.3V to 16V
Continuous Total Power Dissipation	See Dissipation Ratings Table
Operating Free-Air Temperature Range, T_A	–40°C to +85°C
Storage Temperature Range, T_{stg}	–65°C to +150°C
Soldering Temperature	260°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

At specified temperature range.

PARAMETER		MIN	MAX	UNIT
Supply Voltage	V_{DD}	4.5	15	V
Inputs	V_I			
$\overline{PSON}$, VS5, VS33, IS5, IS33			7	V
VS12, IS12			15	V
PGI			VDD + 0.3V (max = 7V)	V
Outputs	V_O			
$\overline{FPO}$			15	V
PGO			7	V
Sink Current	$I_{O(SINK)}$			
$\overline{FPO}$			20	mA
PGO			10	mA
Supply Voltage Rising Time	t_R (1)	1		ms
OCP Reference Source	$I_{(REF)}$	12.5	62.5	µA
Operating Free-Air Temperature Range	T_A	–40	+85	°C

(1) V_{DD} rising and falling slew rate must be less than 14V/ms.

DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq$ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
D	956mW	7.65mW/°C	612mW	497mW
N	1512mW	12.1mW/°C	968mW	786mW

OVER-CURRENT PROTECTION

	MAX OUTPUT CURRENT	OVER-CURRENT PROTECTION TRIP POINT (1)
12V	6A	9.2A
5V	16A	24.6A
3.3V	9A	13.5A

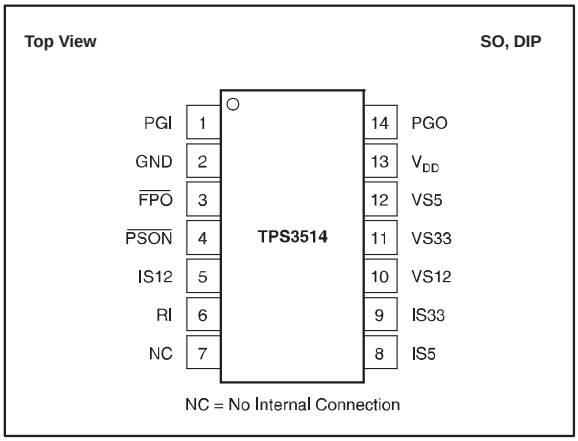
(1) Over-current protection trip point can be programmable.

ELECTRICAL CHARACTERISTICS

Limits apply over operating free-air temperature range, T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	TPS3514 MIN	TPS3514 TYP	TPS3514 MAX	UNIT
OVER-VOLTAGE AND OVER-CURRENT PROTECTION						
Over-Voltage Threshold						
VS33			3.7	3.9	4.1	V
VS5			5.7	6.1	6.5	V
VS12			13.2	13.8	14.4	V
Ratio of Current Sense Sink Current to Current Sense Setting Pin (RI) Source Current, $I_{(REF)}$	C	Resistor at RI = 30kΩ, 0.1% Resistor	7.6	8	8.4	
Leakage Current ($\overline{FPO}$)	I_{lkg}	$V_{(\overline{FPO})}$ = 5V			5	µA
Low-Level Output Voltage ($\overline{FPO}$)	V_{OL}	$I_{(SINK)}$ = 20mA, V_{DD} = 5V			0.7	V
Noise Deglitch Time (OVP)		V_{DD} = 5V	35	73	110	µs
Current Source Reference Voltage	$V_{(RI)}$	V_{DD} = 5V	1.1	1.15	1.2	V
UNDER-VOLTAGE LOCKOUT						
Start Threshold Voltage					4.45	V
Minimum Operating Voltage After Start-Up			3.65			V
PGI AND PGO						
Input Threshold	$V_{IT(PGI)}$		0.9 x typ	1.15	1.01 x typ	V
Under-Voltage Threshold						
VS33			2	2.2	2.4	V
VS5			3.3	3.5	3.7	V
VS12			8.5	9	9.5	V
Input Offset Voltage for OCP Comparators					5	mV
Leakage Current (PGO)	I_{lkg}	PGO = 5V			5	µA
Low-Level Output Voltage (PGO)	V_{OL}	$I_{(SINK)}$ = 10mA, V_{DD} = 4.5V			0.4	V
Short-Circuit Protection Delay	3.3V, 5V		49	75	114	ms
Delay Time	$t_{(d)(1)}$					
PGI to PGO		V_{DD} = 5V	200	300	450	ms
PGI to $\overline{FPO}$		V_{DD} = 5V	3.2	4.8	7.2	ms
Noise Deglitch Time						
PGI to PGO		V_{DD} = 5V	88	150	225	µs
12V UVP to $\overline{FPO}$		V_{DD} = 5V	88	150	225	µs
$\overline{PSON}$ CONTROL						
Input Pull-Up Current	I_I	$\overline{PSON}$ = 0V		–120		µA
High-Level Input Voltage	V_{IH}		2.4			V
Low-Level Input Voltage	V_{IL}				1.2	V
Debounce Time ($\overline{PSON}$)	$t_{(b)}$	V_{DD} = 5V	24	38	50	ms
Delay Time ($\overline{PSON}$ to $\overline{FPO}$)	$t_{(d)(2)}$	V_{DD} = 5V	t_b + 1.1	t_b + 2.3	t_b + 4	ms
TOTAL DEVICE						
Supply Current	I_{DD}	$\overline{PSON}$ = 5V			1	mA

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
3	$\overline{\text{FPO}}$	Inverted Fault Ptotection output. Open-drain output stage.
2	GND	Ground
5	IS12	12V Over-Current Protection Input
8	IS5	5V Over-Current Protection Input
9	IS33	3.3V Over-Current Protection Input
7	NC	No Internal Connection
1	PGI	Power-Good Input
14	PGO	Power-Good Output. Open-drain output stage.
4	$\overline{\text{PSON}}$	On/Off Control Input
6	RI	OCP Reference Source
13	V_{DD}	Supply Voltage
10	VS12	12V Over-Voltage/Under-Voltage Protection Input
11	VS33	3.3V Over-Voltage/Under-Voltage Protection Input
12	VS5	5V Over-Voltage/Under-Voltage Protection Input

FUNCTION TABLE(1)

PGI	$\overline{\text{PSON}}$	UV CONDITION 3.3V/5V	OV CONDITIONS	UV CONDITION 12V OC CONDITIONS	$\overline{\text{FPO}}$ (2)	PGO(3)
< 0.9V	L	No	No	No	L	L
< 0.9V	L	No	No	Yes	L	L
< 0.9V	L	No	Yes	No	H	L
< 0.9V	L	No	Yes	Yes	H	L
< 0.9V	L	Yes	No	No	L	L
< 0.9V	L	Yes	No	Yes	L	L
< 0.9V	L	Yes	Yes	No	H	L
< 0.9V	L	Yes	Yes	Yes	H	L
> 1.2V	L	No	No	No	L	H
> 1.2V	L	No	No	Yes	H	L
> 1.2V	L	No	Yes	No	H	L
> 1.2V	L	No	Yes	Yes	H	L
> 1.2V	L	Yes	No	No	H	L
> 1.2V	L	Yes	No	Yes	H	L
> 1.2V	L	Yes	Yes	No	H	L
> 1.2V	L	Yes	Yes	Yes	H	L
x	H	x	x	x	H	L

(1) x = Don't Care.
(2) For FPO, L = Fault is not latched. H = Fault is latched.
(3) For PGO, L = Fault. H = No Fault.

TIMING DIAGRAMS

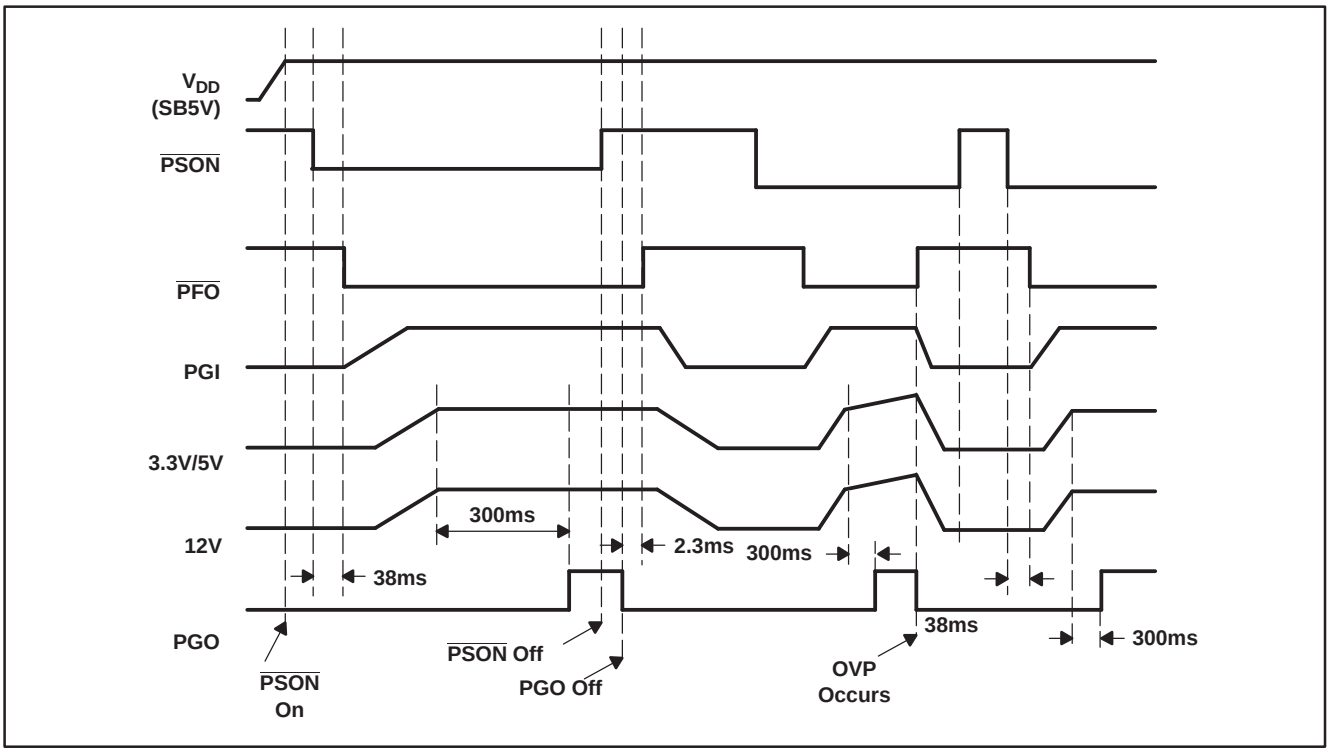


Figure 1. AC Turn-On and Over-Voltage Protect

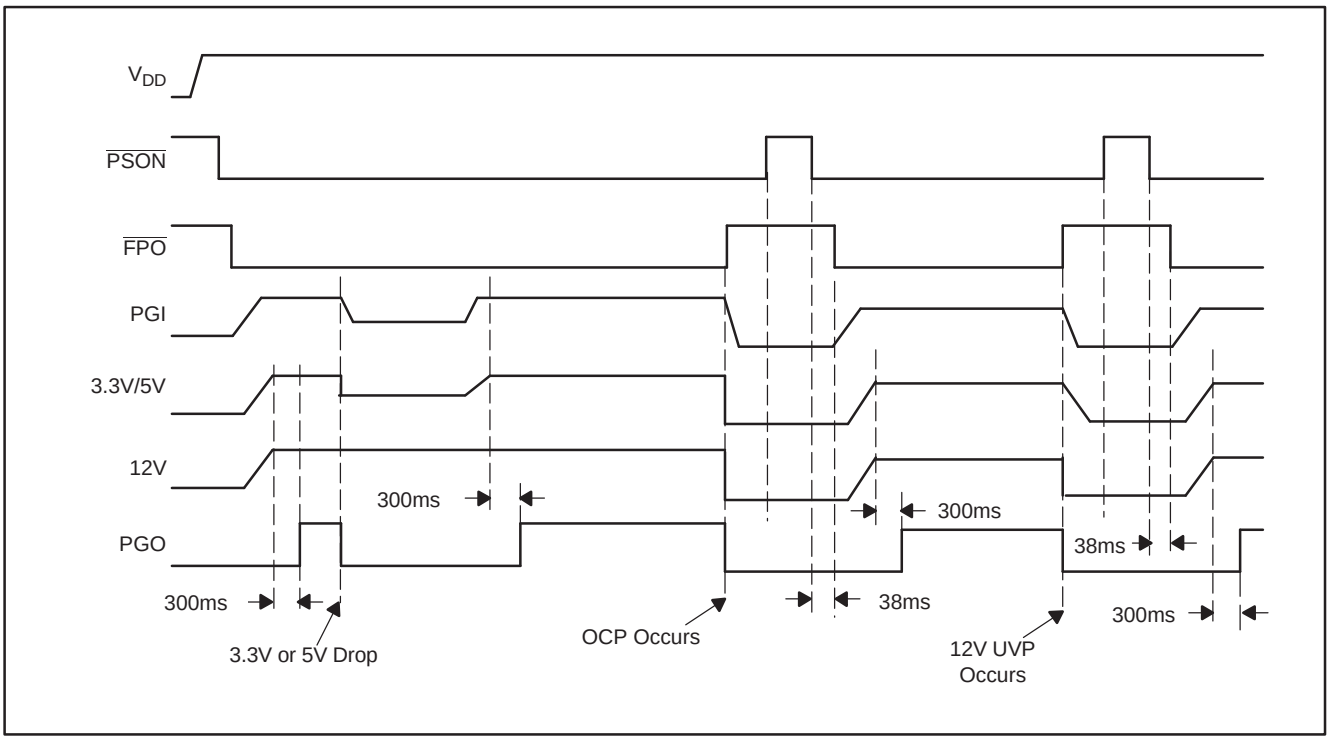
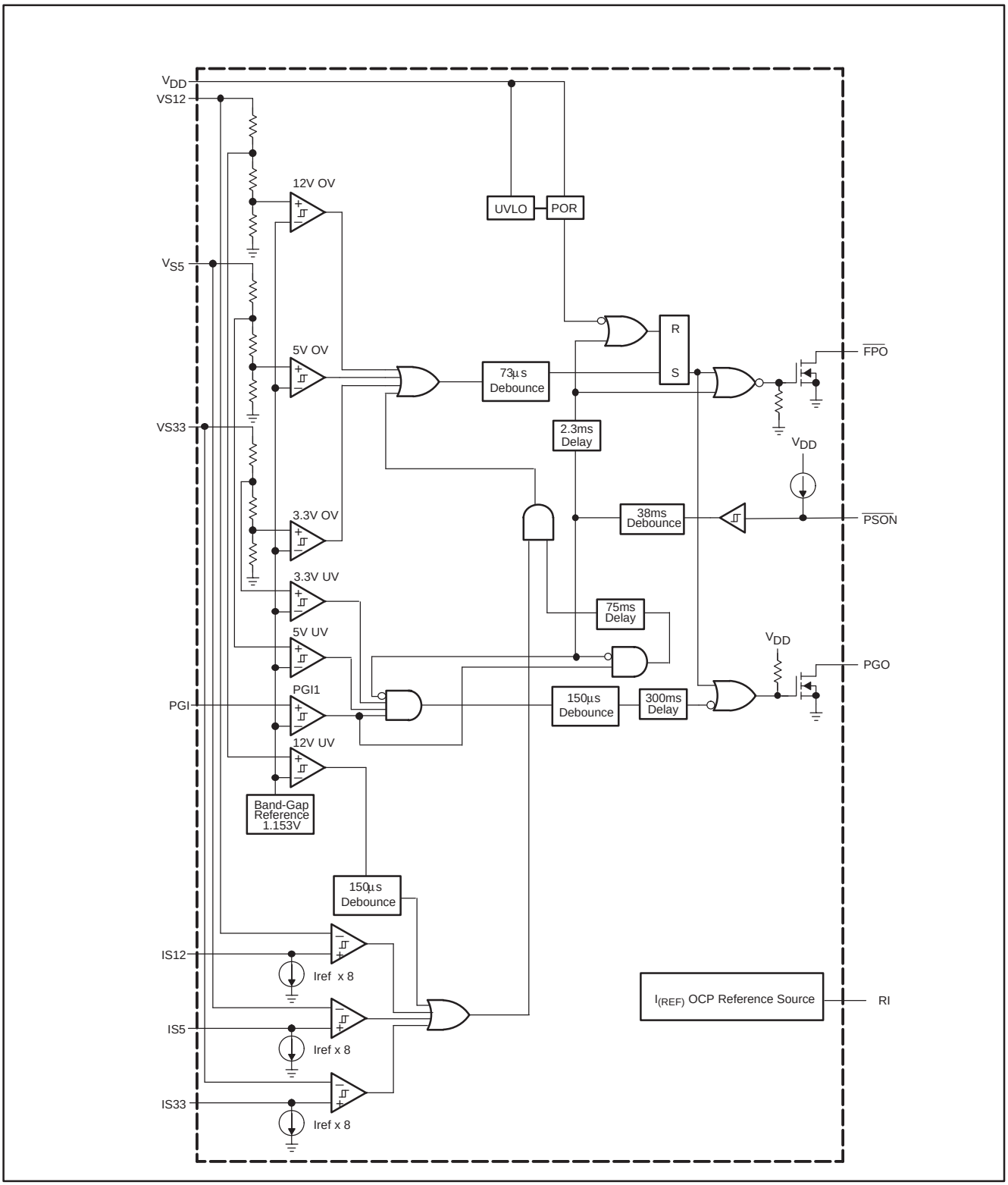


Figure 2. Over-Current and Under-Voltage Detect/Protect

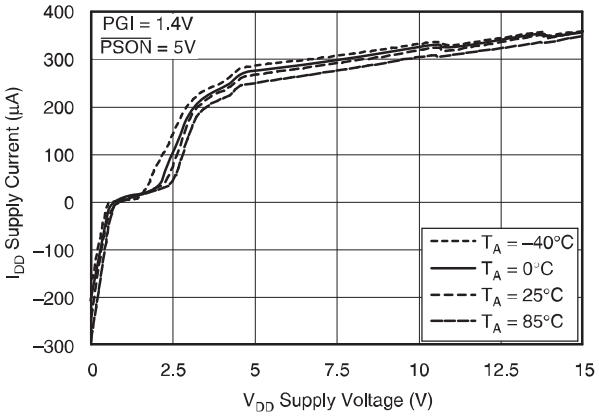
SCHEMATIC


VDD
VS12
VSS5
VS33
IS12
IS5
IS33
PGI
12V OV
5V OV
3.3V OV
3.3V UV
5V UV
PGI1
12V UV
Band-Gap Reference 1.153V
UVLO
POR
73µs Debounce
2.3ms Delay
38ms Debounce
75ms Delay
150µs Debounce
300ms Delay
150µs Debounce
R
S
FPO
PSON
PGO
Iref x 8
Iref x 8
Iref x 8
I(REF) OCP Reference Source
RI

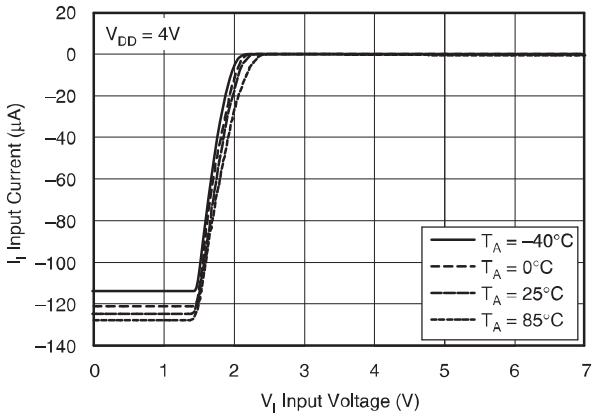
TYPICAL CHARACTERISTICS

T_A = +25°C, unless otherwise noted.

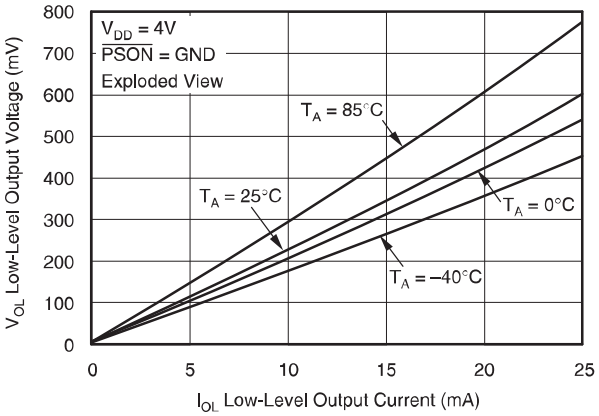
SUPPLY CURRENT vs SUPPLY VOLTAGE



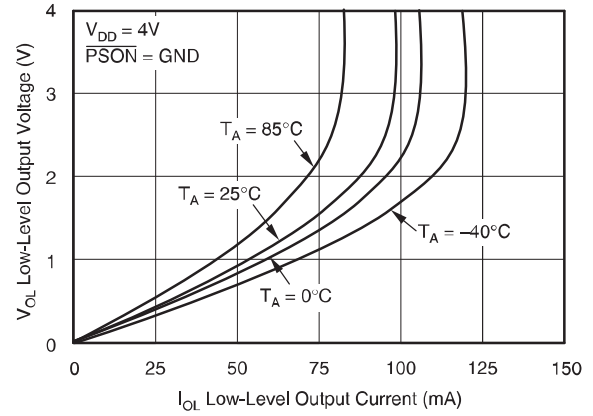
INPUT CURRENT (PSON) vs INPUT VOLTAGE (PSON)



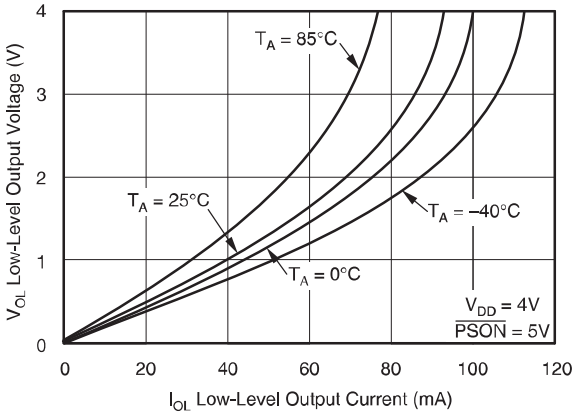
LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)



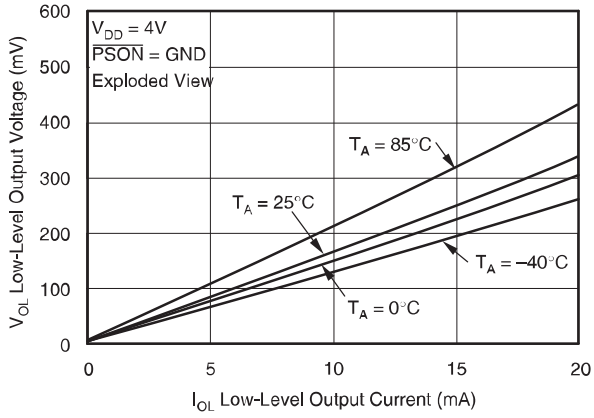
LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)



LOW-LEVEL OUTPUT VOLTAGE (PGO) vs LOW-LEVEL OUTPUT CURRENT (PGO)



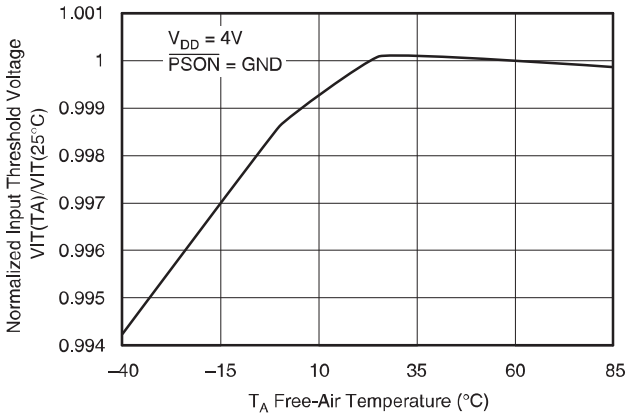
LOW-LEVEL OUTPUT VOLTAGE (PGO) vs LOW-LEVEL OUTPUT CURRENT (PGO)



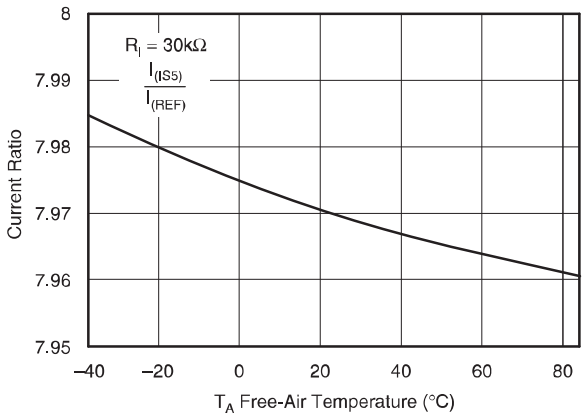
TYPICAL CHARACTERISTICS (continued)

T_A = +25°C, unless otherwise noted.

NORMALIZED SENSE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}



CURRENT RATIO vs FREE-AIR TEMPERATURE



DETAILED DESCRIPTION

Power-Good and Power-Good Delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. Power-Good Output (PGO) is a power-good indicator and should be asserted high by the PC power supply to indicate that the 5VDC and 3.3VDC outputs are above the under-voltage threshold limit. At this time, the supply should be able to provide enough power to assure continuous operation within the specification.

Conversely, when either the 5VDC or the 3.3VDC output voltages fall below the under-voltage threshold, or when main power has been removed for a sufficiently long time so that power-supply operation is no longer assured, PGO should be deasserted to a low state. The power-good, DC enable ($\overline{PSON}$), and the 5V/3.3V supply rails are shown in Figure 3.

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

$2ms \le t_2 \le 20ms$, $100ms < t_3 < 2000ms$, $t_4 > 1ms$, $t_5 \le 10ms$

Furthermore, motherboards should be designed to comply with the above recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3514 family of power-supply supervisors provides a PGO for the 3.3V and 5V supply voltage rails and a separate Power-Good Input (PGI). An internal timer is used to generate a 300ms power-good delay.

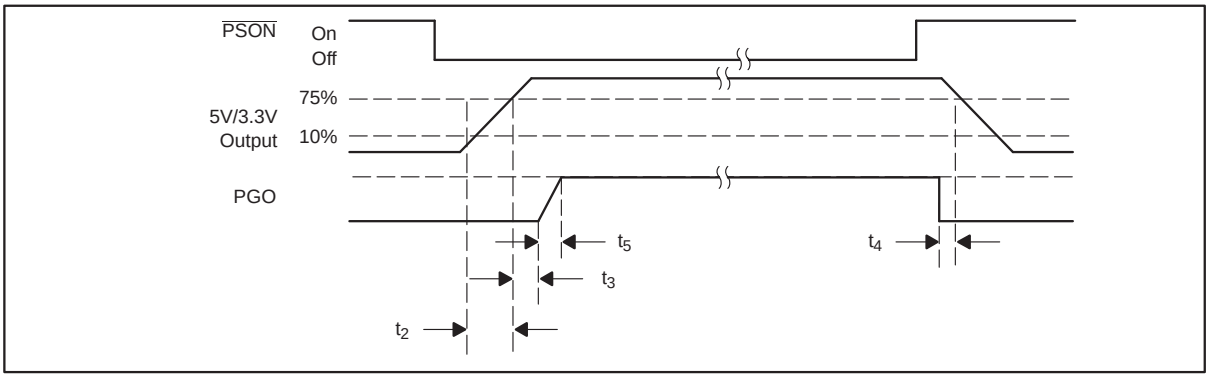


Figure 3. Timing of $\overline{PSON}$ and PGO

If the voltage signals at PGI, VS33, and VS5 rise above the under-voltage threshold, the open-drain PGO will go high after a delay of 300ms. When the PGI voltage or any of the 3.3V/5V rail drops below the under-voltage threshold, PGO will be disabled immediately.

Power-Supply Remote On/Off ($\overline{\text{PSON}}$) And Fault Protect Output ($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turn-on and power-saving functions, the PC power supply will require two characteristics. One is a DC power-supply remote on/off function; the other is standby voltage to achieve very low power consumption of the PC system. Thus, requiring the main power supply to be shut down.

The power-supply remote on/off ($\overline{\text{PSON}}$) is an active-low signal that turns on all of the main power rails including the 3.3V, 5V, –5V, and –12V power rails. When this signal is held high by the PC motherboard or left open-circuited, the signal of the Fault Protect Output ($\overline{\text{FPO}}$) also goes high. In this condition, the main power rails should not deliver current and should be held at 0V.

When the $\overline{\text{FPO}}$ signal is held high due to an occurring fault condition, the fault status will be latched and the outputs of the main power rails should not deliver current and should be held at 0V. Toggling $\overline{\text{PSON}}$ from low to high will reset the fault protection latch. During this fault condition, only the standby power is not affected.

When $\overline{\text{PSON}}$ goes from high to low or low to high, the 38ms debounce block will prevent a glitch on the input from disabling/enabling the $\overline{\text{FPO}}$ output. During the HIGH to LOW transition, the under-voltage function is disabled to prevent turn-on failure.

Power should be delivered to the rails only if the $\overline{\text{PSON}}$ signal is held at ground potential, thus, $\overline{\text{FPO}}$ is active low. The $\overline{\text{FPO}}$ pin can be connected to 5VDC (or up to 15VDC) through a pull-up resistor.

Under-Voltage Protection (UVP)

The TPS3514 provides Under-Voltage Protection (UVP) for the 12V rail and Under-Voltage Detect (UVD) for the 3.3V and 5V rails. When an under-voltage condition appears at the VS12 input pin for more than 150µs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from low to high or V_{DD} is removed.

Over-Current Protection (OCP)

In bridge, or forward type, off-line switching power supplies, usually designed for medium to large power, the overload protection design needs to be very precise. Most of these types of power supplies sense the output current for an overload condition. The trigger-point needs to be set higher than the maximum load in order to prevent false turn-on.

The TPS3514 provides Over-Current Protection (OCP) for the 3.3V, 5V, and 12V rails. When an over-current condition appears at the OCP comparator input pins for more than 73µs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from low to high or V_{DD} is removed.

The resistor connected between the RI pin and the GND pin will create a precise $I_{(REF)}$ for the OCP function. The formula for choosing the RI resistor is $V_{(RI)}/I_{(REF)}$. The $I_{(REF)}$ range is from 12.5µA to 62.5µA. Three OCP comparators and the $I_{(REF)}$ section are supplied through the V12 pin. Current drawn from the VS12 pin is less than 1mA.

Following is an example on calculating OCP for the 12V rail:

$RI = V_{(RI)}/I_{(REF)} = 1.15V/20\mu A = 56k\Omega$

$I_{(REF)} \bullet C \bullet R_{(IS12)} = R_{(SENSE)} \cdot I_{(OCP\_TRIP)}$

$I_{(OCP\_TRIP)} = 20\mu A \bullet 8 \bullet 560\Omega/0.01\Omega = 9.2A$

C = Current Ratio (typically = 8)

Over-Voltage Protection (OVP)

The Over-Voltage Protection (OVP) of the TPS3514 monitors 3.3V, 5V, and 12V. When an over-voltage condition appears at one of the 3.3V, 5V, or 12V input pins for more than 73µs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from low-to-high or V_{DD} is removed.

During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide over-voltage protection within the power supply.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3514D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS3514D	Samples
TPS3514DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS3514D	Samples
TPS3514N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TPS3514N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

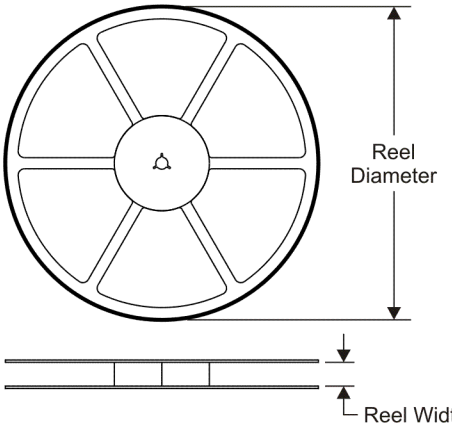
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

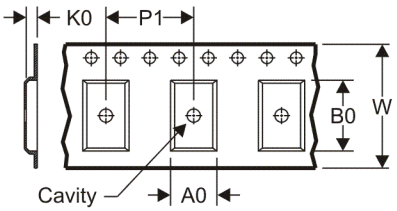
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

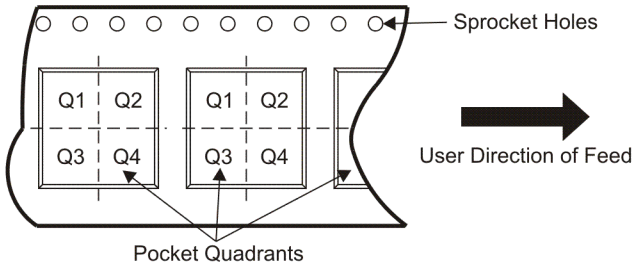


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

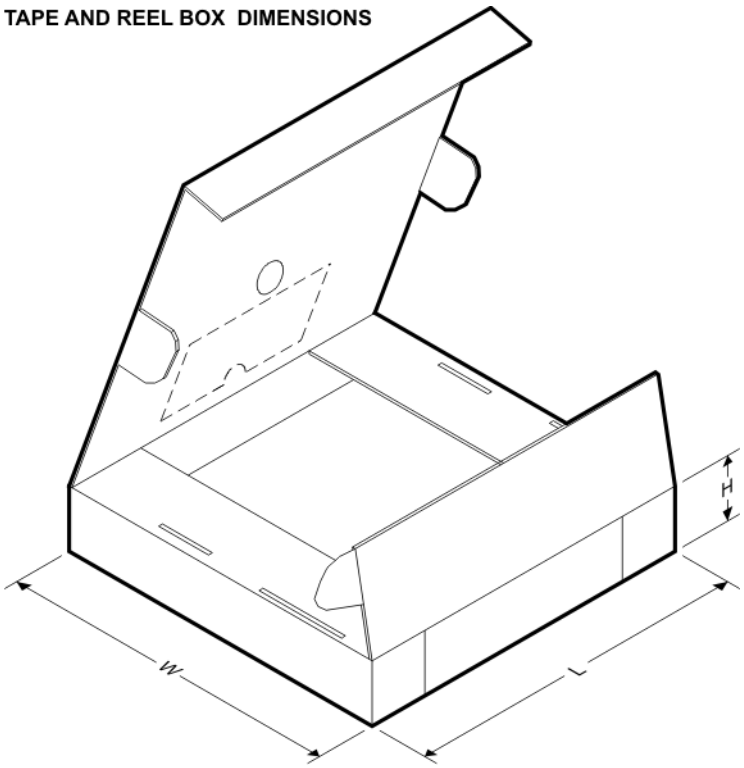
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3514DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



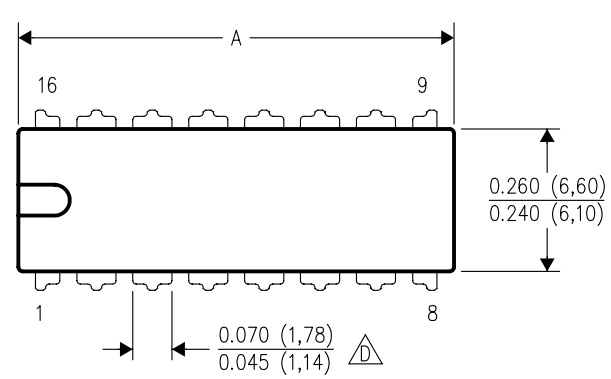
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3514DR	SOIC	D	14	2500	333.2	345.9	28.6

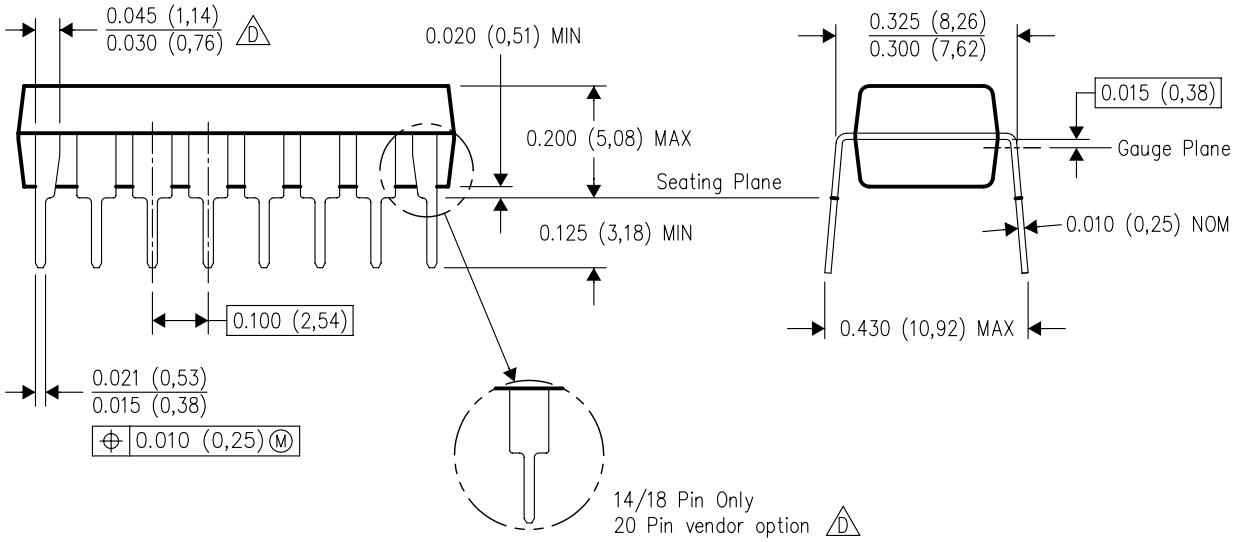
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



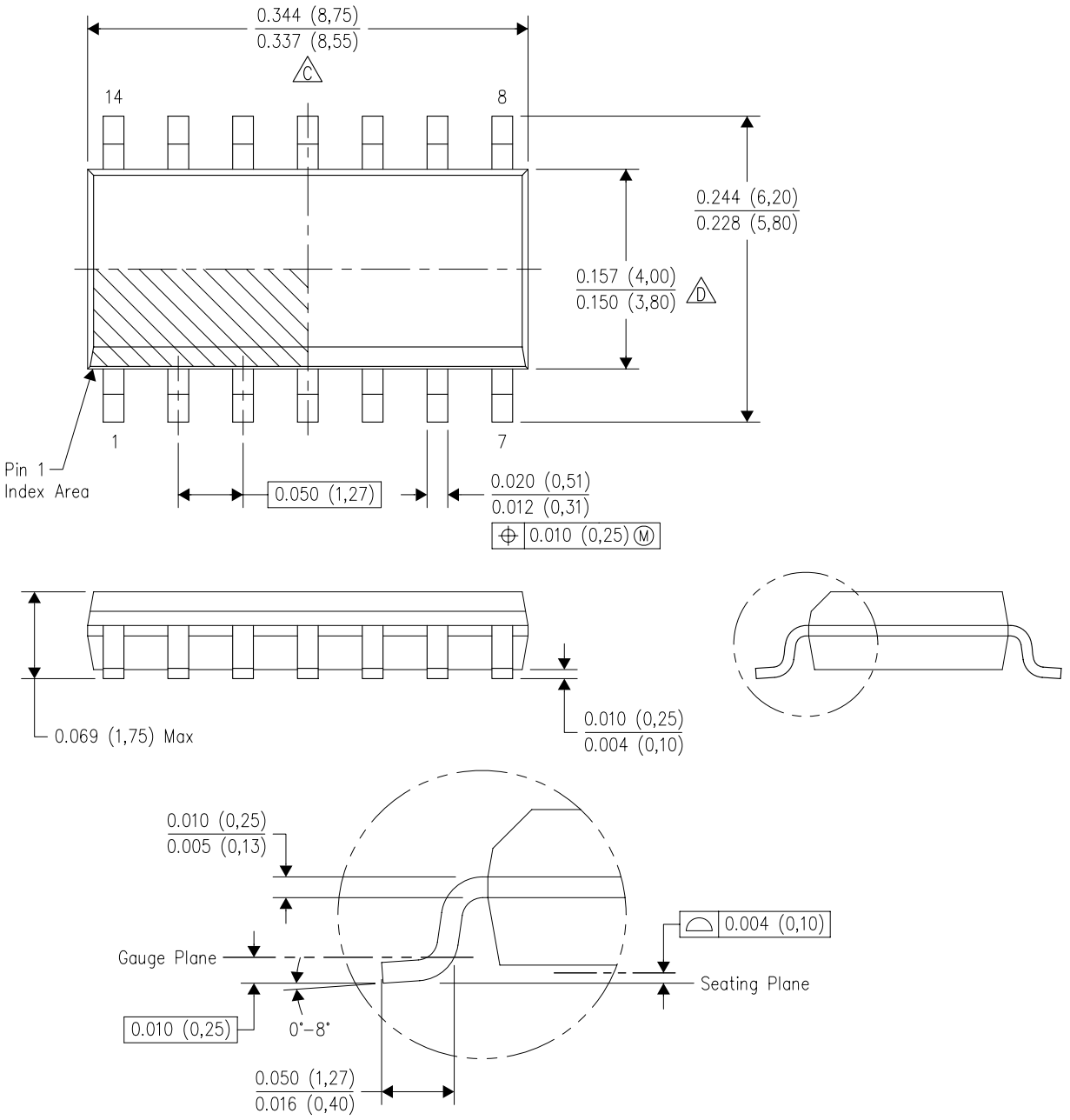
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

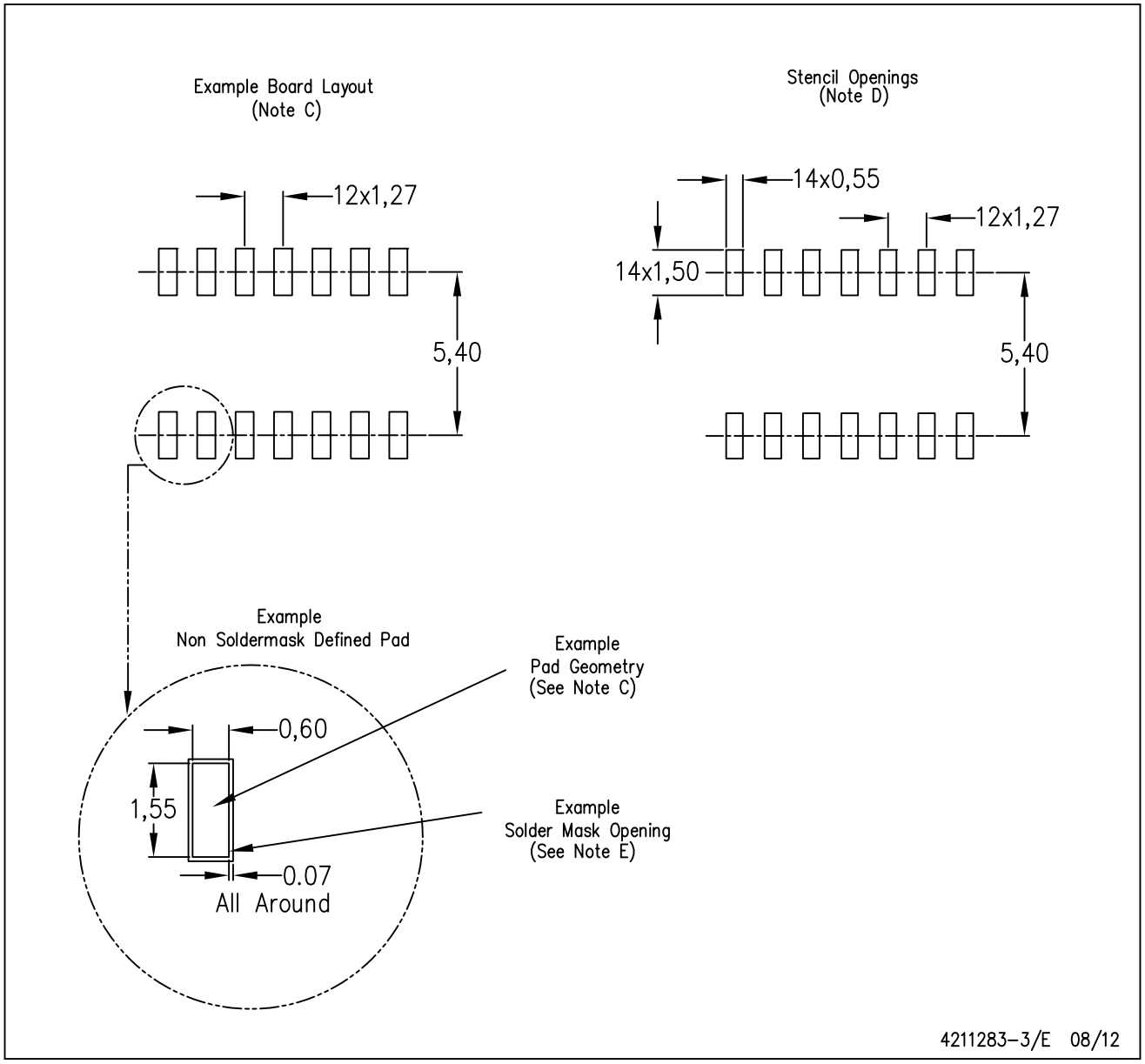
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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