

MS-7383 uATX Version :2.0

PCB Size: 244*230mm(OSP)

CPU:

Intel Pentium 4, Pentium D, Core2 Duo,
Wolfdale, Kentsfield processors in
LGA775 Package.

System Chipset:

Intel Bearlake G31 - MCH (North Bridge)
Intel ICH7/ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI 4M EEPROM
Aliza Codec -- ALC883/888/861D/660
LPC Super I/O -- W83627DHG
LAN-- REALTEK RTL8101E/8111B
Clock Gen- RTM876-660

Main Memory:

Dual Channel DDR II * 4 (Max 2GB)

Expansion Slots:

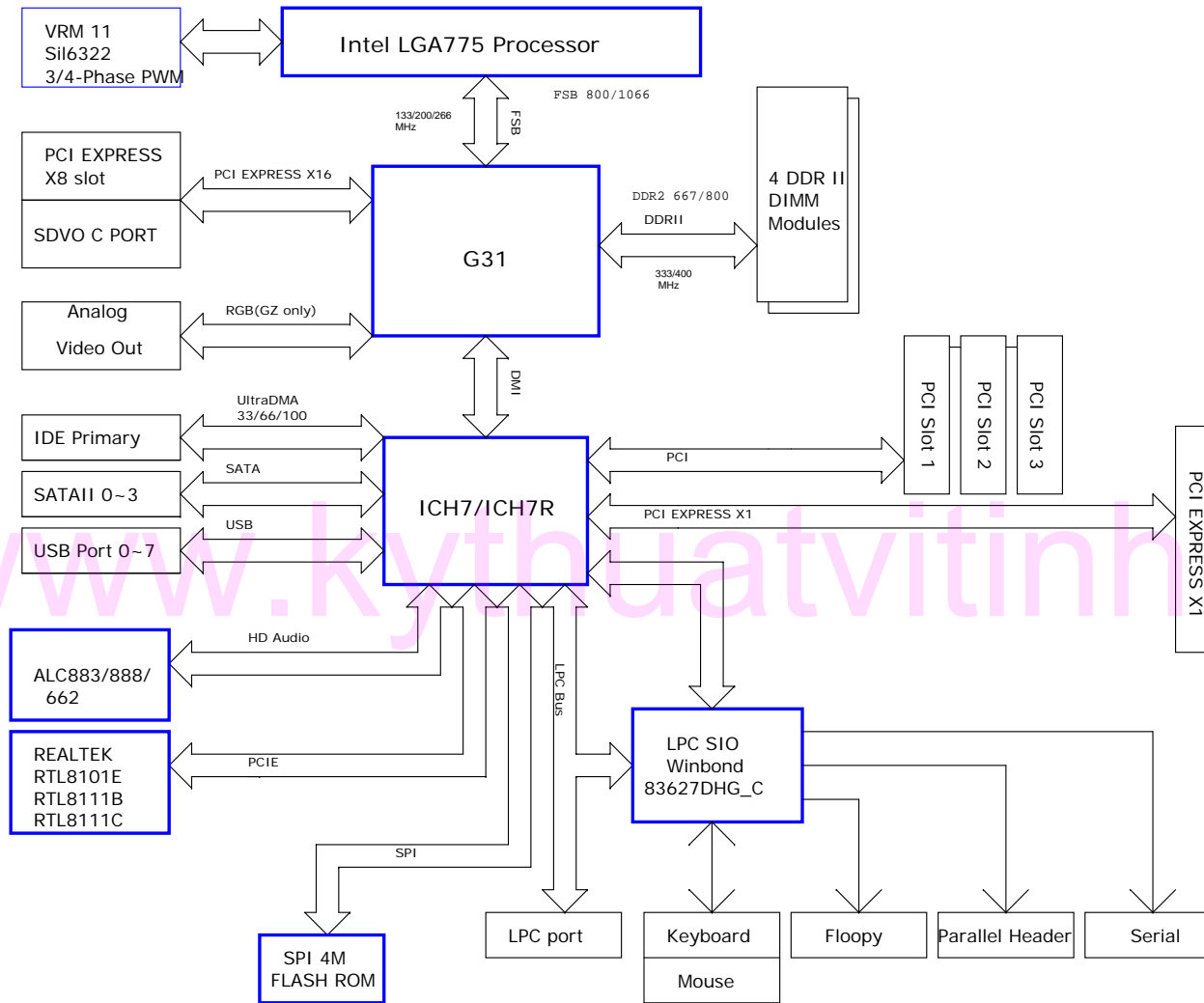
PCI2.2 SLOT * 3
PCI EXPRESS X16 SLOT

RICH PWM:

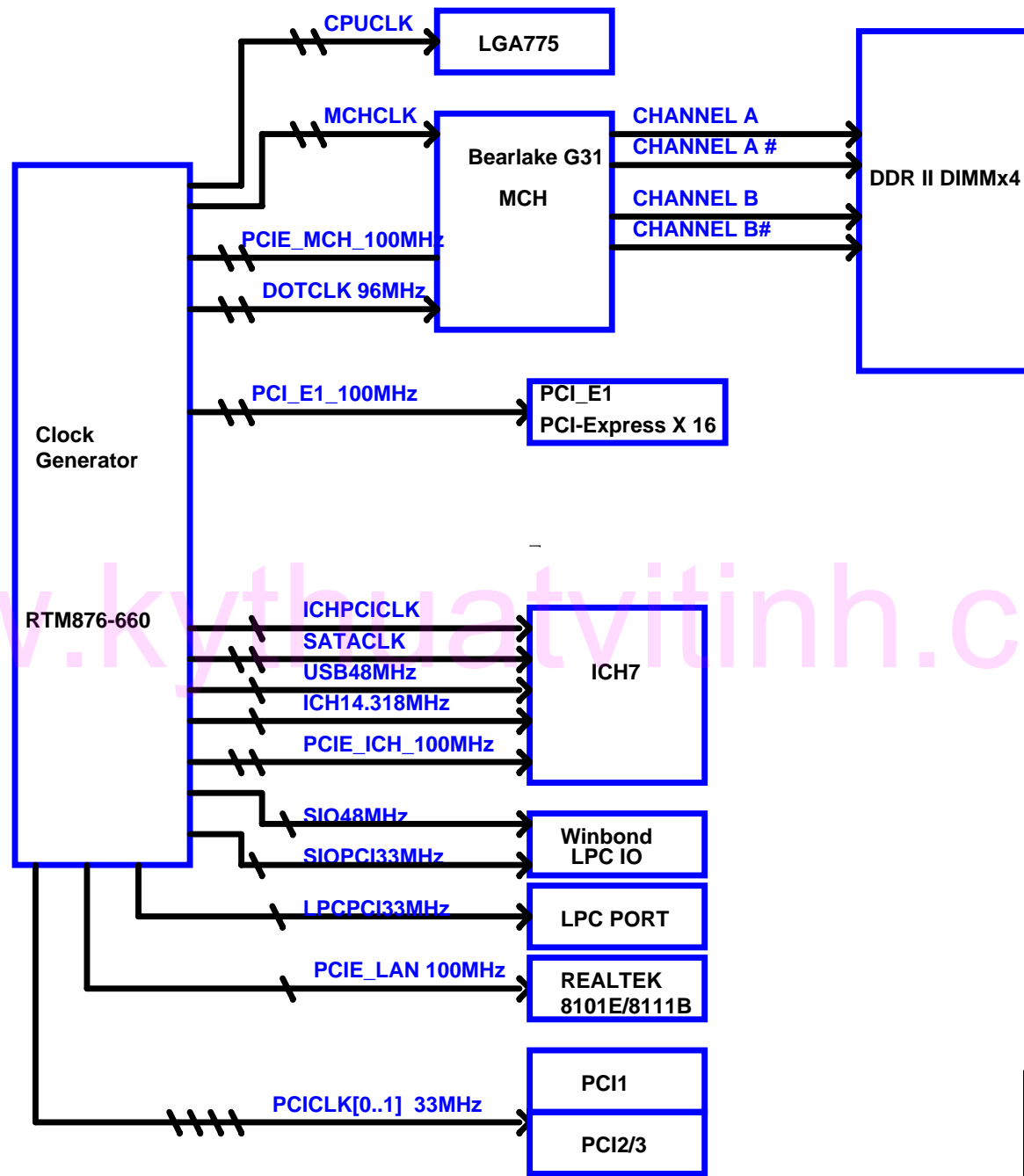
Controller: Sil6322

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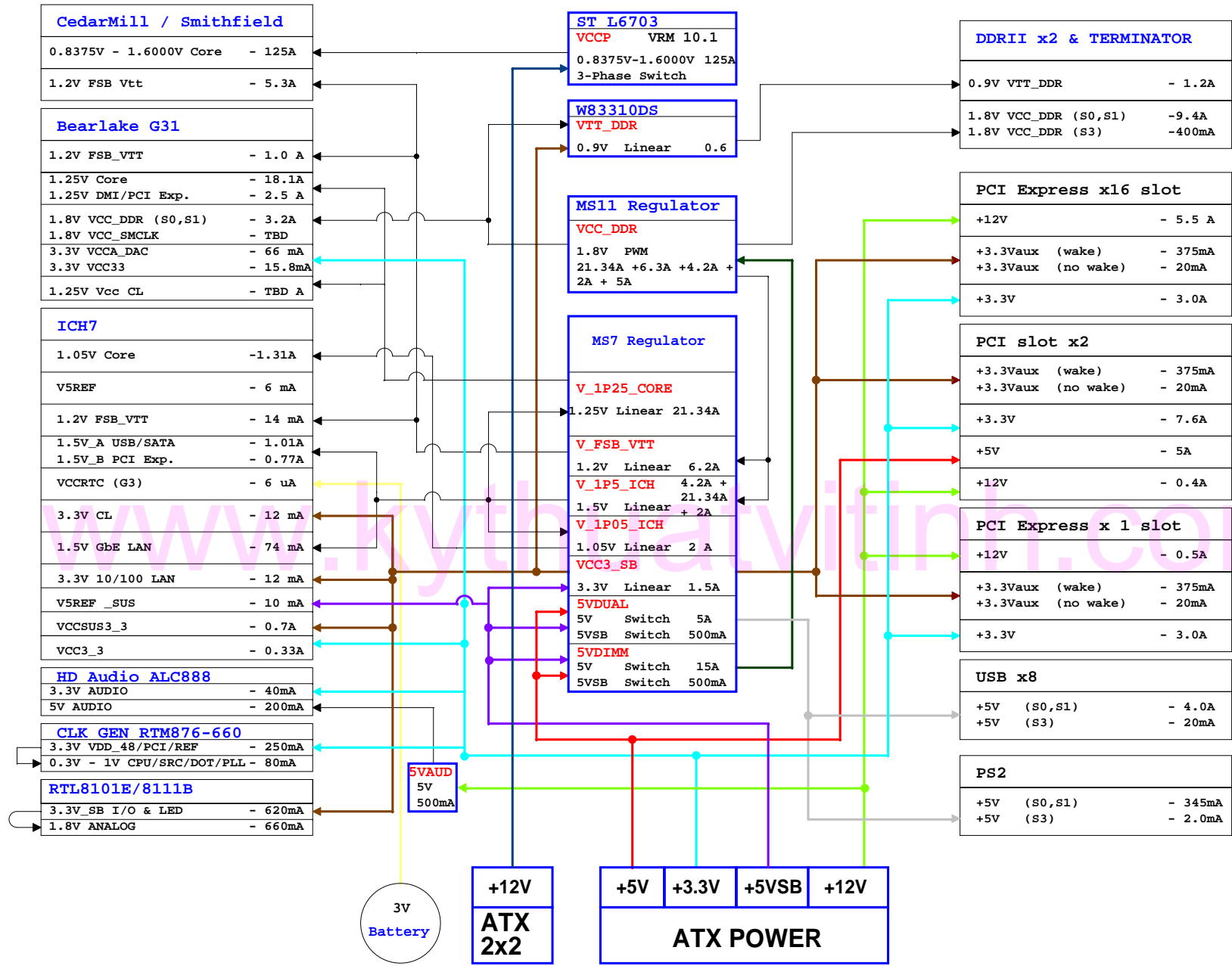
Block Diagram

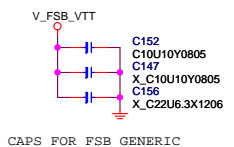
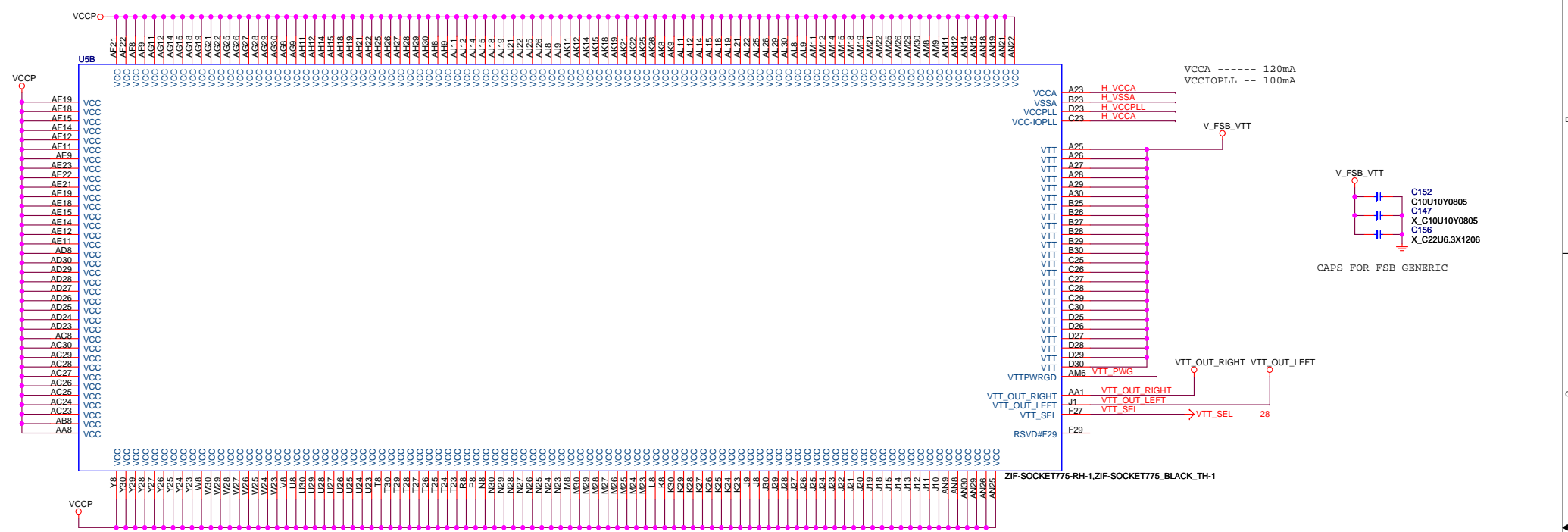


CLOCK MAP

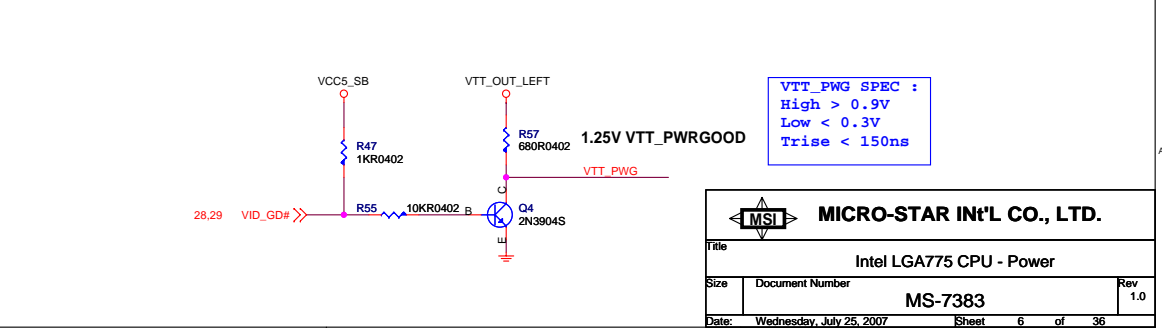
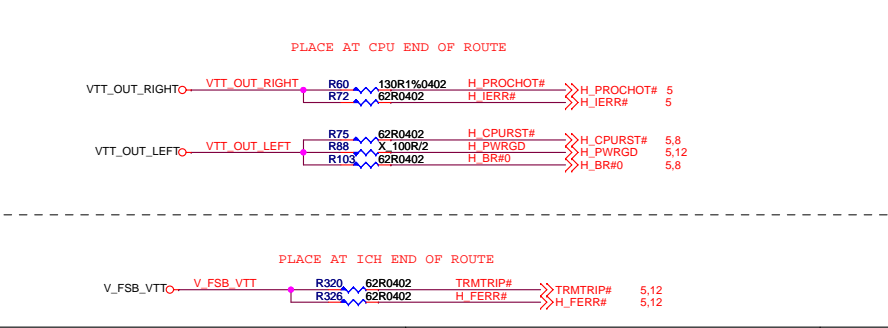
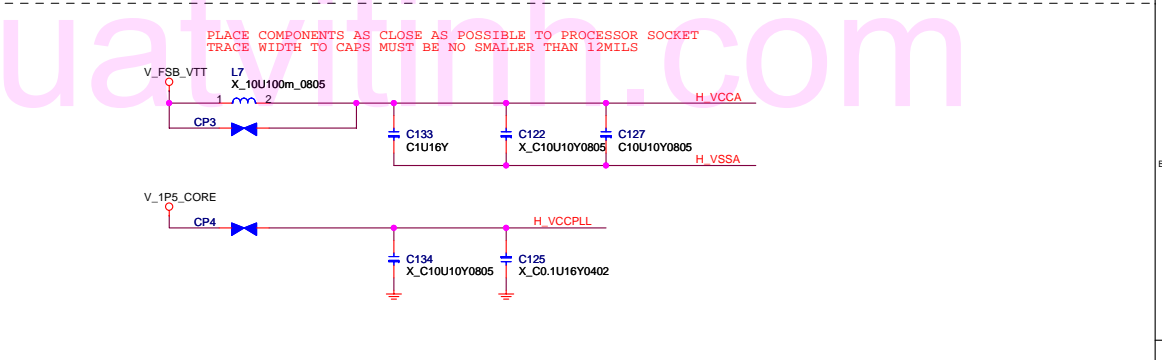
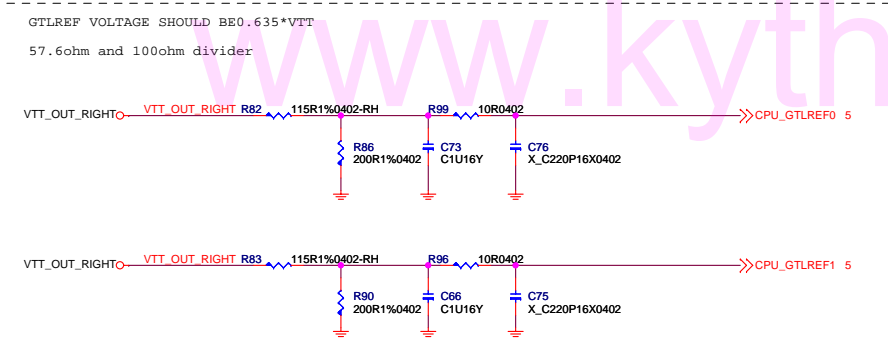


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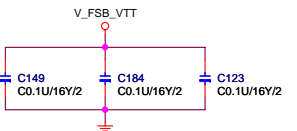
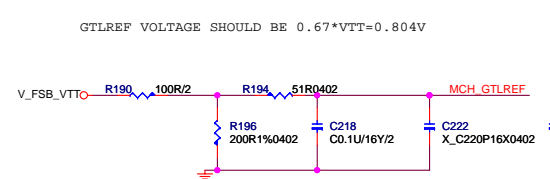
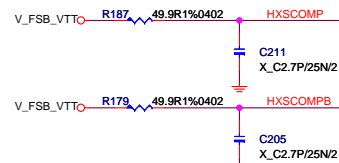
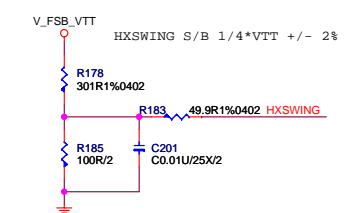
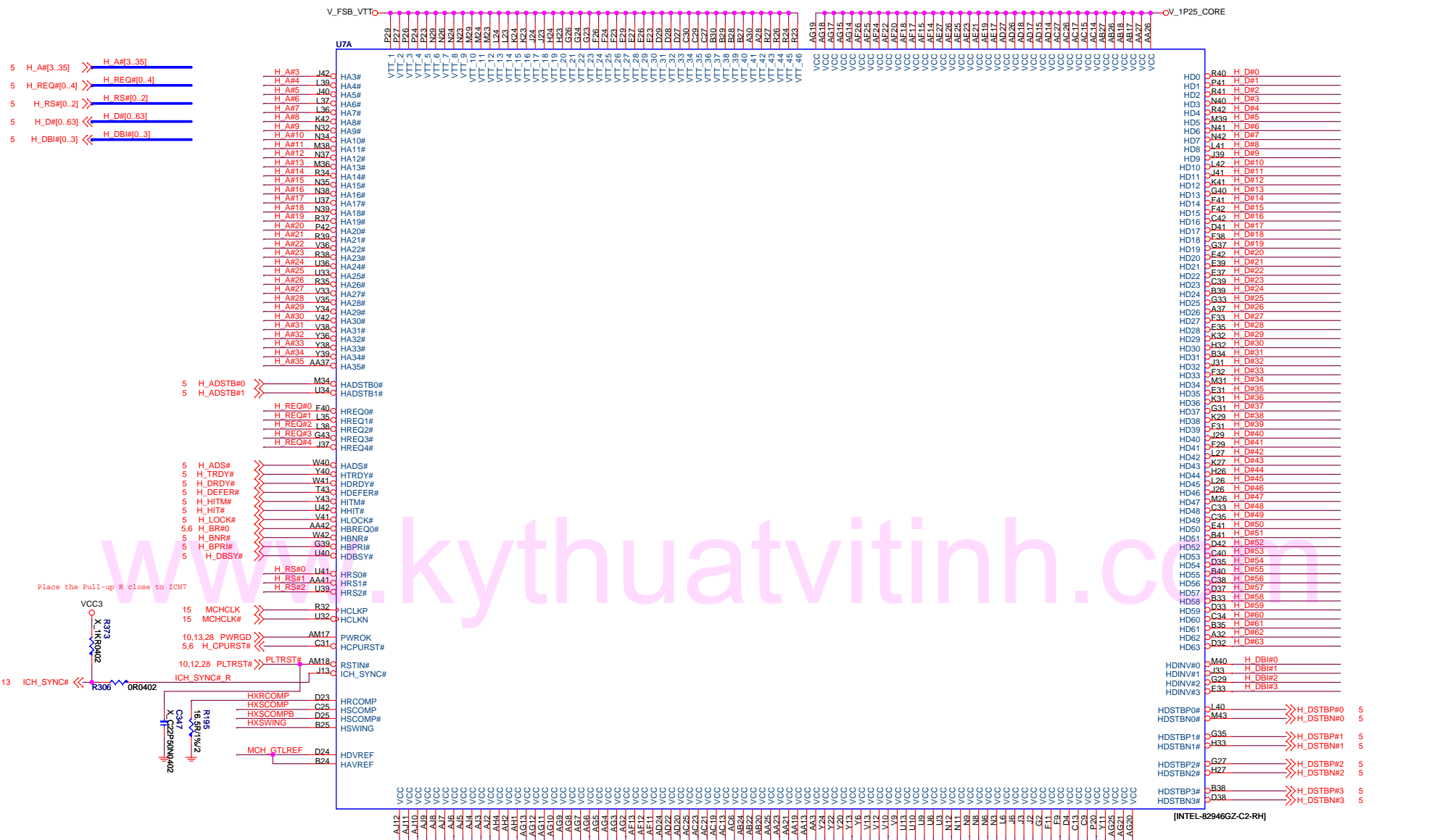




CAPS FOR FSB GENERIC



MICRO-STAR INT'L CO., LTD.		
Title Intel LGA775 CPU - Power		
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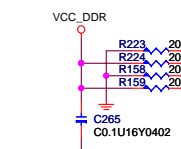
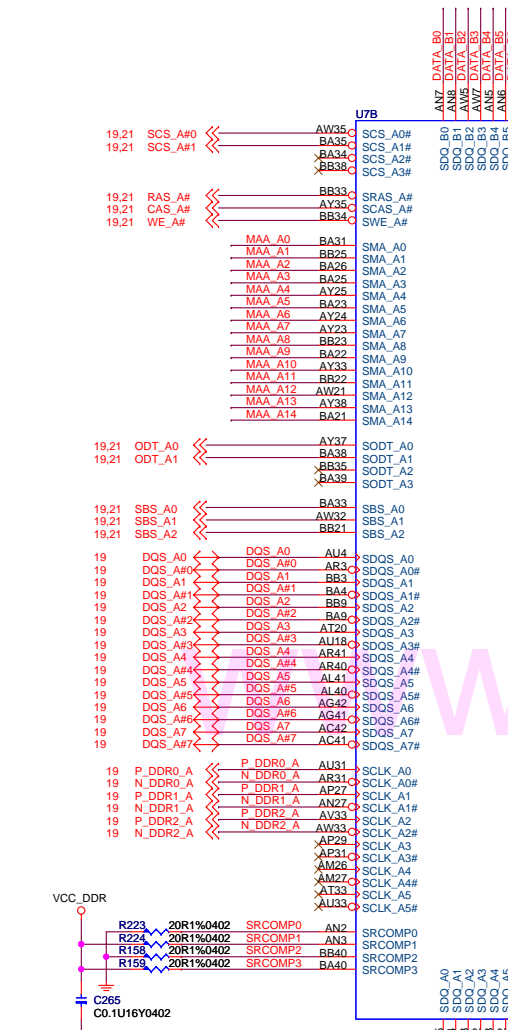


MICRO-STAR INT'L CO., LTD.

Title: **Intel Bearlake G31 - CPU Signals**

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20 DATA_B[0..63] <-> DATA_B[0..63] 20 DQM_B[0..7] <-> DQM_B[0..7]
 19 DATA_A[0..63] <-> DATA_A[0..63] 19 DQM_A[0..7] <-> DQM_A[0..7]
 19,21 MAA_A[0..14] <-> MAA_A[0..14] 20,21 MAA_B[0..14] <-> MAA_B[0..14]



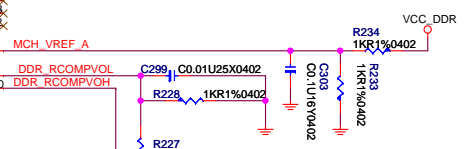
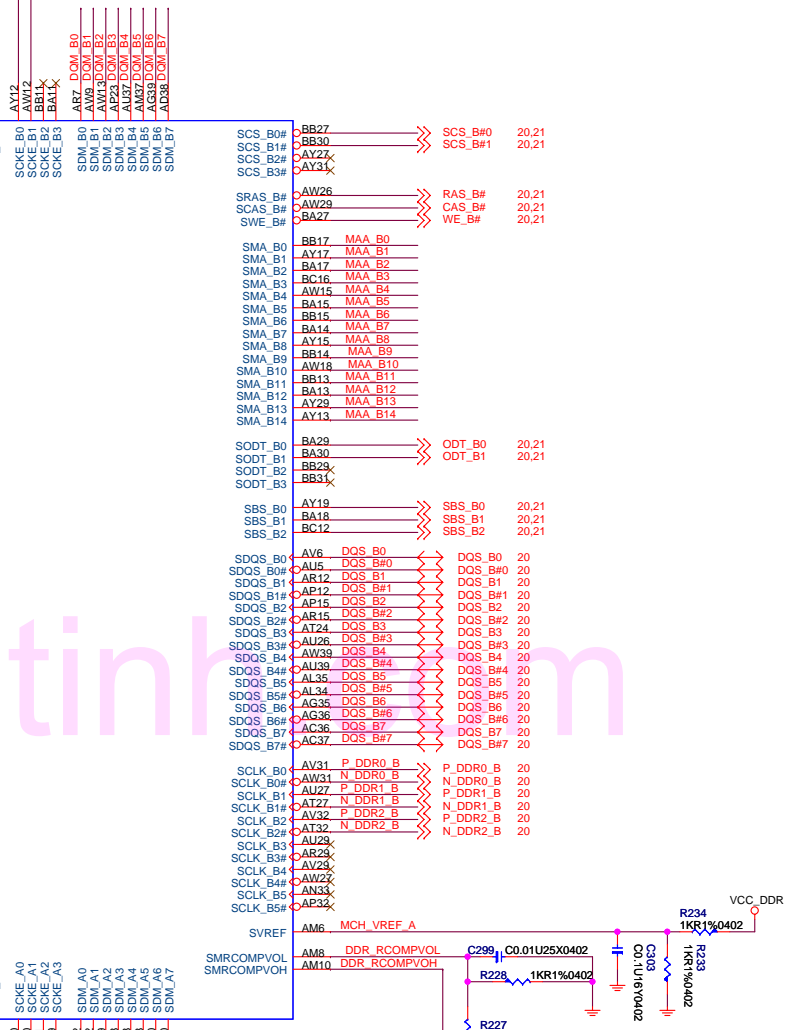
[INTEL-82946GZ-C2-RH]



SCKE_B0 <-> SCKE_B0 20,21
 SCKE_B1 <-> SCKE_B1 20,21

SCKE_A1 <-> SCKE_A1 19,21
 SCKE_A0 <-> SCKE_A0 19,21

PLACE 0.1UF CAP CLOSE TO MCH



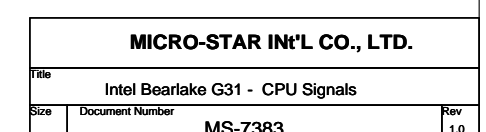
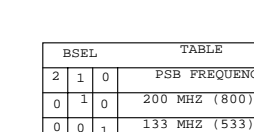
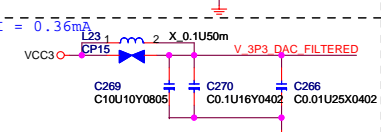
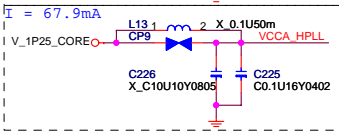
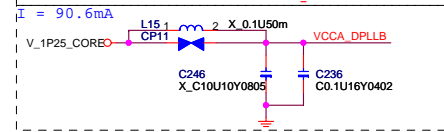
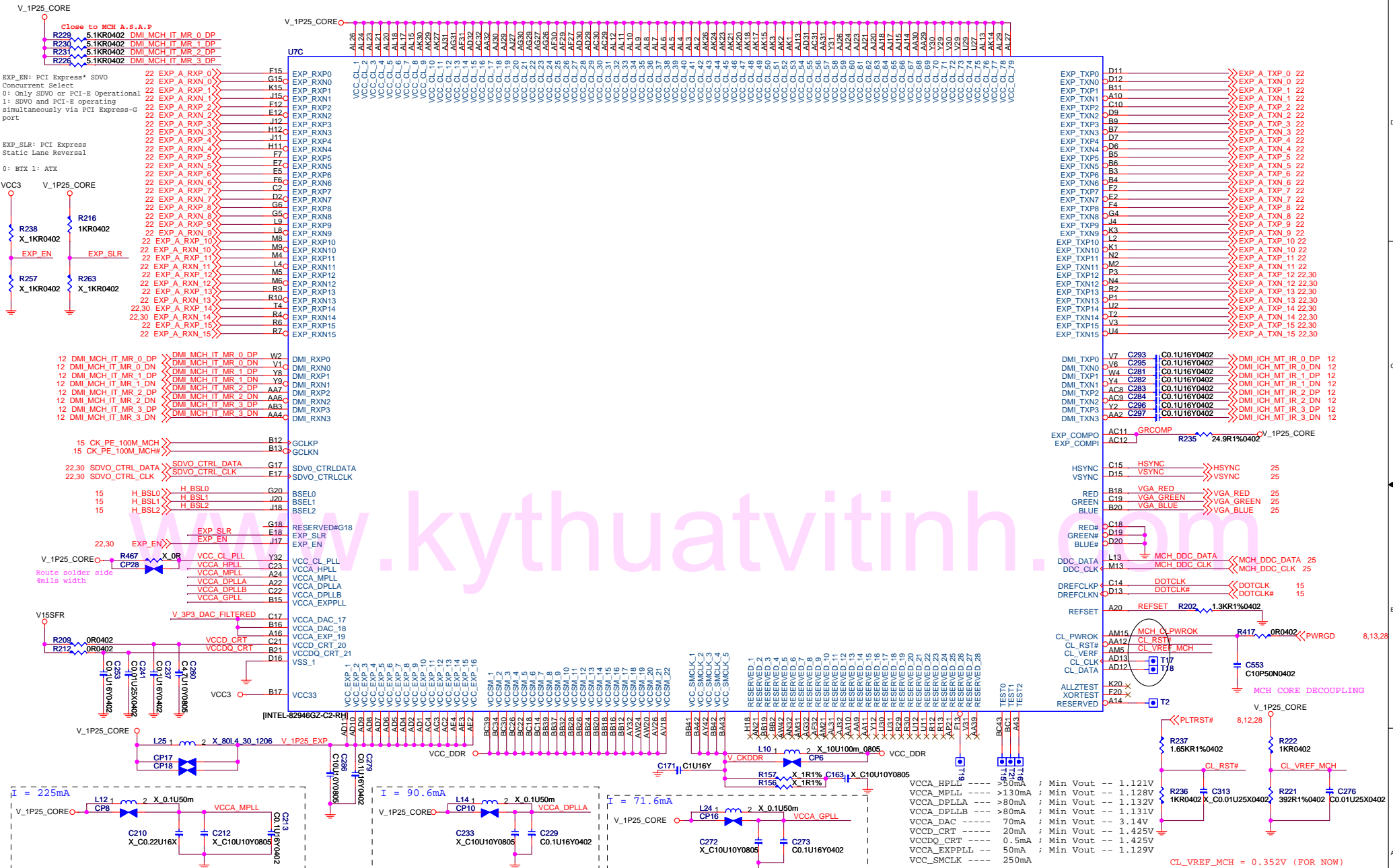
DDR_RCOMPVOL = 0.8 * VCC_DDR
 DDR_RCOMPVOL = 0.2 * VCC_DDR

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Title Intel Bearlake G31 - CPU Signals

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BSEL		TABLE	
2	1	0	PSB FREQUENCY
0	1	0	200 MEHZ (800)
0	0	1	133 MHZ (533)

VCCA_HPLL	<< 0mA	Min Vout	-- 1.121V
VCCA_MPLL	>130mA	Min Vout	-- 1.128V
VCCA_DPLLA	>80mA	Min Vout	-- 1.132V
VCCA_DPLLB	>80mA	Min Vout	-- 1.131V
VCCA_DAC	70mA	Min Vout	-- 3.14V
VCCD_CRT	20mA	Min Vout	-- 1.425V
VCCDQ_CRT	0.5mA	Min Vout	-- 1.425V
VCCA_EXPPLL	50mA	Min Vout	-- 1.129V
VCC_SMCLK	250mA		

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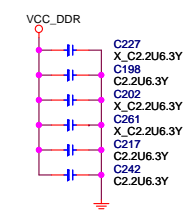
Intel Bearlake G31 - CPU Signals

Size	Document Number	Rev
	MS-7383	1.0

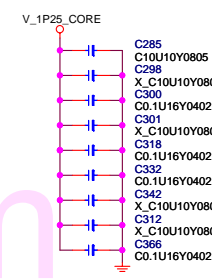
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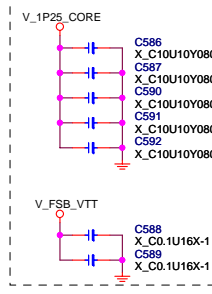
Place close to GMCH



MCH CORE DECOUPLING



5020 Parts



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Title Intel Bearlake G31 - CPU Signals		
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23 AD[0..31] <-> AD[0..31]
 23 C_BE#[0..3] <-> C_BE#[0..3]
 23 PREQ#[0..5] <-> PREQ#[0..5]

U16A

AD0 E18 AD0
 AD1 C18 AD1
 AD2 A16 AD2
 AD3 F18 AD3
 AD4 E16 AD4
 AD5 A18 AD5
 AD6 E17 AD6
 AD7 A16 AD7
 AD8 A16 AD8
 AD9 C14 AD9
 AD10 E14 AD10
 AD11 D14 AD11
 AD12 B12 AD12
 AD13 C13 AD13
 AD14 G15 AD14
 AD15 G13 AD15
 AD16 E12 AD16
 AD17 C11 AD17
 AD18 D11 AD18
 AD19 A11 AD19
 AD20 A10 AD20
 AD21 F11 AD21
 AD22 F10 AD22
 AD23 E9 AD23
 AD24 D9 AD24
 AD25 B9 AD25
 AD26 A8 AD26
 AD27 A8 AD27
 AD28 C7 AD28
 AD29 B6 AD29
 AD30 E6 AD30
 AD31 D6 AD31

C_BE#0 B15 C/BE0#
 C_BE#1 C12 C/BE1#
 C_BE#2 D12 C/BE2#
 C_BE#3 C15 C/BE3#

23 DEVSEL# <-> A12 DEVSEL#
 23 FRAME# <-> F12 FRAME#
 23 IRDY# <-> F14 IRDY#
 23 TRDY# <-> F15 TRDY#
 23 STOP# <-> E15 STOP#
 23 PAR <-> E14 PAR
 23 LOCK# <-> B10 PLOCK#
 23 SERIR# <-> C9 SERIR#
 23 PERR# <-> C9 PERR#
 23 PCI_PME# <-> B19 PCI_PME#

15 ICH_PCLK <-> A9 PCICLK
 23 PCIRST# <-> B18 PCIRST#

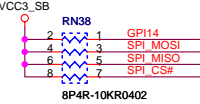
PREQ#0 D7 REQ0#
 PREQ#1 C16 REQ1#
 PREQ#2 C17 REQ2#
 PREQ#3 E13 REQ3#
 PREQ#4 A13 REQ4#
 PREQ#5 C8 REQ5#

23 PGNT#0 <-> E7 GNT0#
 23 PGNT#1 <-> D16 GNT1#
 23 PGNT#2 <-> D17 GNT2#
 23 PGNT#3 <-> E13 GNT3#
 23 PGNT#4 <-> A14 GPIO48/GNT4#
 23 PGNT#5 <-> D8 GPIO17/GNT5#

23 PIRO#A <-> A3 PIROA#
 23 PIRO#B <-> B4 PIROB#
 23 PIRO#C <-> C5 PIROC#
 23 PIRO#D <-> B5 PIROD#
 23 PIRO#E <-> G6 GPIO2/PIROE#
 23 PIRO#F <-> F7 GPIO3/PIROF#
 23 PIRO#G <-> F8 GPIO4/PIROG#
 23 PIRO#H <-> G7 GPIO5/PIROH#

16 SERIRQ <-> AH21 SERIRQ
 24 IDE_IRQ <-> AH16 IDEIRQ

SPI_MOSI R410 47R0402 SPI_MOSI_F P5 SPI_MOSI
 SPI_CS# R409 47R0402 SPI_CS_F# P6 SPI_MISO
 SPI_CLK R411 47R0402 SPI_CLK_F R2 SPI_CLK
 SPI_ARB P1 SPI_ARB



PCI INTERFACE

ICH 7
 PART 1/3

INTERRUPT SPI

CPU

PCI EXPRESS

DIRECT MEDIA

LAN

A20M# <-> AH28 H_A20M# 5
 CPUSLP# <-> AG27X
 FERR# <-> AG26 H_FERR# 5,6
 IGNNE# <-> AG22 H_IGNNE# 5
 INIT# <-> AF22 H_INIT# 5
 INIT3_3V# <-> AG21 T24
 INTR <-> AF25 H_INTR 5
 NMI <-> AF23 H_NMI 5
 SM# <-> AH24 ICH_H_SM# 5
 STPCLK# <-> AH22 H_STPCLK# 5
 RCIN# <-> AG23 KBRST# 16
 A20GATE <-> AE22 A20GATE 16
 TRMTRIP# <-> AF26 TRMTRIP# 5,6
 GPO4R/CPUPWRGD <-> AG24 H_PWRGD 5,6

PLTRST# <-> C26 PLTRST L R322 33R0402 PLTRST# 8,10,28
 PERN_1 <-> F26 HSI_N1 HSI_N1 31
 PERP_1 <-> F25 HSI_P1 HSI_P1 31
 PETN_1 <-> E28 HSO_P1 C C662 C0.1U16Y0402 HSO_N1 HSO_N1 31
 PETP_1 <-> E27 HSO_P1 C C663 C0.1U16Y0402 HSO_P1 HSO_P1 31

PERN_2 <-> H26 X
 PERP_2 <-> H25 X
 PETN_2 <-> G28 X
 PETP_2 <-> G27 X

PERN_3 <-> K26 HSI_N3 HSI_N3 18
 PERP_3 <-> K25 HSI_P3 HSI_P3 18
 PETN_3 <-> J28 HSO_N3 C C415 C0.1U16Y0402 HSO_N3 HSO_N3 18
 PETP_3 <-> J27 HSO_P3 C C414 C0.1U16Y0402 HSO_P3 HSO_P3 18

PERN_4 <-> M26 X
 PERP_4 <-> M25 X
 PETN_4 <-> L28 X
 PETP_4 <-> L27 X

PERN_5 <-> P26 X
 PERP_5 <-> P25 X
 PETN_5 <-> N28 X
 PETP_5 <-> N27 X

PERN_6 <-> T26 X
 PERP_6 <-> T25 X
 PETN_6 <-> R28 X
 PETP_6 <-> R27 X

DML_0RXN <-> V26 DMI_ICH_MT_IR_0_DN DMI_ICH_MT_IR_0_DN 10
 DML_0RXP <-> U25 DMI_ICH_MT_IR_0_DP DMI_ICH_MT_IR_0_DP 10
 DML_0TXN <-> U28 DMI_ICH_IT_MR_0_DN C421 C0.1U16Y0402 DMI_ICH_IT_MR_0_DN 10
 DML_0TXP <-> U27 DMI_ICH_IT_MR_0_DP C422 C0.1U16Y0402 DMI_MCH_IT_MR_0_DP 10

DML_1RXN <-> V26 DMI_ICH_MT_IR_1_DN DMI_ICH_MT_IR_1_DN 10
 DML_1RXP <-> Y25 DMI_ICH_MT_IR_1_DP DMI_ICH_MT_IR_1_DP 10
 DML_1TXN <-> W28 DMI_ICH_IT_MR_1_DN C423 C0.1U16Y0402 DMI_ICH_IT_MR_1_DP 10
 DML_1TXP <-> W27 DMI_ICH_IT_MR_1_DP C424 C0.1U16Y0402 DMI_MCH_IT_MR_1_DP 10

DML_2RXN <-> AB26 DMI_ICH_MT_IR_2_DN DMI_ICH_MT_IR_2_DN 10
 DML_2RXP <-> AB25 DMI_ICH_MT_IR_2_DP DMI_ICH_MT_IR_2_DP 10
 DML_2TXN <-> AA28 DMI_ICH_IT_MR_2_DN C425 C0.1U16Y0402 DMI_ICH_IT_MR_2_DP 10
 DML_2TXP <-> AA27 DMI_ICH_IT_MR_2_DP C426 C0.1U16Y0402 DMI_MCH_IT_MR_2_DP 10

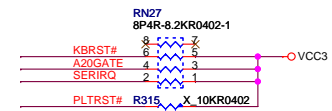
DML_3RXN <-> AD25 DMI_ICH_MT_IR_3_DN DMI_ICH_MT_IR_3_DN 10
 DML_3RXP <-> AD24 DMI_ICH_MT_IR_3_DP DMI_ICH_MT_IR_3_DP 10
 DML_3TXN <-> AC28 DMI_ICH_IT_MR_3_DN C427 C0.1U16Y0402 DMI_MCH_IT_MR_3_DN 10
 DML_3TXP <-> AC27 DMI_ICH_IT_MR_3_DP C428 C0.1U16Y0402 DMI_MCH_IT_MR_3_DP 10

DML_CLKN <-> AE28 CK_PE_100M_ICH# 15 V_DMI
 DML_CLKP <-> AE27 CK_PE_100M_ICH# 15
 DML_ZCOMP <-> C25 DMI_BIAS R318 24.9R1%0402
 DML_IRCOMP <-> D25

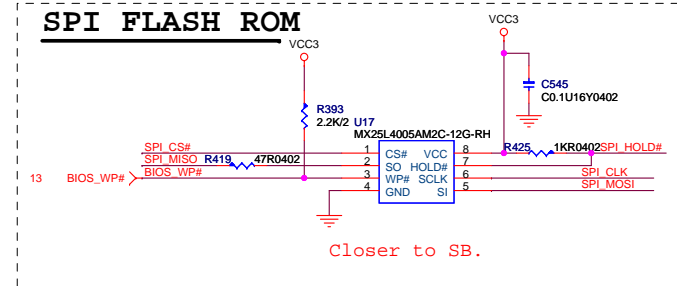
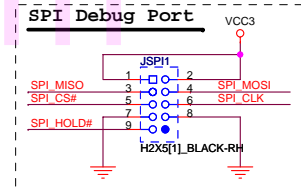
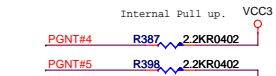
LAN_CLK <-> V3
 LAN_RSTSYNC <-> U3
 LAN_RXD0 <-> U5
 LAN_RXD1 <-> T5
 LAN_RXD2 <-> U7
 LAN_TXD0 <-> V6
 LAN_TXD1 <-> V7
 LAN_TXD2 <-> W7

EE_CS <-> W1
 EE_DIN <-> W3
 EE_DOUT <-> Y1
 EE_SHCLK <-> Y2

[INTEL-NH82801GB-A1-LF]



GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

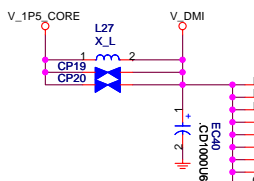


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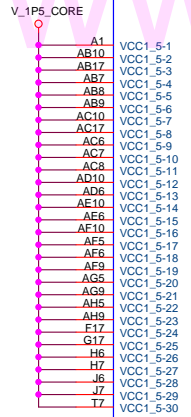
Title: Intel ICH7 - PCI & DMI & CPU & IRQ

Size: Document Number MS-7383

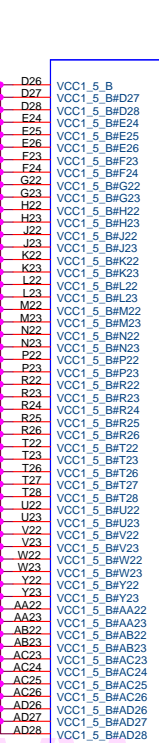
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Vcc1_5_B = 0.74A
Vcc1_5_A = 0.97A



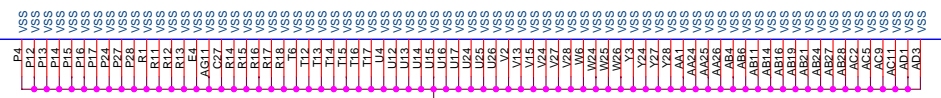
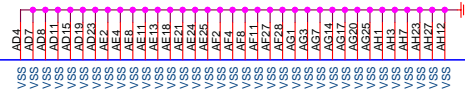
VCC1_05 ----- 1.31A
VCC1_5_A ----- 0.97A
VCC1_5_B ----- 0.74A
VCC3_3 ----- 0.58A
VCCSUS3_3 ----- 0.7A
V5REF ----- 6mA
V5REFSUS ----- 10mA
V_CPU_IO ----- 14mA



1.5V DMI POWER

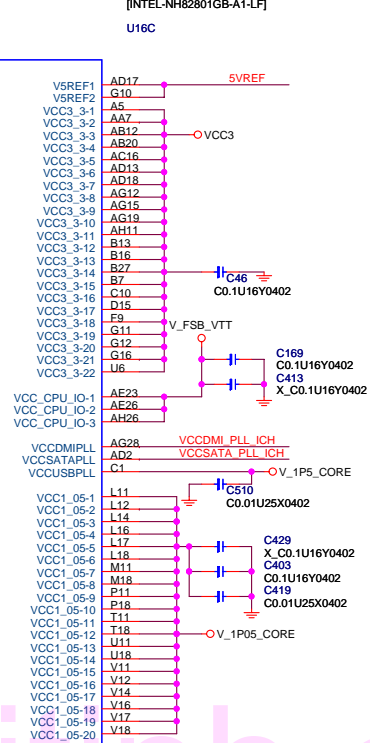
1.5V CORE WELL POWER

ICH 7
PART 3/3

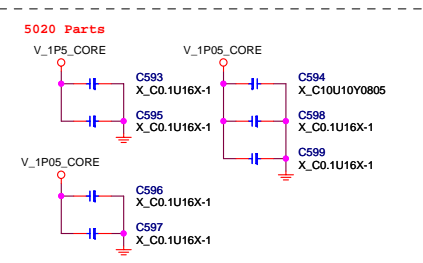
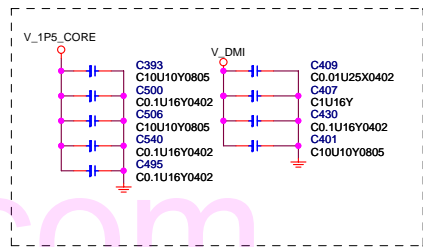
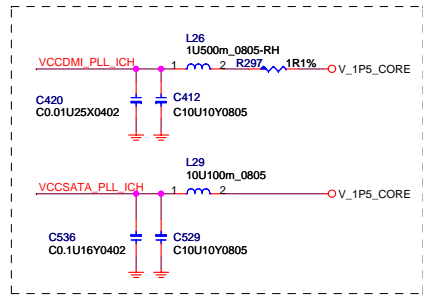
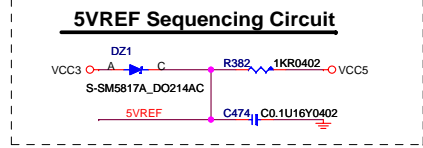


S0 POWER

S5 POWER



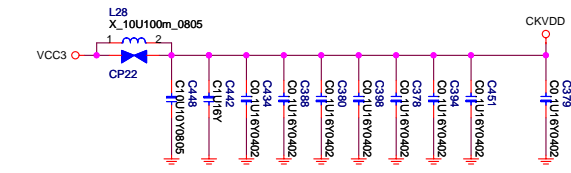
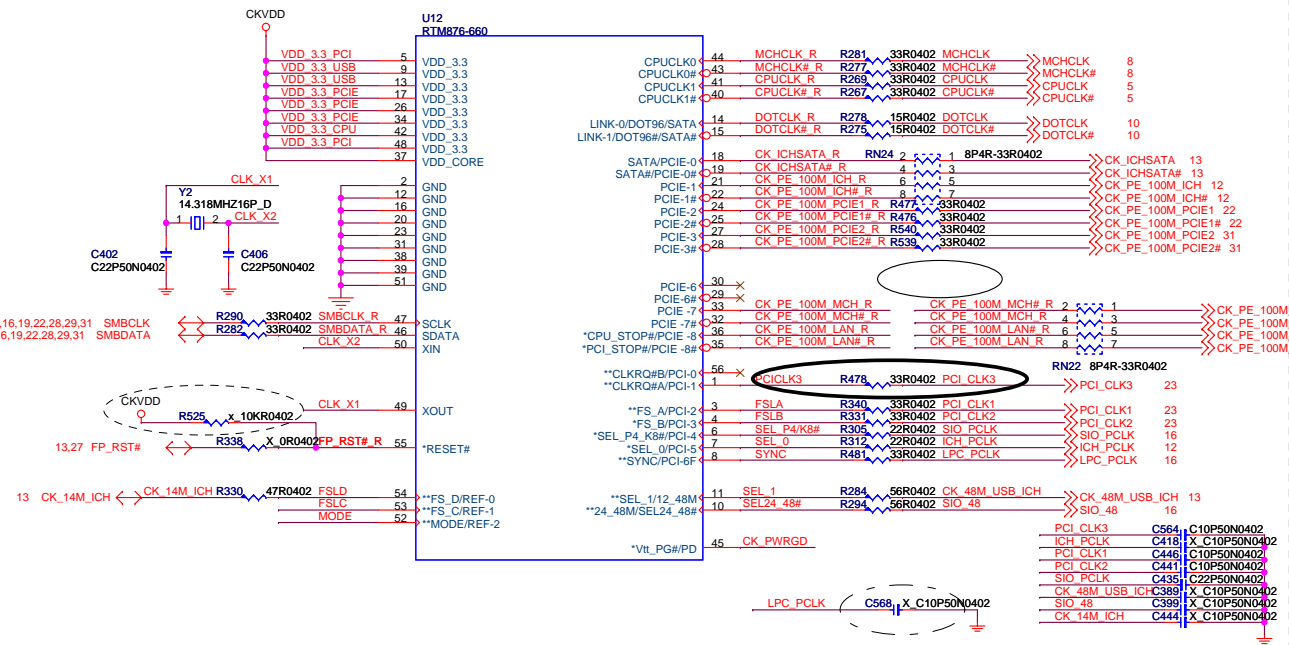
[INTEL-NH82801GB-A1-LF]
U16C



For HALT test, please place at bottom side under ICH7

Title Intel ICH7 - POWER		
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Clock Generator - RTM876-660

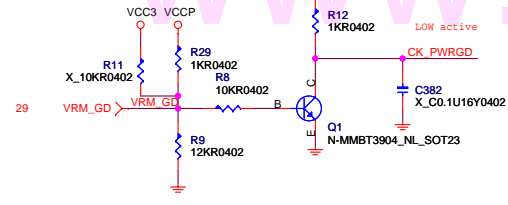


STRAPPING RESISTOR

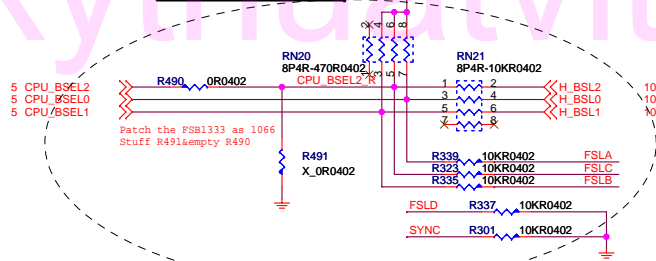
SEL_0	R298	10KR0402	CKVDD	SEL_I	SEL_0	Chipset Support
SEL_1	R279	10KR0402		SEL_0	SEL_0	SIS
				SEL_1	SEL_0	VIA
				SEL_0	SEL_1	Intel W/GEX
				SEL_P4/K8#		Intel
						Pin#40,41,43,44
SEL_P4/K8#	R316	10KR0402	CKVDD			K8 3.3V swing
				MODE		Pin#35/36
MODE	R314	10KR0402				PCI-E 8 T/C
						PCI_STOP#/CPU_STOP#
				SEL24_48#		Pin#10
						48Mhz
						24Mhz
				PCICLK3		Pin#1
						pci clk
						CLKREQ0

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	200M

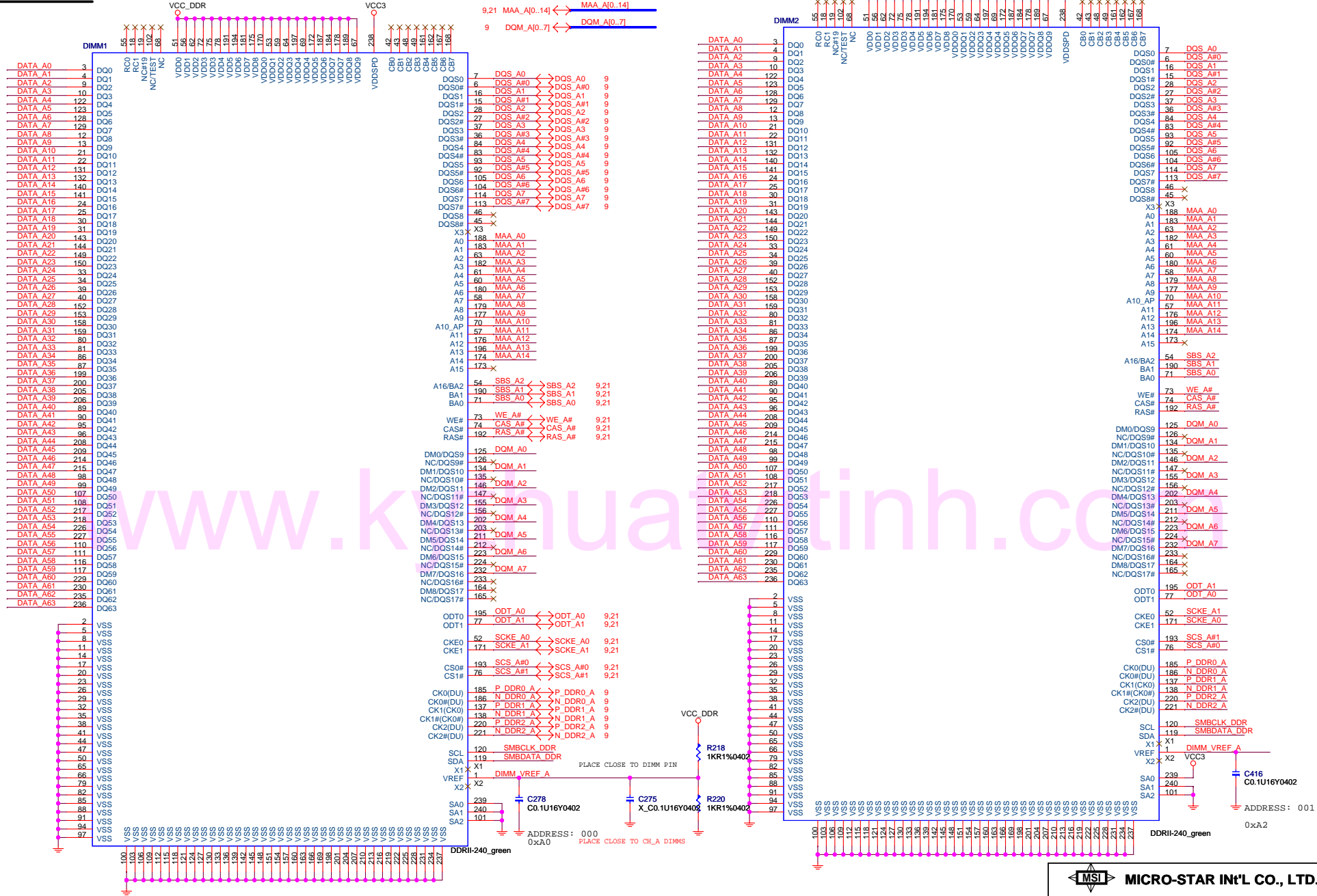
Clock Generator Power Good Block



CPU Frequency Selection



DDR2 CHANNEL A

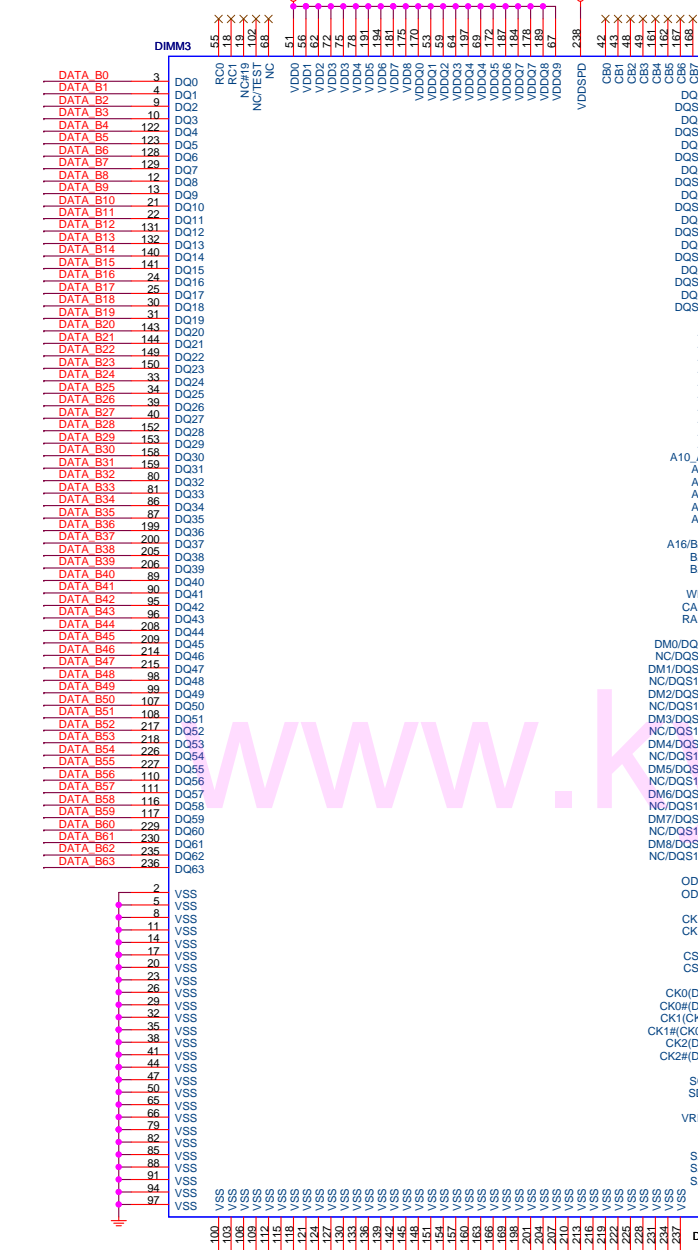


13,15,16,22,28,29,31 SMBCLK <-> R41 33R0402 <-> SMBCLK_DDR 20
13,15,16,22,28,29,31 SMBDATA <-> R53 33R0402 <-> SMBDATA_DDR 20



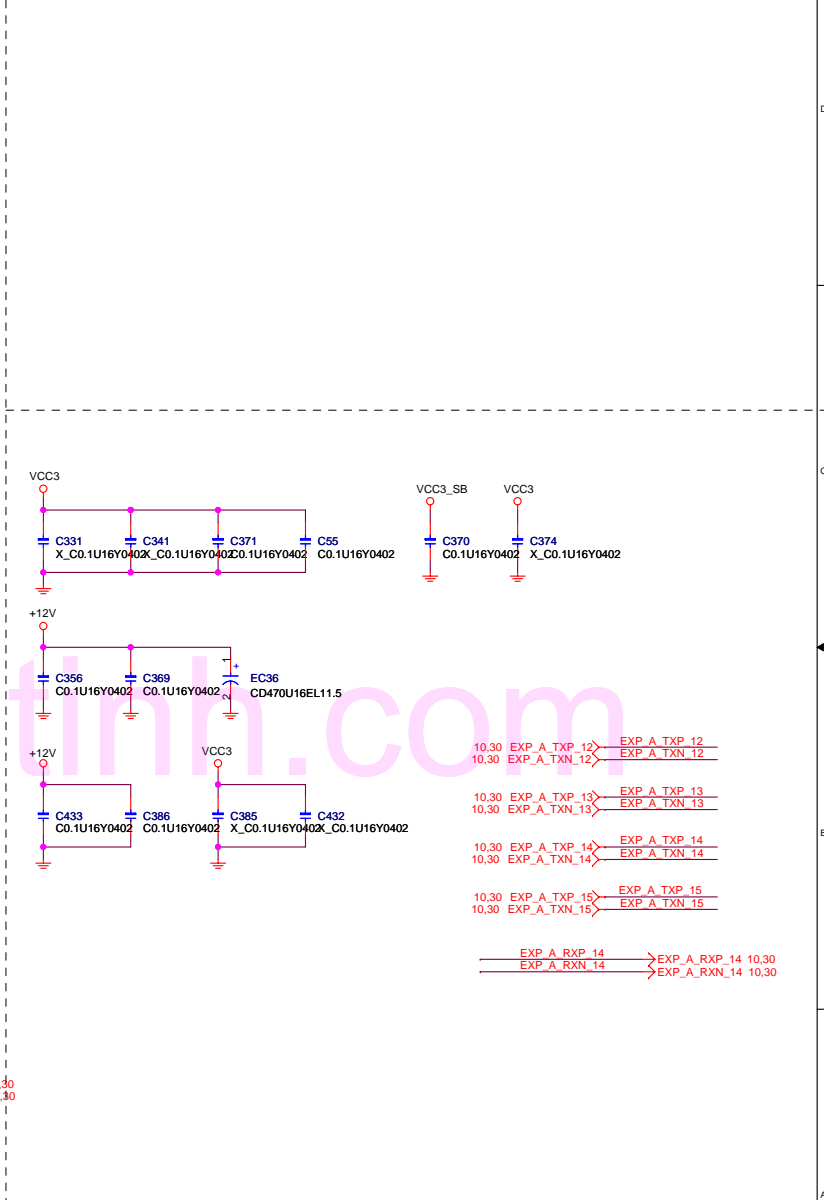
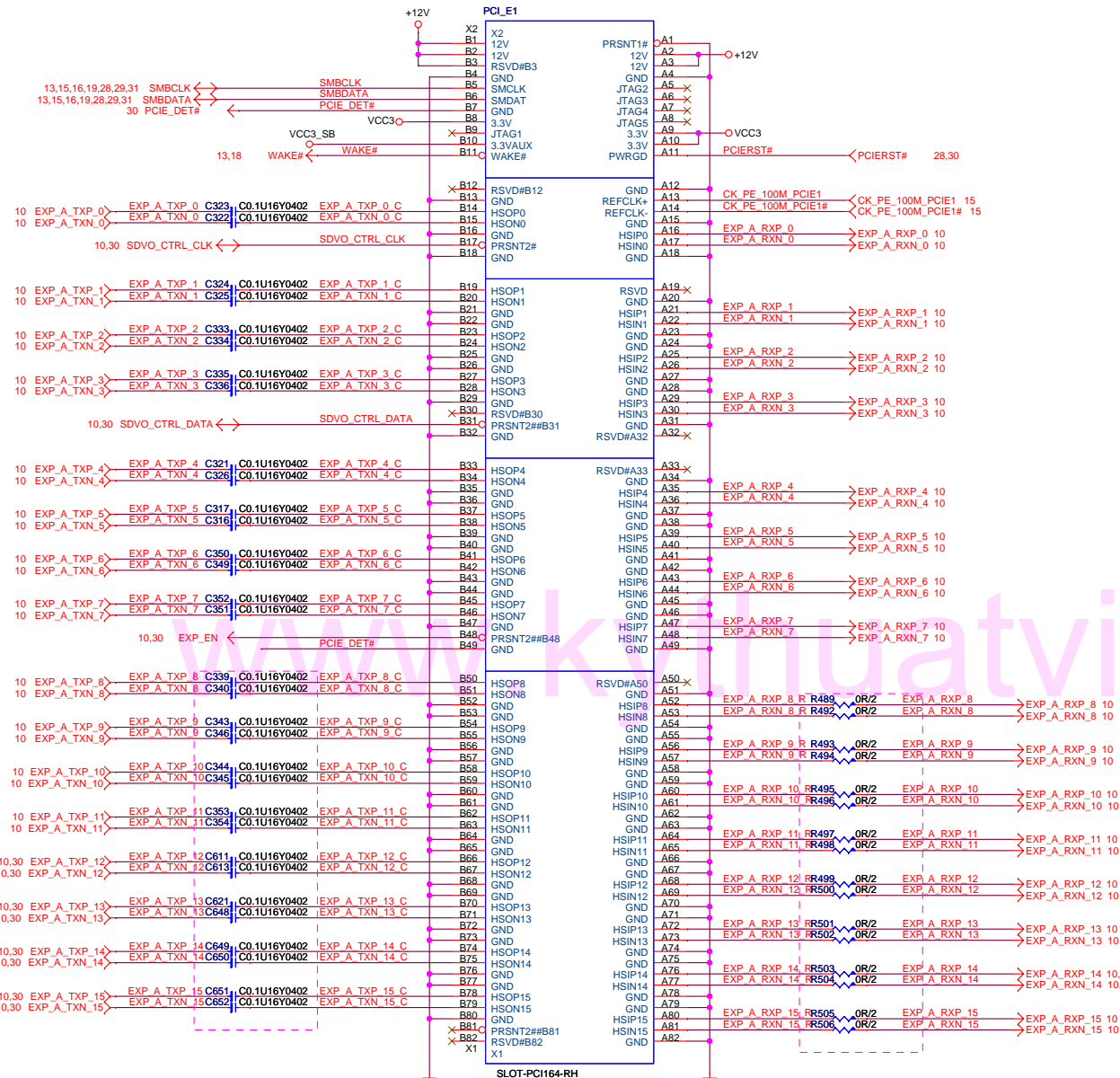
Table with 4 columns: Title (DDR II DIMM 1&2), Size, Document Number (MS-7383), Rev (1.0). Includes date and sheet information.

DDR2 CHANNEL B



PCI EXPRESS X16 PORT

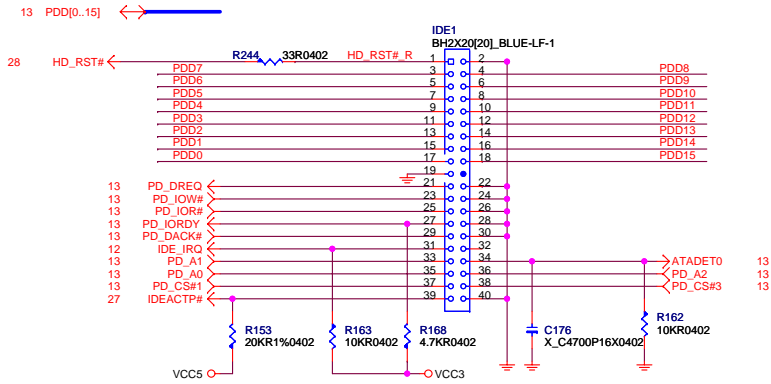
Dafault: N11-1640401-K06 (Default PCIE16 slot)
 有卡号的料號:N11-1640061-A10 (By customer option)



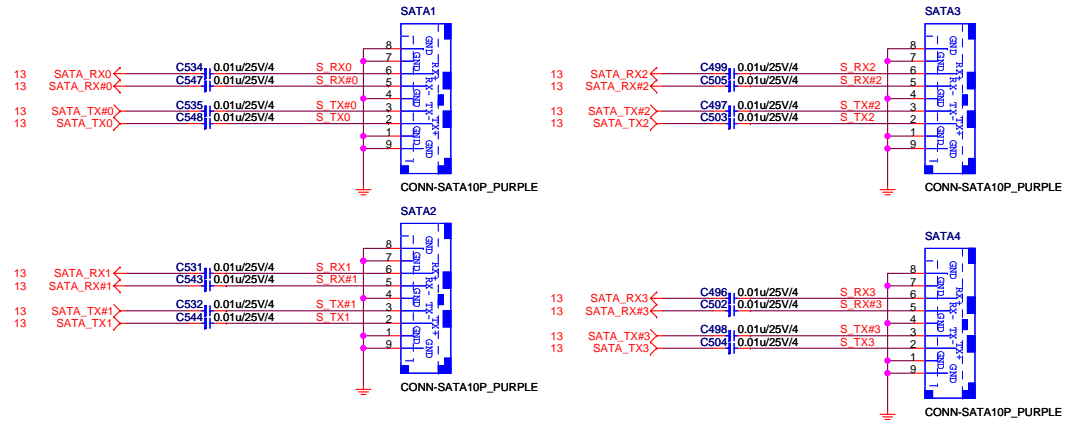
Stuff for Without Onboard DVI and PCI_E 16X
 Remove for Onboard DVI and PCI_E 16X

MSI MICRO-STAR INT'L CO., LTD.		
Title PCI EXPRESS X16 & X1 PORT		
Size	Document Number MS-7383	Rev 1.0
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ATA 33/66/100 IDE Connectors



SERIAL ATA CONNECTOR BLOCK



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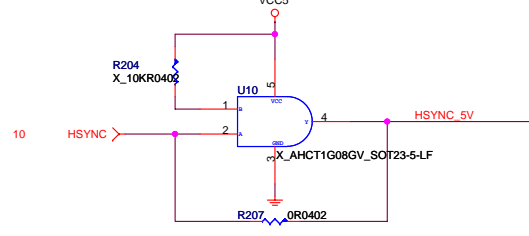
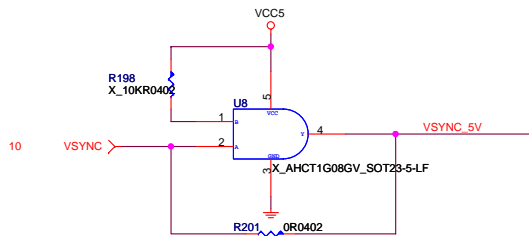
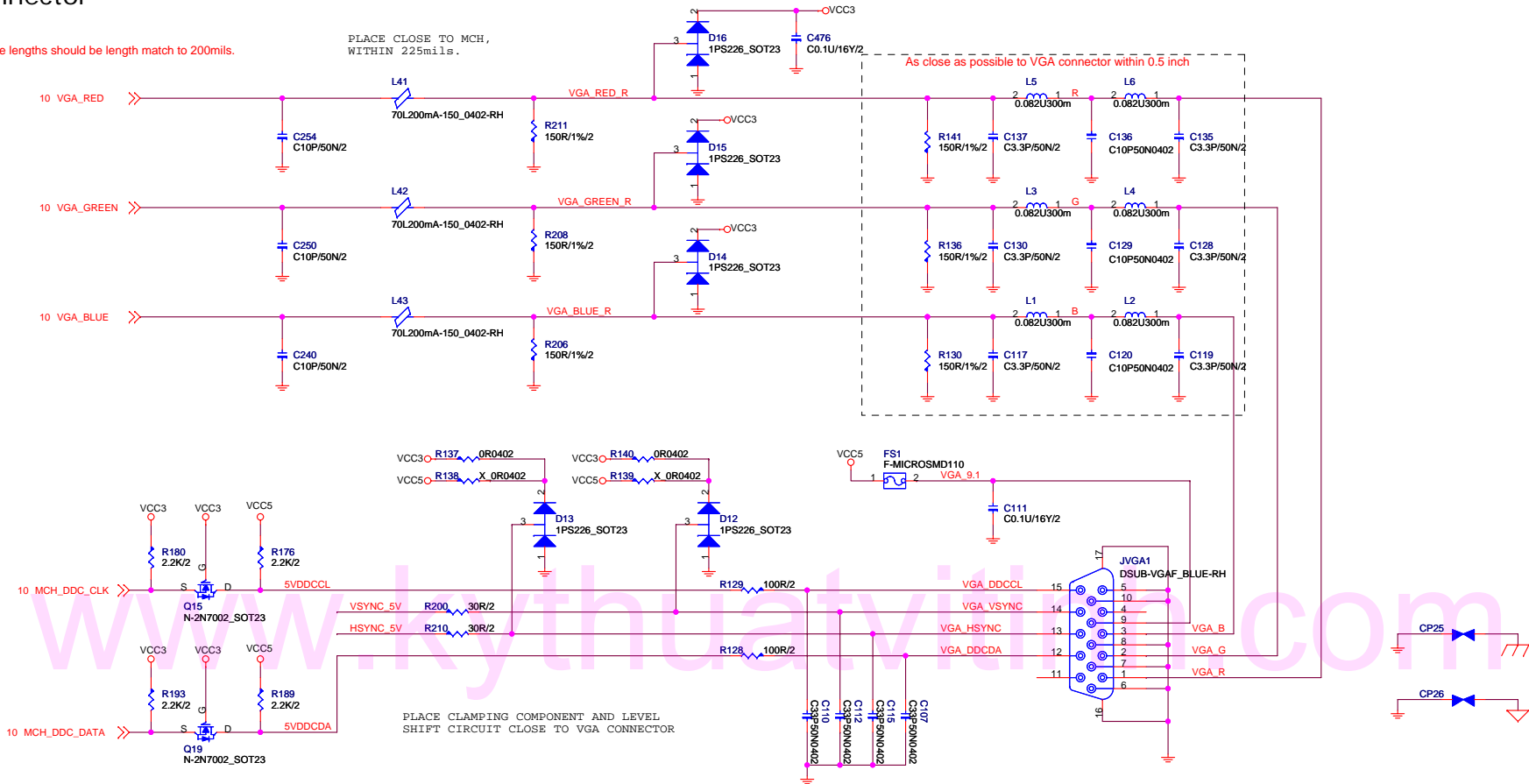
Video Connector

Thw R , G , B route lengths should be length match to 200mils.

PLACE CLOSE TO MCH,
WITHIN 225mils.

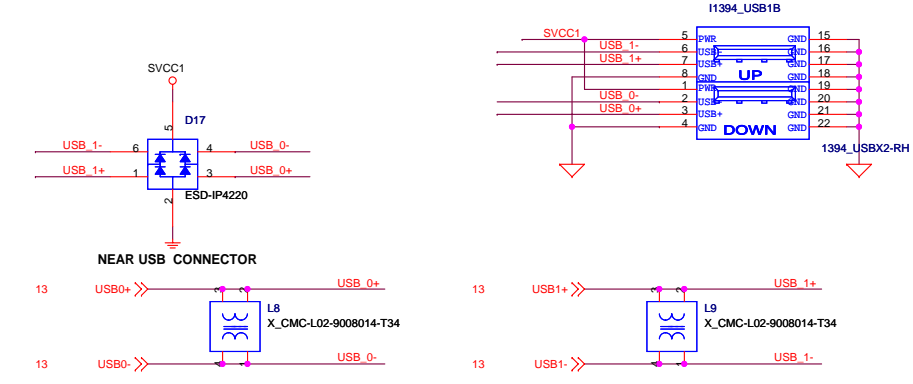
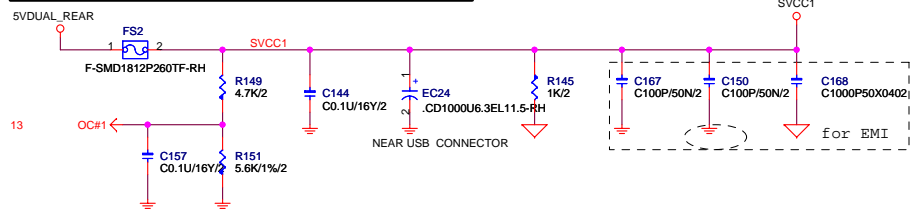
PLACE CLOSE TO VGA CONNECTOR

As close as possible to VGA connector within 0.5 inch

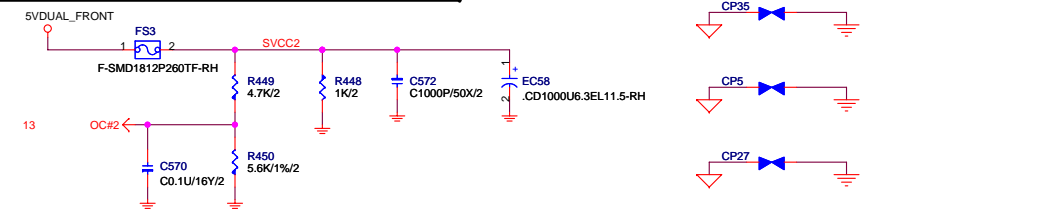


<OrgAddr1> MICRO-STAR INT'L CO., LTD.		
Title VGA connector		
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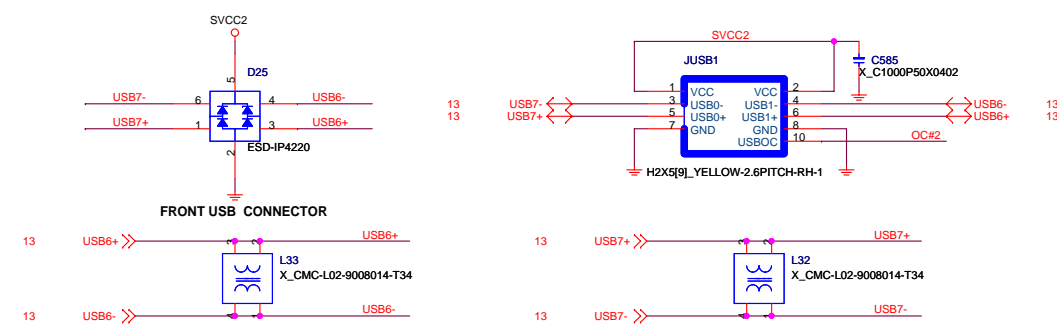
POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



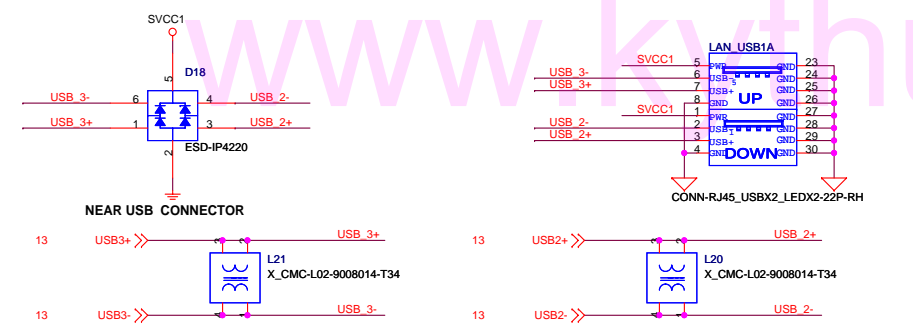
POWER CIRCUIT FOR USB PORT (FRONT)



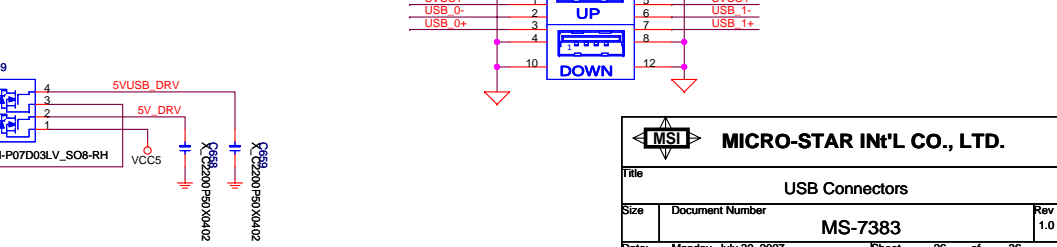
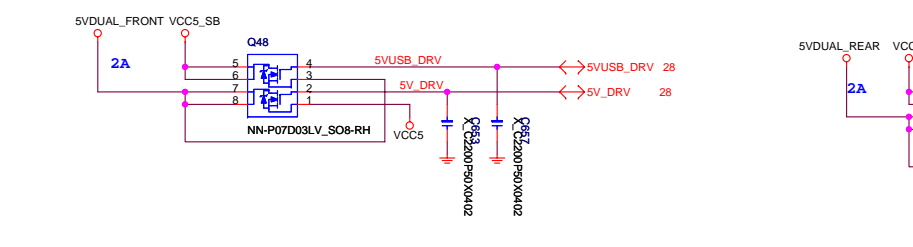
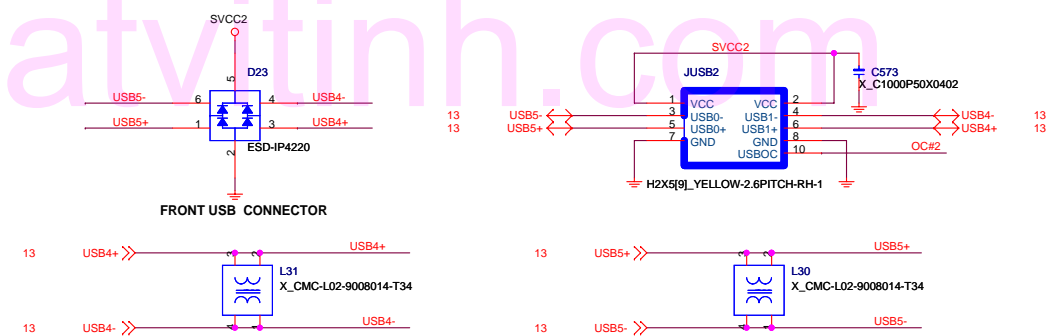
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



REAR PANEL USB CONNECTOR FOR USB PORT 2,3

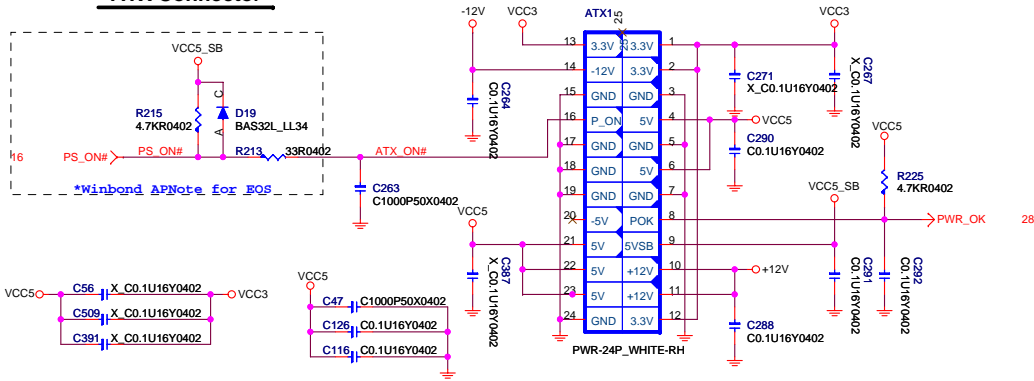


FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

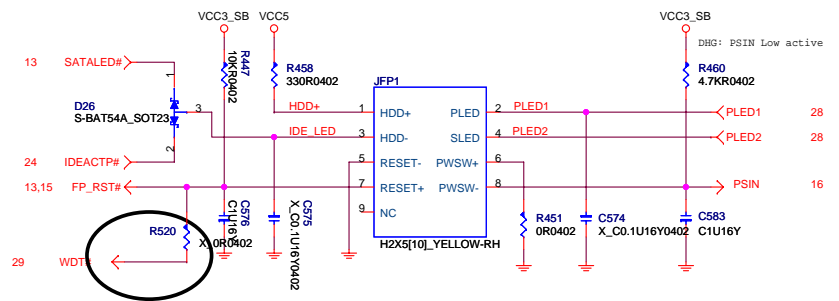


MSI MICRO-STAR INT'L CO., LTD.		
Title USB Connectors		
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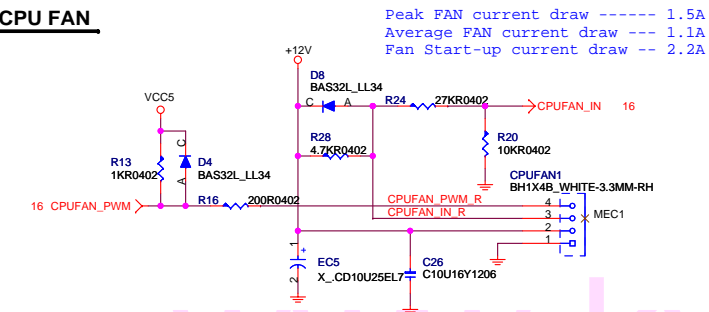
ATX Connector



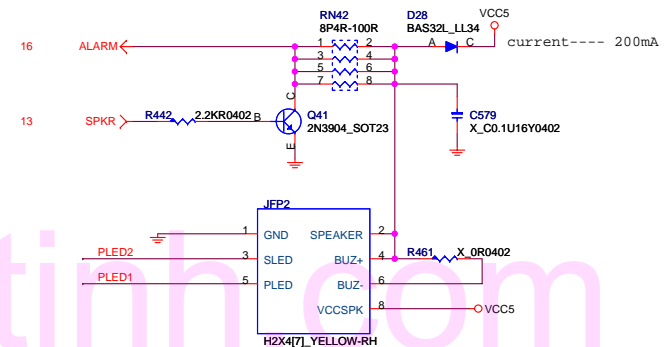
INTEL/PB Front Panel Connector



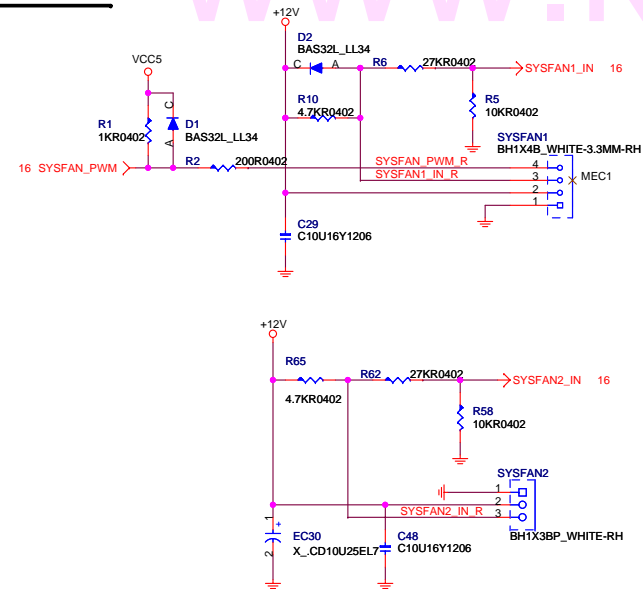
CPU FAN




MSI Front Panel Connector



SYSTEM FAN

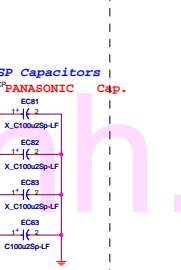
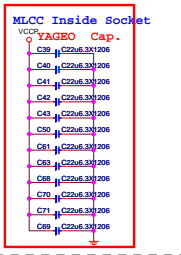
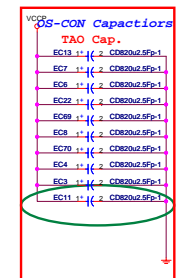
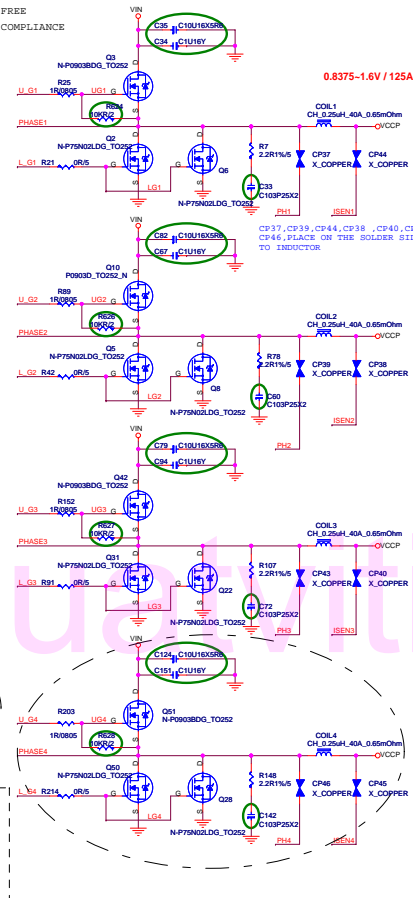
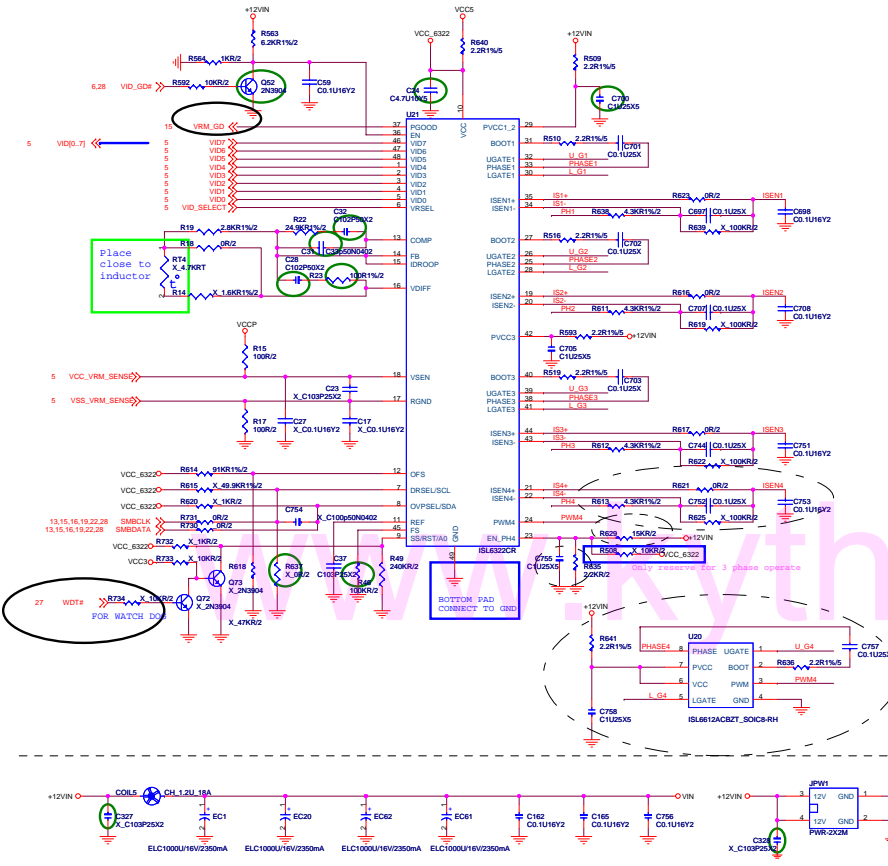


 MICRO-STAR INT'L CO., LTD.		
Title ATX Connector & Front Panel		
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Voltage Regular Module

ESR<13m ,Ripple
cur.<2.7A, Lc<12uA, 105C

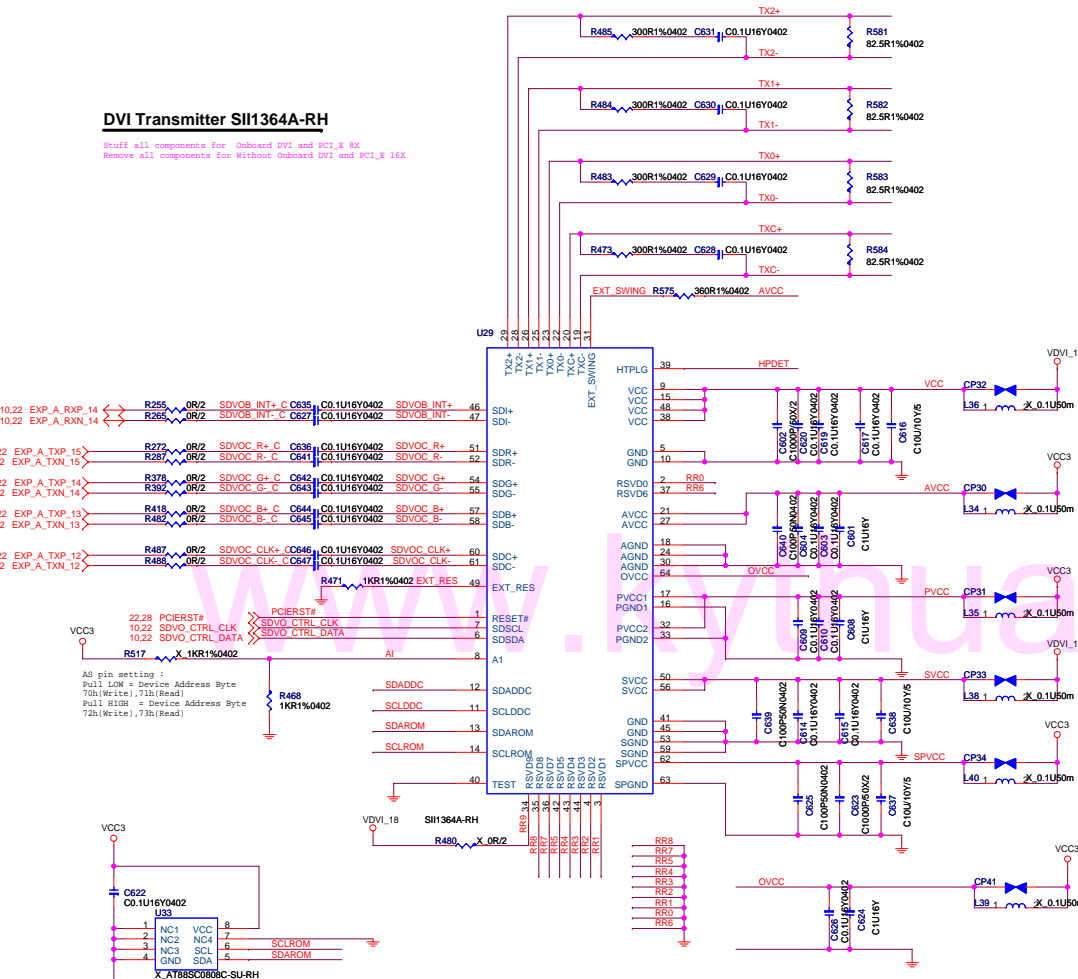
N-P0903BDG_TO252 mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5m (10V/25A),Vgs(on)=1-3V,Id=50A,Class=1800pf,Qg=50nC,Vds=25V,Vgs=±20V,RoHS compliance
P75N02LDG_TO252 mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7m (10V,30A),Vgs(on)=1-3V,Id=75A,Class=5000pf,Qg=140nC,Vds=25V,Vgs=±20V,RoHS compliance
C100U25P CAP_OS-CON,560u/4V,Dip-2/8*9/3.5mm,ESR<7mohm,Ripplecur.<6100mA,Lc.<500uA,SPEC series,RoHS compliance
CD560U40S-2 ESR<12m ,Ripplecur.<2350mA,105C, longlife change from 2000hrs to 3000hrs,KZJ
1800UF/6.3V 9.2mH CHOKE,0.25uH,20#,DIP/8.5mm,40A,0.6mOhm,,FEW,FERRITE,SQUARE,ROHS COMPLIANCE
CH-1.1U25A-LF IND CHOKE,1.1uH,20#,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,FEW,IRON,LEAD FREE
CD100U16L20-2 CAP,EL,1000u,16V,Dip-8x20/3.5mm,20#,12mOhm,2350mA,105C,3000hrs,ROHS COMPLIANCE



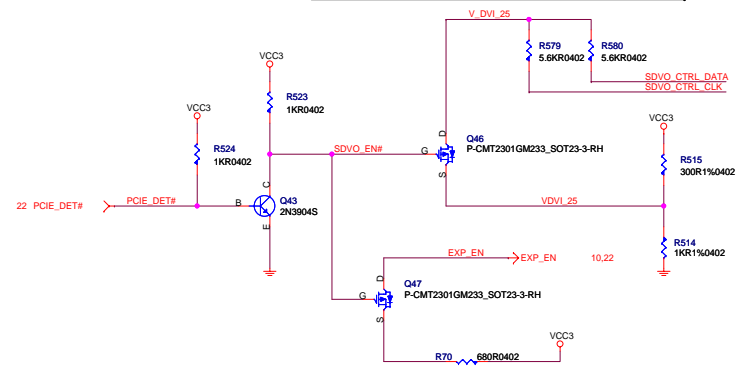
3P-9mos : EC13 use P/N:C94-6810421-p01(10 pcs)
C39 P/N:C11-1063047-y01(12pcs)
EC63 remove
Q3/Q10/q42 P/N:D03-0480900-O05
Q2/Q5/Q6/Q8/Q31/Q22 P/N:D03-60N032B-N03

DVI Transmitter SII1364A-RH

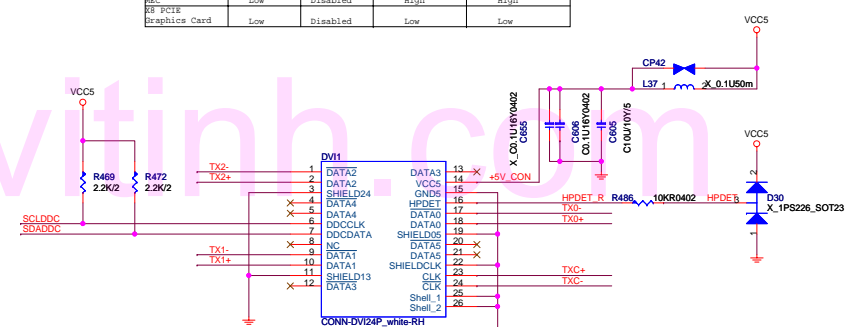
Stuff all components for Onboard DVI and PCI_#_8X
Remove all components for Without Onboard DVI and PCI_#_16X



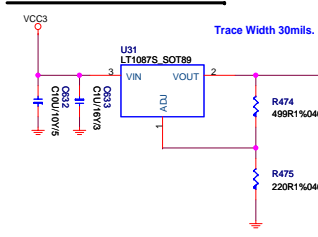
SDVO Concurrent PCIe Dynamic Switch Logic



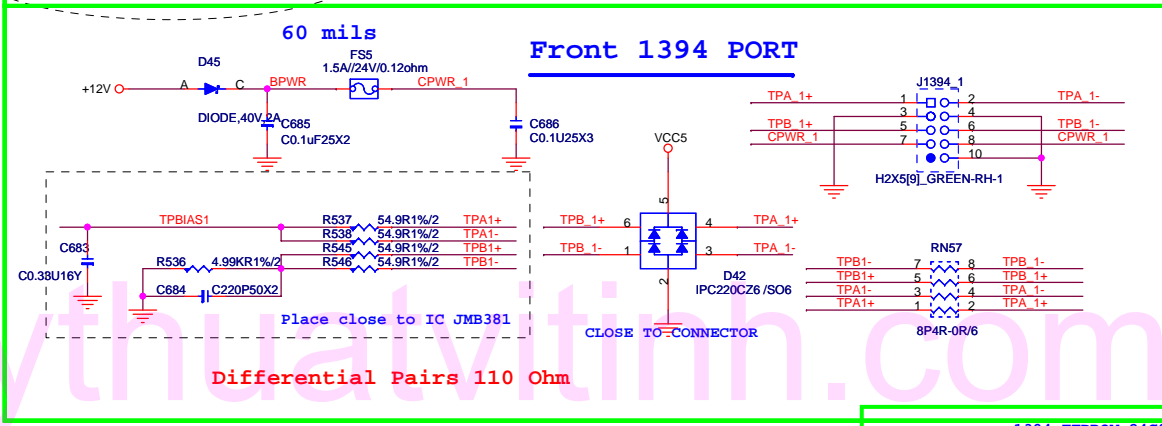
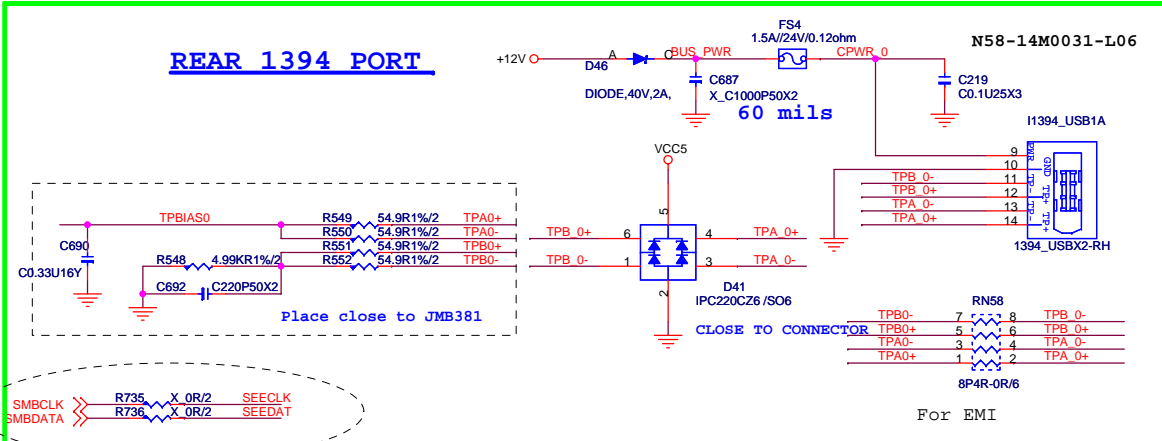
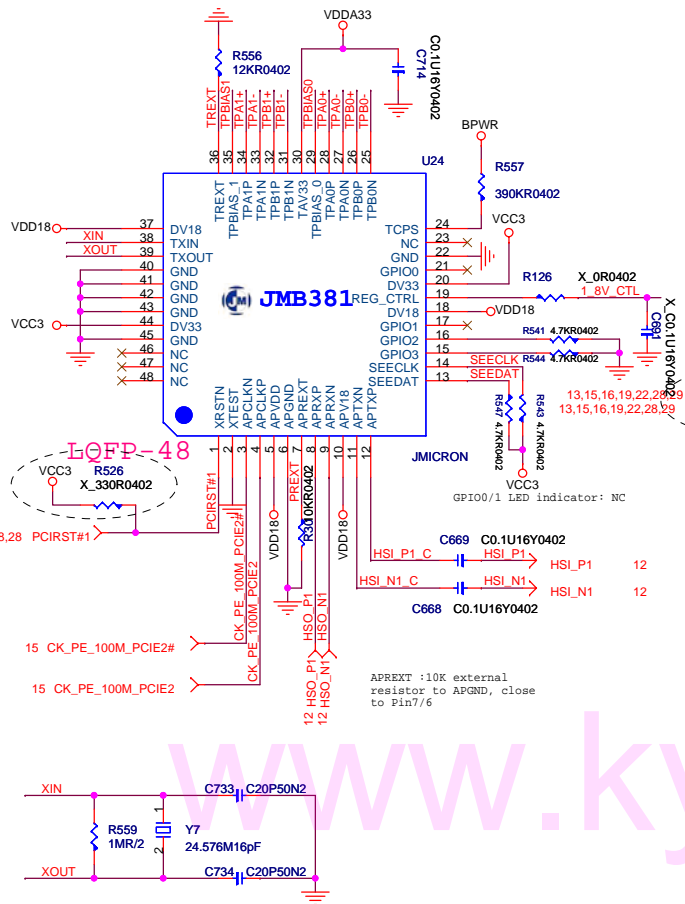
Wide Device in System	Pin B7 of the PCIe #x slot	SDVO Down Subsystem	SDVO_CTRL_DATA (WCS pin 017 also routed to X8 slot pin B31)	EXP_EN (WCS pin J17 also routed to X8 slot pin B48)
SDVO Down	High	Enabled	High	High
SDVO Expansion card	Low	Disabled	High	Low
WCS PCIe	Low	Disabled	High	High
Graphics Card	Low	Disabled	Low	Low



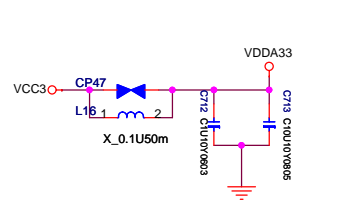
DMI TRANSMITTER REGULATORS



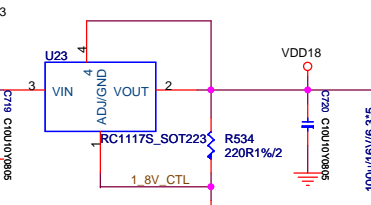
VCC3 max 80mA
VDDV1_18 max 320mA
VCC5 max 55mA



Power Selection Circuit



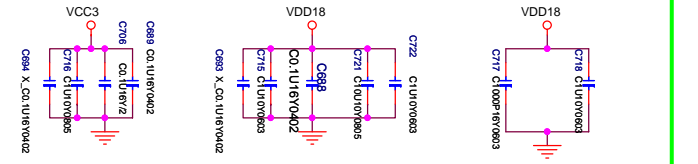
Power Selection Circuit



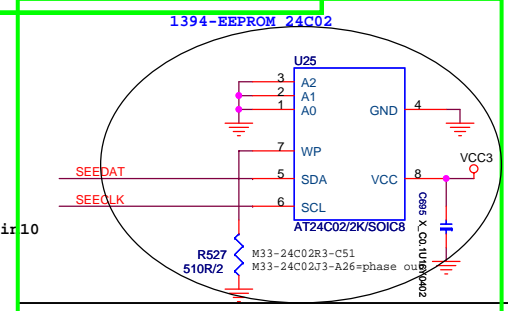
$$V_o = V_{ref} (1 + R_2/R_1)$$

where $V_{ref} = 1.25V$

Decouple capacitors



please close to Pin5, Pin10



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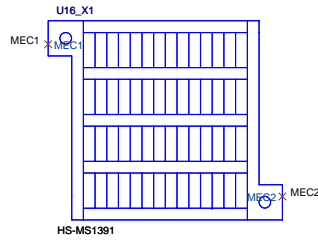
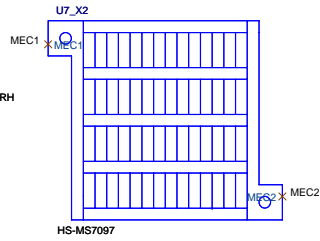
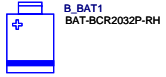
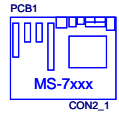
Title		
LPC SUPER I/O & CONNECTORS		
Size	Document Number	Rev
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Auto-BOM Manual Parts


@MACH 04/18/07
CFG7383-GD G31 ver:A+W/O PCB+DVI+PCI_E 8X +ALC888
CFG7383-MP G31 ver:A+W/O PCB + PCI_E 16X +ALC888

G31 HEATSINK

ICH7 HEATSINK



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- 1.P25- change CN7 to C613 C614 C615 C 616
- 2.P25- change R209\R206\R202 location
- 3.P25- change U10 to U10+U11
- 3.P25- remove RN42\RN43
- 4.P28- Remove EC37,EC53
- 5.P16- Change parallal port to PGND
- 6.P29- Remove EC4
- 7.P18- Remove C520,add c597
- 8.P28- Remove EC79
- 9.P18- Remove EC70
- 10.P21- Add EMI cap VCC_DDR,VTT_DDR
- 11.P27- Remove c106,c111
- 12.P5- Remove EC6
- 13.P15- Add Q41,R343
- 14.P18- Remove EGND
- 15.P6- Change R58\81\82\83 to 115R

05 Remove H_CPUSLP#(Pin L2)
 12 SPI power use VCC3;Remove reserved R384,R392,R418
 13 Modify RSMRST# to divider circuit and short to LAN_RST# directly
 15 Add the circuit patch the 1333 as 1066
 28 Modify the V_1P5_CORE,V_FSB_VTT sequence control circuit

MS-73830B mach@07'0523

P16 Add JTPM1;PS2 power rail change to SVCC1
 P18 Add Reserved RTL8111C circuit
 P20 Modify the Dimm3, 4placement
 P22 Add PCIE 1X
 P26 USB power change to DUAL MOS regulator,remove the jumpers
 P28 R357 change to 10KR
 P30 R475 change to 220R1%;Add PCIE/SDVO Dynamic detect circuit;

MS-7383 2.0 david@07'0612

P16 Add com2
 P22 remove PCIE 1X
 P23 Add PCI slot3;and signal PGNT#2
 P27 ADD Watchdog on VRM
 P16 modify FDD P/N: N32-2173071-H06==>N32-2173051-H06,(V0C->V0d)
 P16 &P30 Add C655 0.1uf i and R521 0 ohm for EMI
 P29 PCIE_8X + DVI +4phase/12 mos(CFG_7383_GD)
 PCIE_16X+3phase/9mos(CFG_7383_MP)
 P13 reserve R84 to GPI9 for therm#
 P29 change C33/60/72/142 1000PF to 2200PF
 install C177(1000PF) ==>EMI
 Swap RN45: DCDB#/DSRB# 07/06/23
 P15 ADD C568 for LPC_CLK 06/25/07
 P31 modify PCB1 P/N:P80-0738320-Y34 2007/06/27

P15 ADD pull high to VRM_GD
 add pull-high to FP_RST_R#
 modify pull high Therm_SB# to VCC3 (R375) 07/09/07


P16 install R254 and reserve R262 for BIOS*4E/4F, TPM:2E/2F" 2007/07 /11

P31 Add JMB381 1394 and change USB1 Footprint to 1394+USB*2 footprint 2007/07 /15

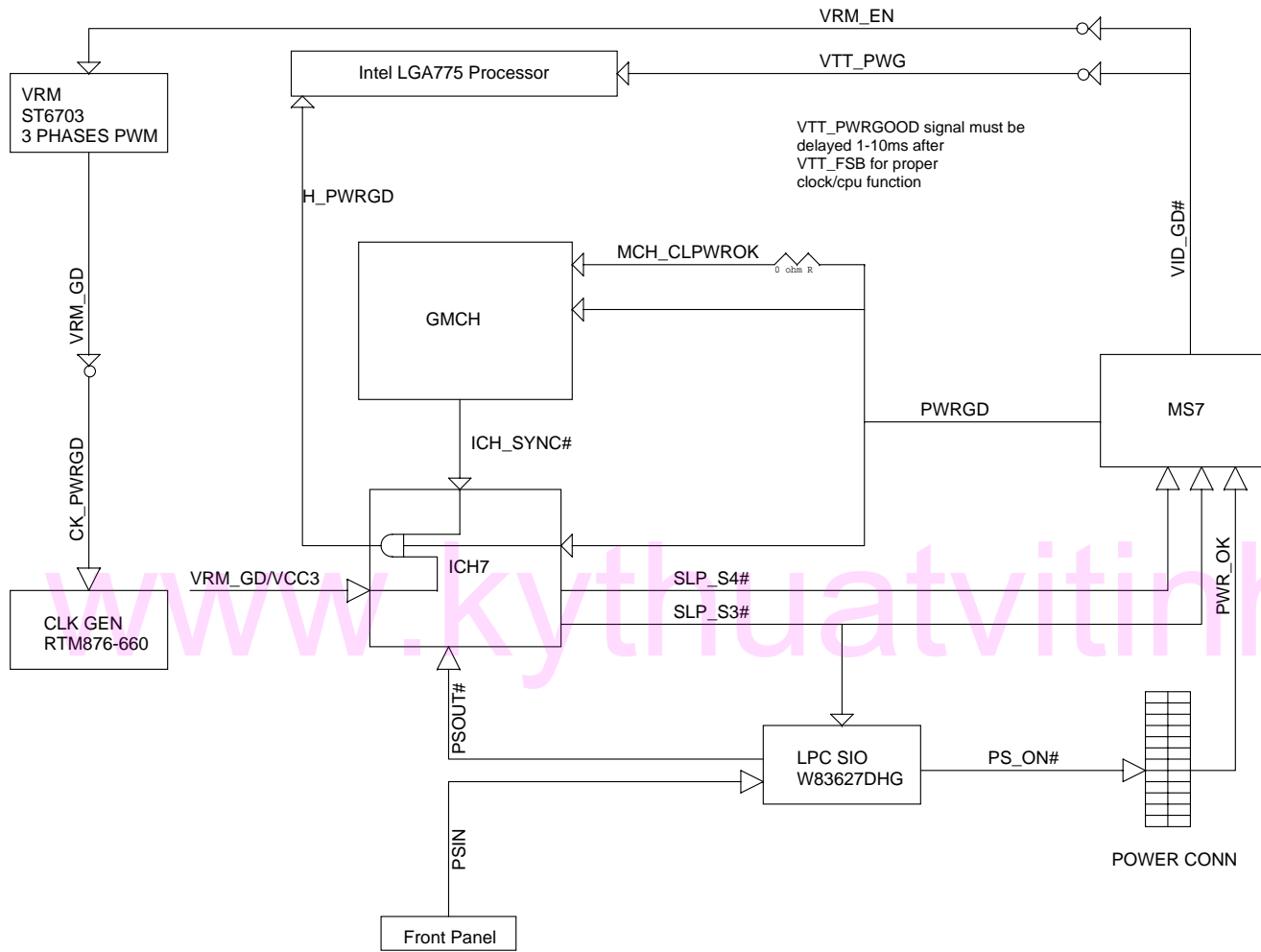
P31 Add C722 c693/c694 2007/07 /17
 07/18: modify P/N and reserve R521 for Therm#
 add 1394 EEprom 07/19

P15 remove C383/c404/c62/ec66 for EMI "011"
 C717 1UF ->1000PF; RN24/R476/477/530/540 change to 33 ohm "013"2007/07 /23

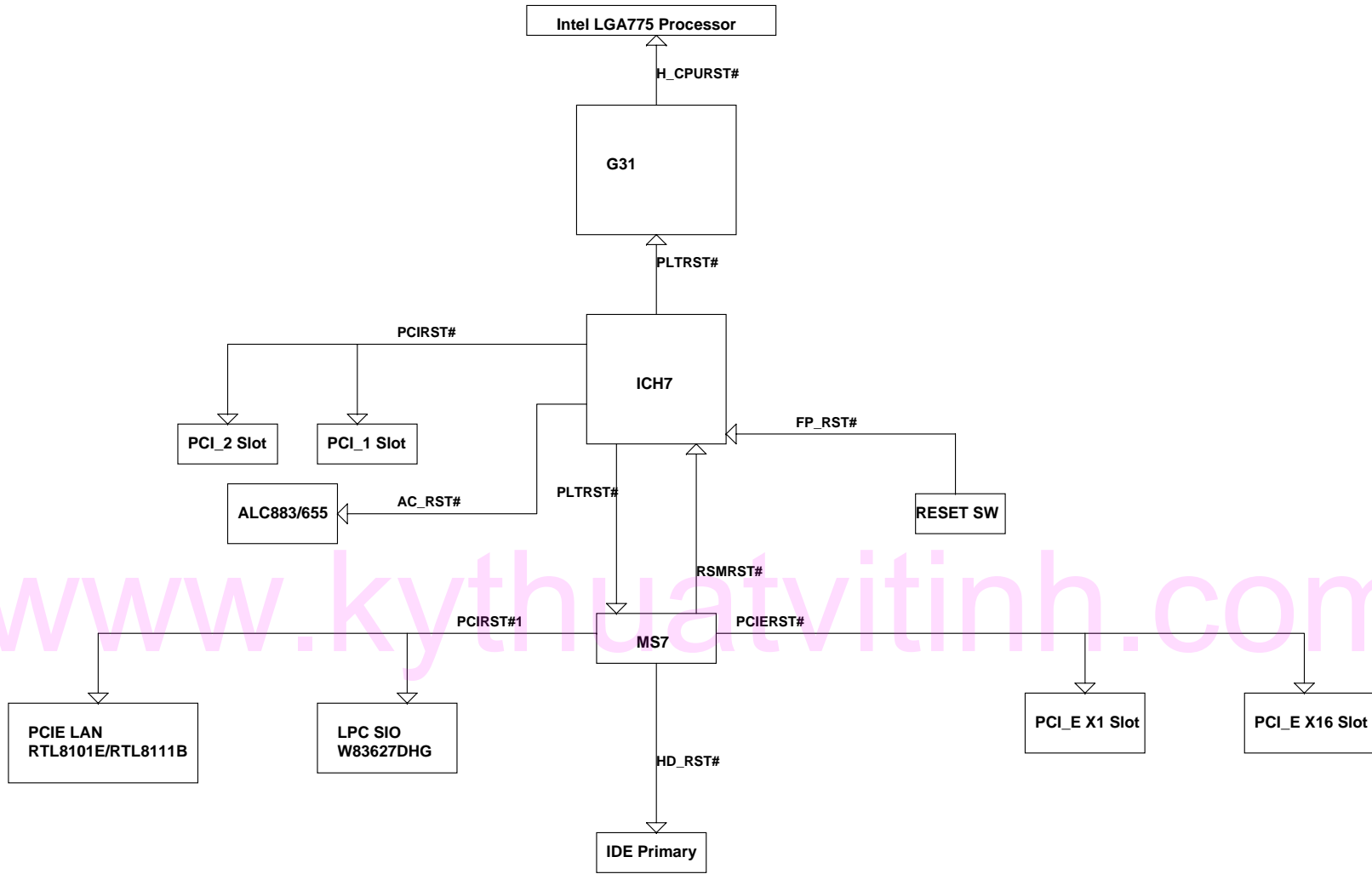


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PWROK MAP



Title			POWEROK MAP		
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GPIO	Alt Func	PIN	I/O	CORE	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	PIRQE#
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	PIRQ#F
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	PIRQ#G
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	PIRQ#H
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	SMB_ALERT#
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	0	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	N/A	PGNT#5
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	1	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	1	NC
GPIO21	SATA_OGP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	PREQ#4
GPIO23	LDRO_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC (NO CHANGE)
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	1	HW PULL LOW
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	0	NC
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	0	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	0	NC
GPIO29	DC5#	C3	I/O	Resume	N	N	3.3V	GPI	OC#2
GPIO30	DC6#	A2	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO31	DC7#	B3	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	1	BIOS_WP#
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	1	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	0	NC
GPIO35	SATAACKREQ#	AD21	I/O	CORE	N	N	3.3V	1	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO40	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	PGNT#4
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used.
GPIO[39:36,23:21,13,7-0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

GPIO	Alt Func	PIN	USAGE	Input/Output	NOTES
GP24	MDAT	66	MSDAT#	I/OD16ts	PS2 Mouse Data.
GP25	MCLK	65	MSCLK#	I/OD16ts	PS2 Mouse Clock.
GP26	KDAT	63	KBDAT#	I/OD16ts	Keyboard Data.
GP27	KCLK	62	KBCLK#	I/OD16ts	Keyboard Clock.
GP32	SCL/RSTOUT2#	90	SMBCLK_ISO	INts	Serial Bus clock.
GP33	SDA/RSTOUT3#	89	SMBDATA_ISO	I/OD12ts	Serial bus bi-directional Data.
GP35	Unmultiplexed	87	UNUSED		
GP36	Unmultiplexed	69	UNUSED		
GP37	Unmultiplexed	64	UNUSED		
GP54	PWR0K	71	UNUSED		
GP40	RIB#	85	RIB#	INt	Ring Indicator.
GP41	DCDB#	84	DCDB#	INt	Data Carrier Detect.
GP42	IRTX/SOUTB	83	IRTX(SOUTB)	OUT8	IR Transmitter output./UART B Serial Output.
GP43	IRRX/SINB	82	IRRX(SINB)	INt	Serial Input/IR Receiver input.

GPIO	Alt Func	PIN	USAGE	Input/Output	NOTES
GP44	DTRB#	81	DTRB#	OUT8	UART B Data Terminal Ready.
GP45	RTSB#	80	RTSB#	OUT8	UART B Request To Send.
GP46	DSRB#	79	DSRB#	INt	Data Set Ready.
GP47	CTSB#	78	CTSB#	INt	Clear To Send.
GP50	EN_VRM10/WDTO#	77	STRAPPED DOWN	INcd	defined as VID transition voltage level
GP51	RSMRST#	75	RSMRST#	OD12	Resume reset signal output.
GP52	SUSB#	73	SLP_S3#	INt	System S3 states input.
GP53	PSON#	72	PSON#	OD12	This pin generates the PWRCTL# signal while the power is on.
GP56	PSIN	68	PSIN	INtd	Panel Switch Input.
GP57	PSOUT#	67	PSOUT#	OD12	Panel Switch Output.
GP60	RIA#	57	RIA#	INt	Ring Indicator.
GP61	DCDA#	56	DCDA#	INt	Data Carrier Detect.
GP62	SOUTA/PENKBC	54	SOUTA	OUT8	UART A Serial Output.
GP63	SINA	53	SINA	INt	Serial Input.
GP64	DTRA#/PENROM	52	DTRA#	OUT8	UART A Data Terminal Ready.
GP65	RTSA#/HEFRAS	51	RTSA#	OUT8	UART A Request To Send.
GP66	DSRA#	50	DSRA#	INt	Data Set Ready.
GP67	CTSA#	49	CTSA#	INt	Clear To Send.

PCI Config.

DEVICEMCP1	INT	PIN	REQ#	GNT#	IDSEL	CLOCK
LAN	PIRQ#E	PREQ#4	PGNT#4		AD20	PCI_LAN
PCI1	PIRQ#A	PREQ#0	PGNT#0		AD16	PCI_CLK0
	PIRQ#B					
	PIRQ#C					
	PIRQ#D					
PCI2	PIRQ#B	PREQ#1	PGNT#1		AD17	PCI_CLK1
	PIRQ#C					
	PIRQ#D					
	PIRQ#A					

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	P_DDR0_A/N_DDR0_A
		P_DDR1_A/N_DDR1_A
		P_DDR2_A/N_DDR2_A
DIMM 2	A2H	P_DDR0_B/N_DDR0_B
		P_DDR1_B/N_DDR1_B
		P_DDR2_B/N_DDR2_B
DIMM 1	A4H	P_DDR0_B/N_DDR0_B
		P_DDR1_B/N_DDR1_B
		P_DDR2_B/N_DDR2_B
DIMM 2	A6H	P_DDR0_B/N_DDR0_B
		P_DDR1_B/N_DDR1_B
		P_DDR2_B/N_DDR2_B



JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

JCI1	Chassis Intrusion
Open	Normal
(1-2)	Chassis Open