

Compal Confidential

JALA0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

(With Ati & nVidia MXM/B)

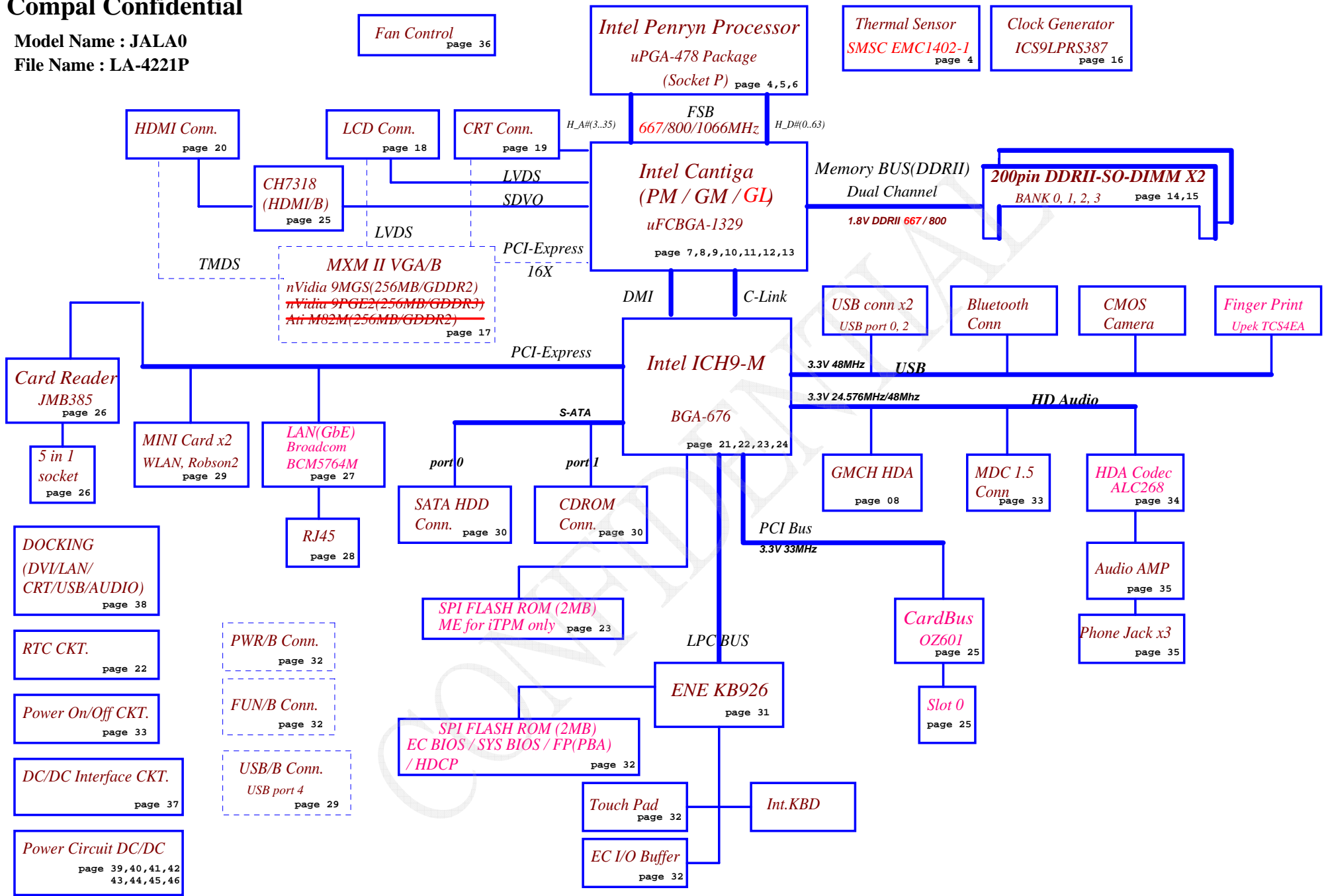
2008-04-18

REV:1.0

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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	SCHMATIC MB A4221
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Model Name : JALAO
File Name : LA-4221P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Cardbus OZ601	AD16	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GPU(MXM/B)	1001 111X b

EC SM Bus2 address

Device	Address
ADT7421	1001 100X b
(LAN BCM5764M)	Reserved

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
LAN BCM5764M	Reserved
(MINI CARD_WL_Robson)	Reserved

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

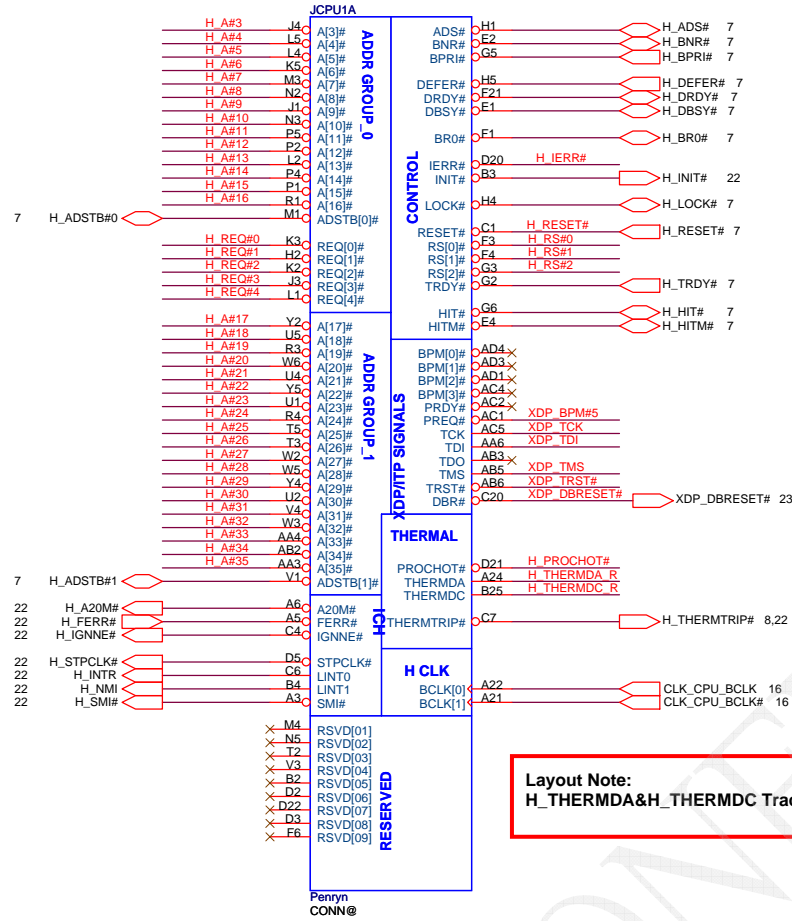
BTO Option Table

BTO Item	BOM Structure
Discrete_H	PM@
UMA	GM@
UMA_H	UMAGM@
UMA_L	UMAGL@
Kinabalu_H	MAIN@
Kinabalu_L	VALUE@
RTC Batt	45@
ICH9M BASE	ICH9MB@
ICH9M ENHANCE	ICH9ME@
SB ROM(2MB)	SPI2MB@
SB ROM(4MB)	SPI4MB@

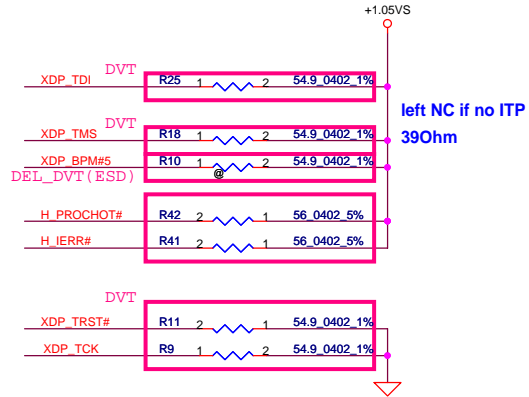
Kinabalu_L : UMA(GL) & w/o Dock & w/o Mini card 2 & w/o iTPM

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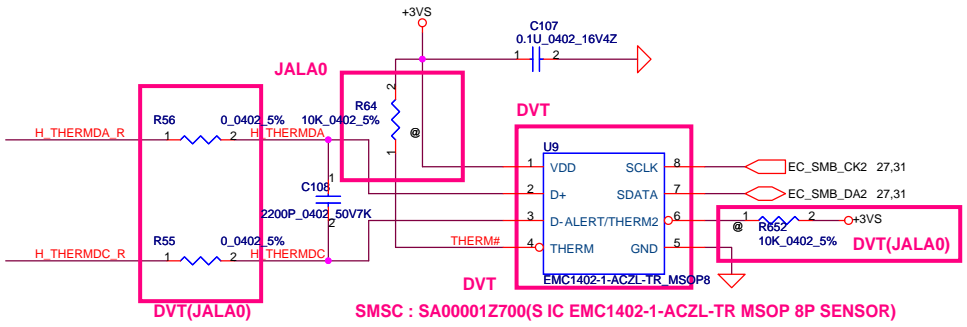
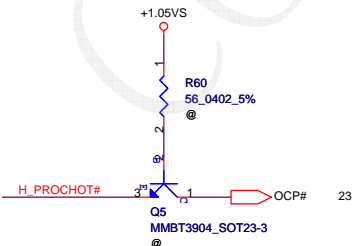
- 7 H_A#[3..35] H_A#[3..35]
- 7 H_REQ#[0..4] H_REQ#[0..4]
- 7 H_RS#[0..2] H_RS#[0..2]

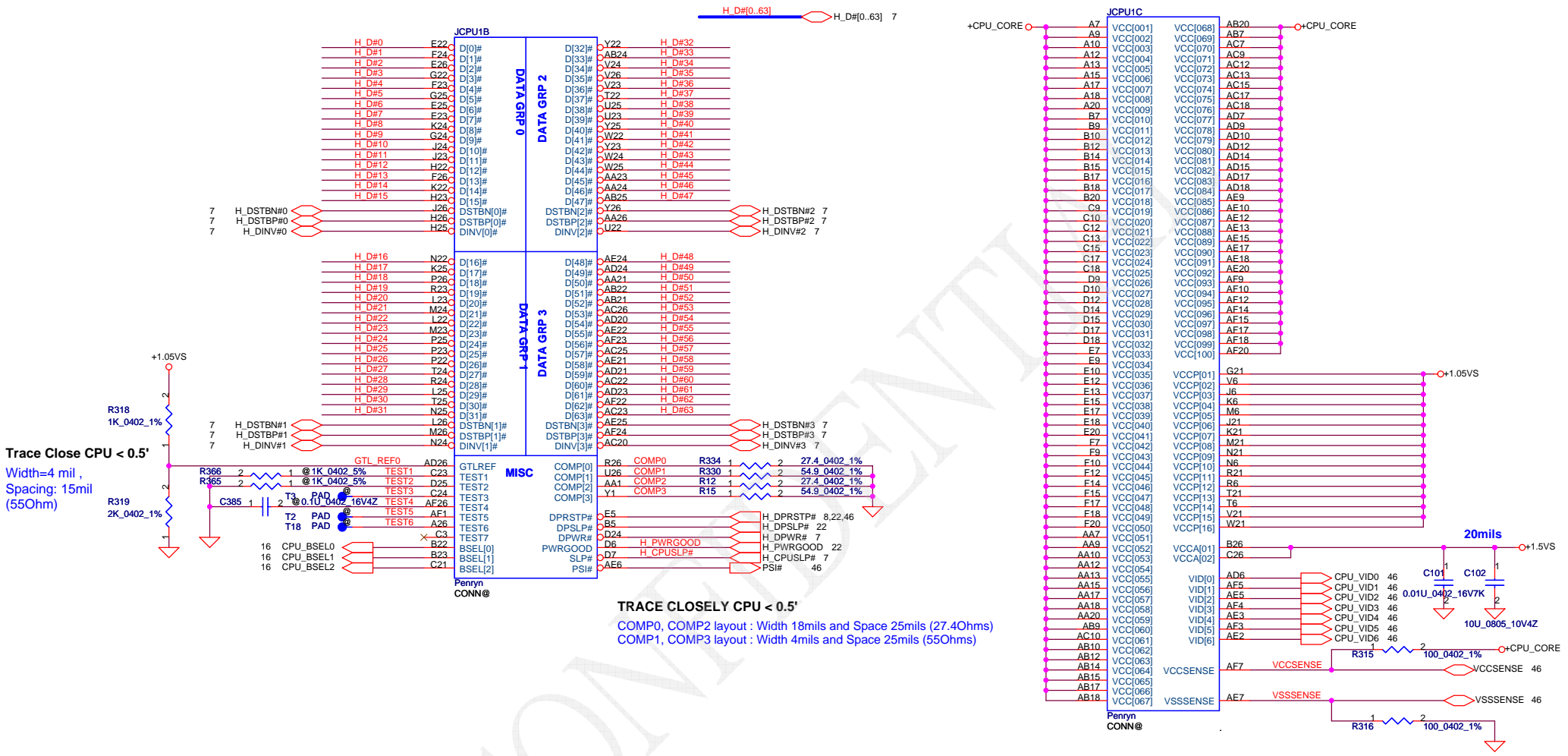


Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166





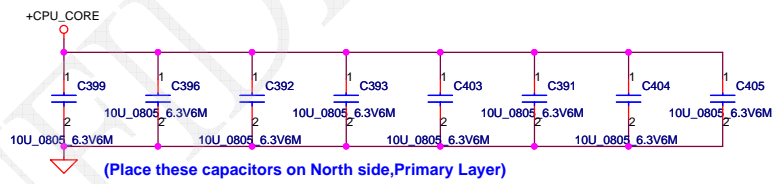
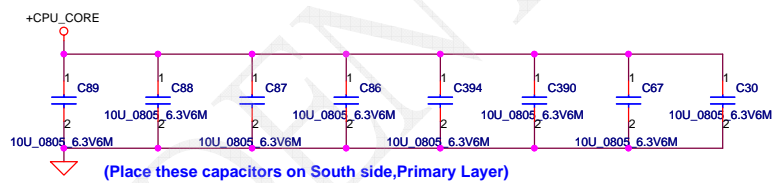
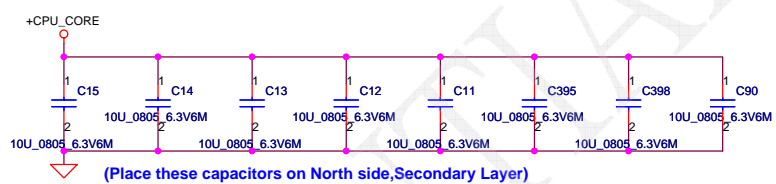
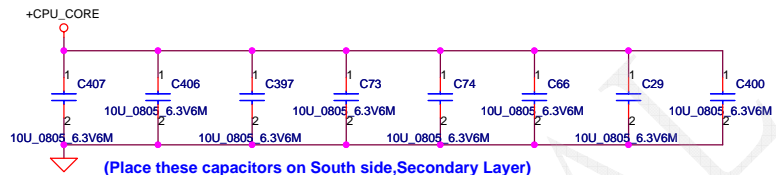
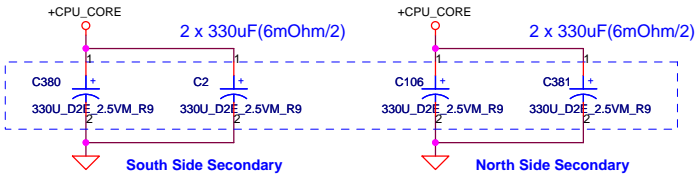
Trace Close CPU < 0.5'
Width=4 mil,
Spacing: 15mil
(55Ohm)

TRACE CLOSELY CPU < 0.5'
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

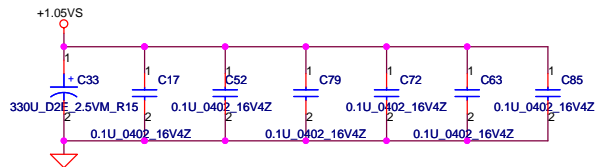
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JCPU1D	
A4	VSS[001]
A8	VSS[002]
A11	VSS[003]
A14	VSS[004]
A16	VSS[005]
A19	VSS[006]
A23	VSS[007]
AF2	VSS[008]
B6	VSS[009]
B8	VSS[010]
B11	VSS[011]
B13	VSS[012]
B16	VSS[013]
B19	VSS[014]
B21	VSS[015]
B24	VSS[016]
C5	VSS[017]
C8	VSS[018]
C11	VSS[019]
C14	VSS[020]
C16	VSS[021]
C19	VSS[022]
C2	VSS[023]
C22	VSS[024]
C25	VSS[025]
D1	VSS[026]
D4	VSS[027]
D8	VSS[028]
D11	VSS[029]
D13	VSS[030]
D16	VSS[031]
D19	VSS[032]
D23	VSS[033]
E3	VSS[034]
E6	VSS[035]
E8	VSS[036]
E11	VSS[037]
E14	VSS[038]
E16	VSS[039]
E19	VSS[040]
E21	VSS[041]
E24	VSS[042]
F5	VSS[043]
F8	VSS[044]
F11	VSS[045]
F13	VSS[046]
F16	VSS[047]
F19	VSS[048]
F2	VSS[049]
F22	VSS[050]
F25	VSS[051]
G4	VSS[052]
G1	VSS[053]
G23	VSS[054]
G26	VSS[055]
H3	VSS[056]
H6	VSS[057]
H21	VSS[058]
H24	VSS[059]
J2	VSS[060]
J5	VSS[061]
J22	VSS[062]
J25	VSS[063]
K1	VSS[064]
K4	VSS[065]
K23	VSS[066]
K26	VSS[067]
L3	VSS[068]
L6	VSS[069]
L21	VSS[070]
L24	VSS[071]
M2	VSS[072]
M5	VSS[073]
M22	VSS[074]
M25	VSS[075]
N1	VSS[076]
N4	VSS[077]
N23	VSS[078]
N26	VSS[079]
P3	VSS[080]
	VSS[081]
	VSS[162]
	VSS[163]

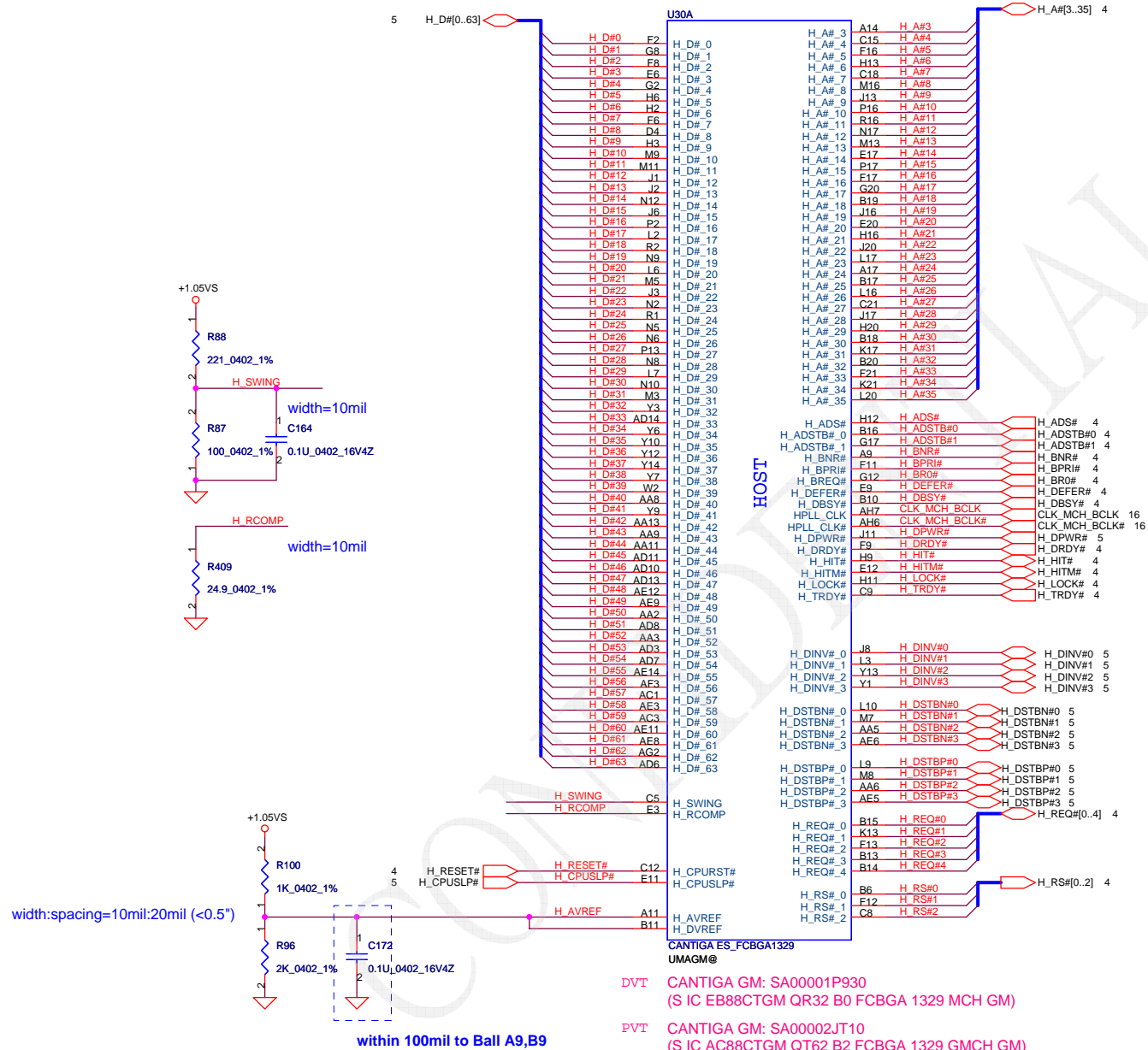
Penryn
CONN@



+CPU-CORE Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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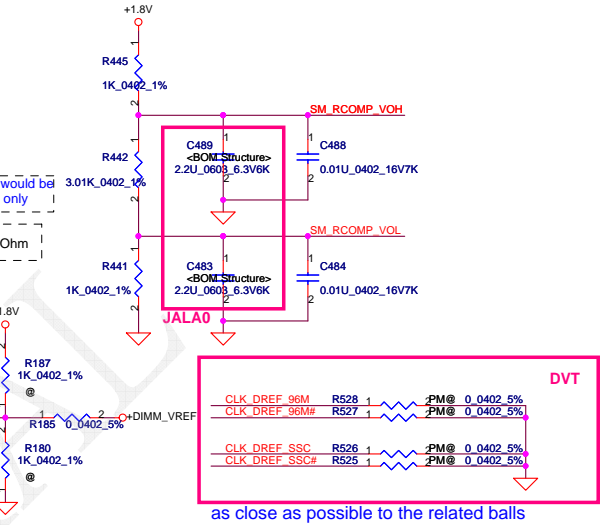
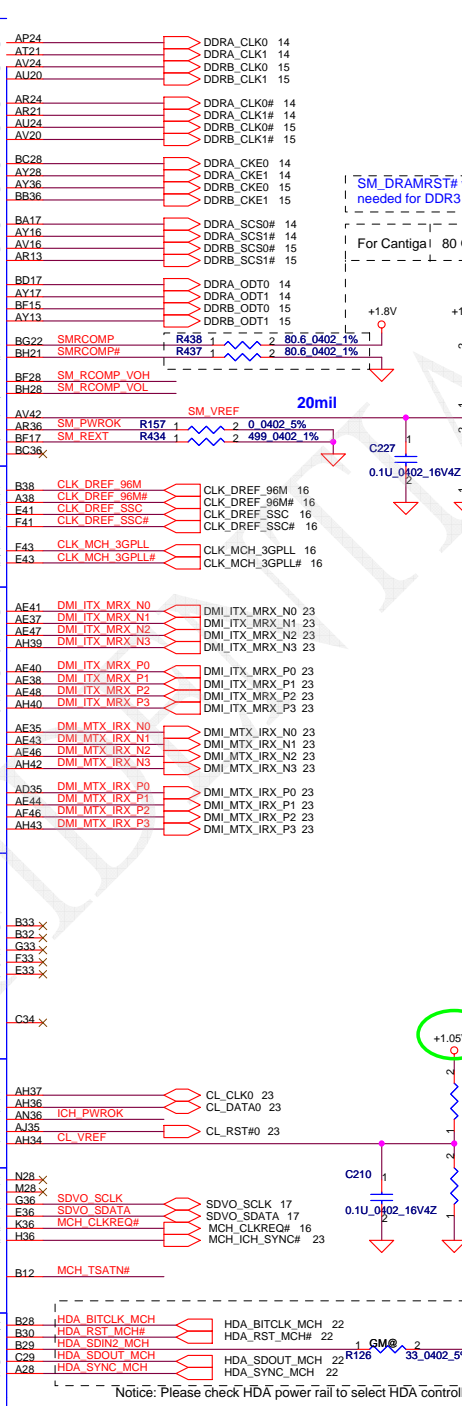
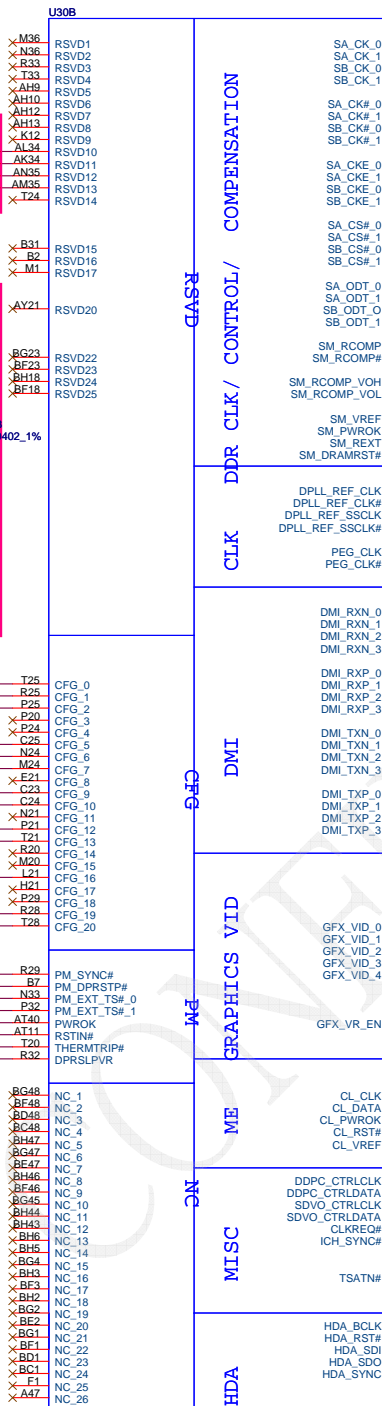
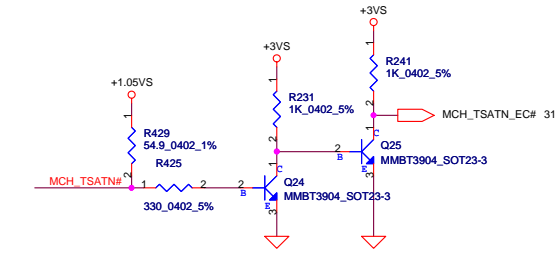
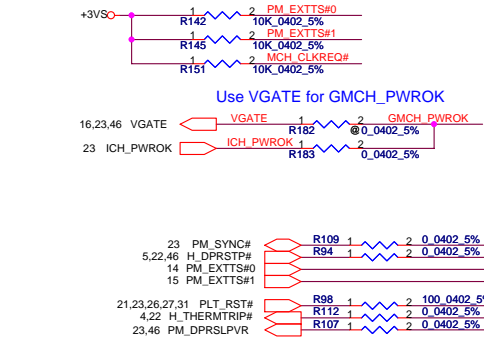
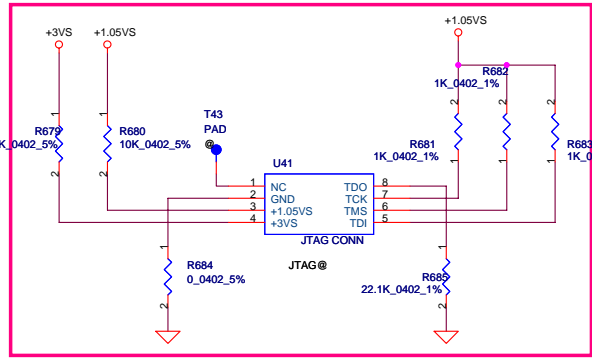


- DVT CANTIGA GM: SA00001P930
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)
- PVT CANTIGA GM: SA00002JT10
(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)
- PVT2 CANTIGA GM: SA00002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)
- Pre-MP CANTIGA GM: SA00002JTB0
(S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABOI)

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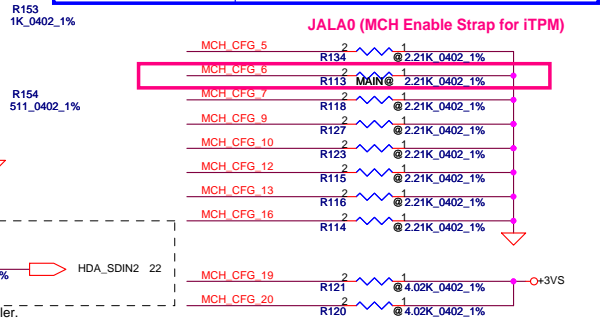
PVT2_JALA0 (Add Management Engine JTAG pins)

All RSVD balls on GMCH should be left No Connect.



Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present



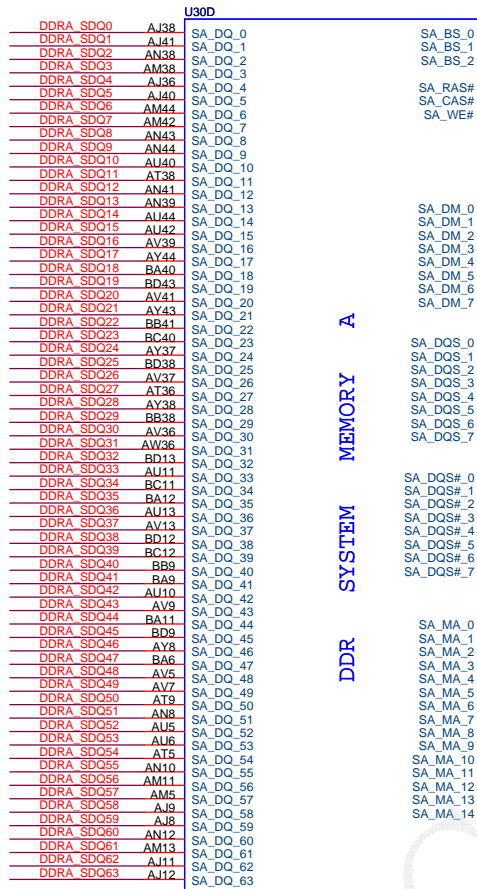
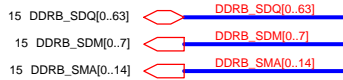
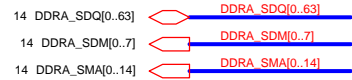
Notice: Please check HDA power rail to select HDA controller.

Pre-MP CANTIGA GM: SA00002JTBO (S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO) DVT CANTIGA GM: SA00001P930 (S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)
 PVT2 CANTIGA GM: SA00002JT50 (S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM) PVT CANTIGA GM: SA00002JT10 (S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

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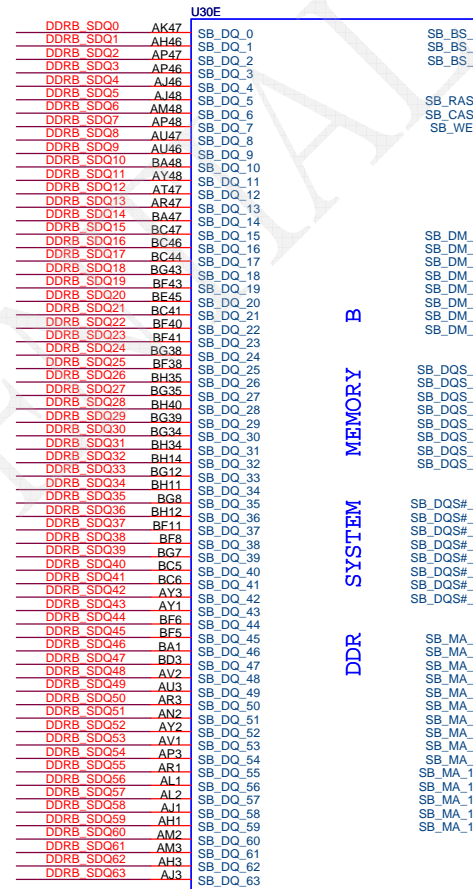
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DDR SYSTEM MEMORY A

CANTIGA ES_FCBGA1329
UMAGM@

- DVT CANTIGA GM: SA00001P930 (S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)
- PVT CANTIGA GM: SA00002JT10 (S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)
- PVT2 CANTIGA GM: SA00002JT50 (S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

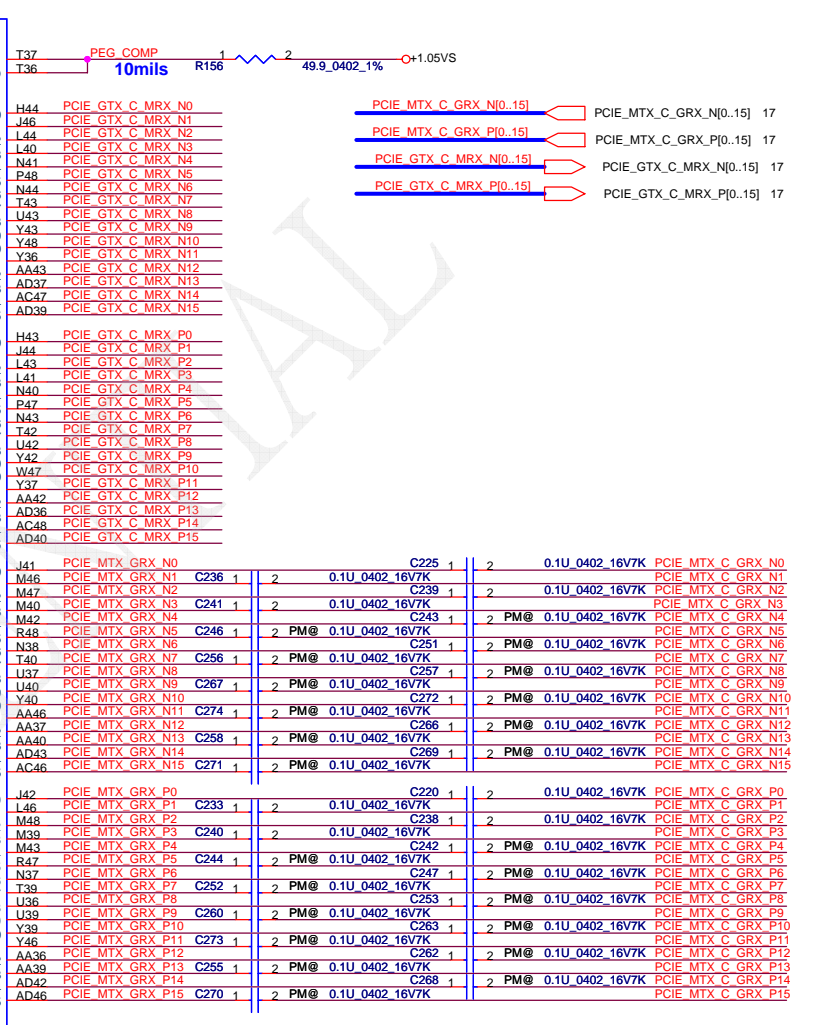
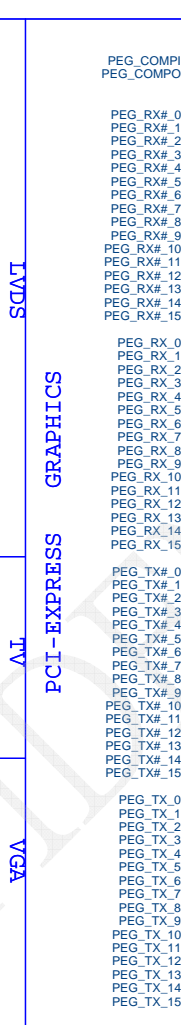
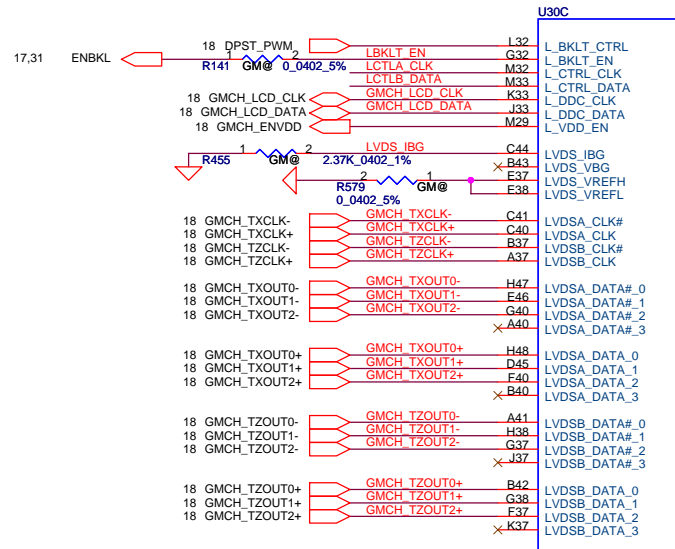


DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329
UMAGM@

- Pre-MP CANTIGA GM: SA00002JTBO (S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO!)

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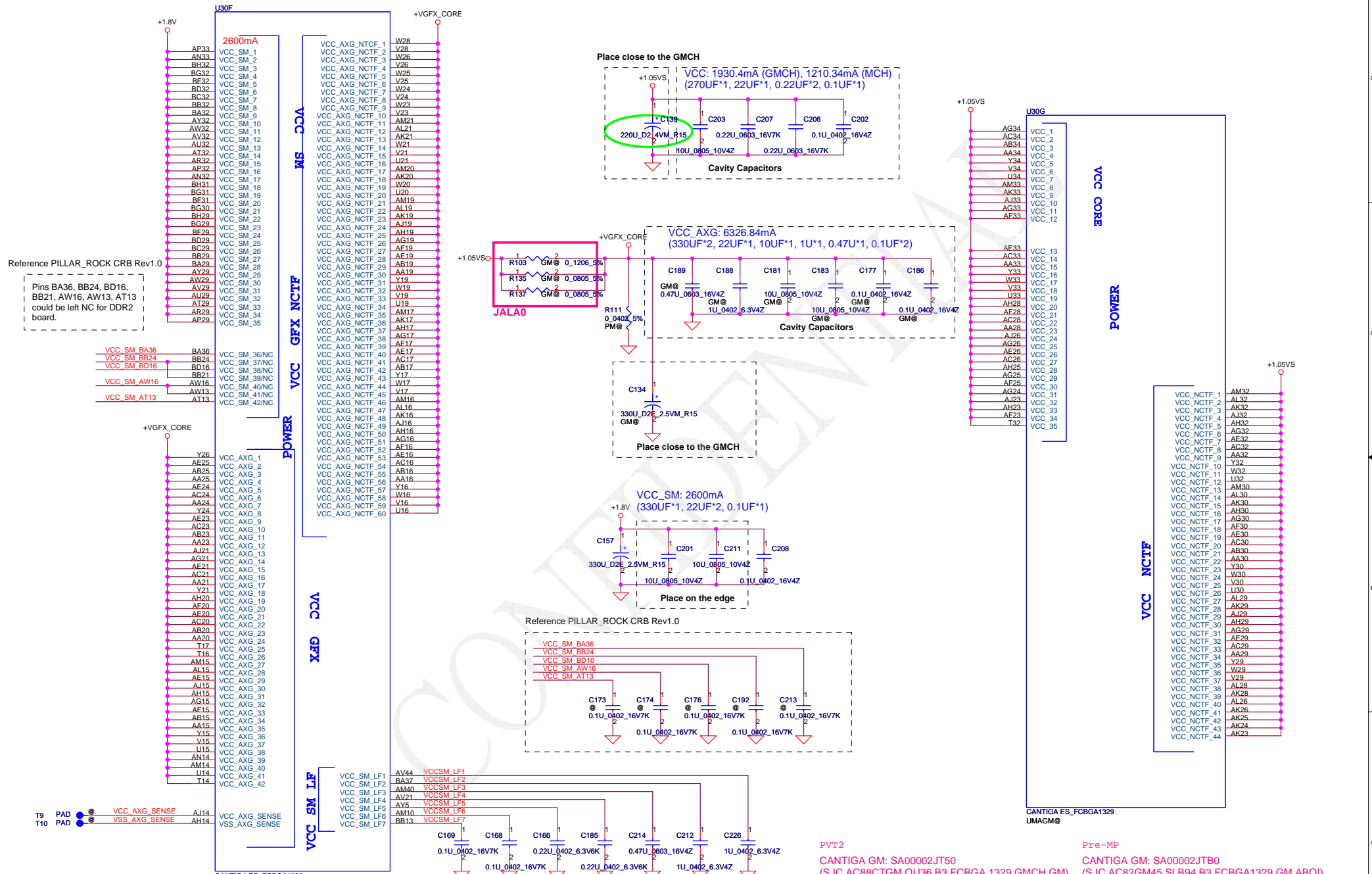


Change to 00hm when use PM chip

Change to 00hm when use PM chip

SAO0001P930	SAO0002JT50
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)	(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)
SAO0002JT50	SAO0002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)	(S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO)

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Reference PILLAR_ROCK CRB Rev1.0
Pins BA36, BB24, BD16, BB21, AW16, AW13, AT13 could be left NC for DDR2 board.

Reference PILLAR_ROCK CRB Rev1.0
VCC_SM_BA36
VCC_SM_BB24
VCC_SM_BD16
VCC_SM_BB21
VCC_SM_AW16
VCC_SM_AW13
VCC_SM_AT13

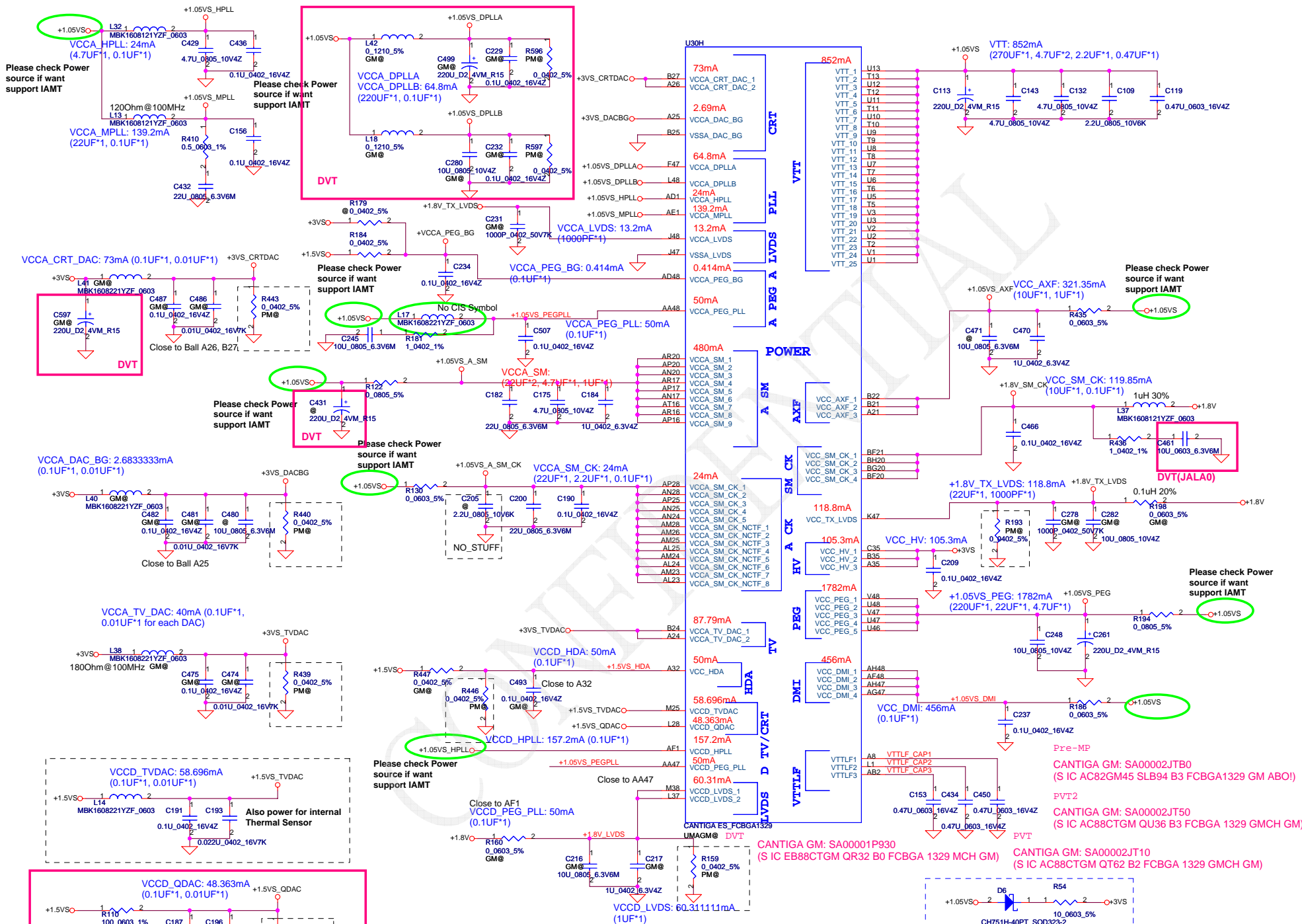
PVT2
CANTIGA GM: SA00002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

Pre-MP
CANTIGA GM: SA00002JT80
(S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABOI)

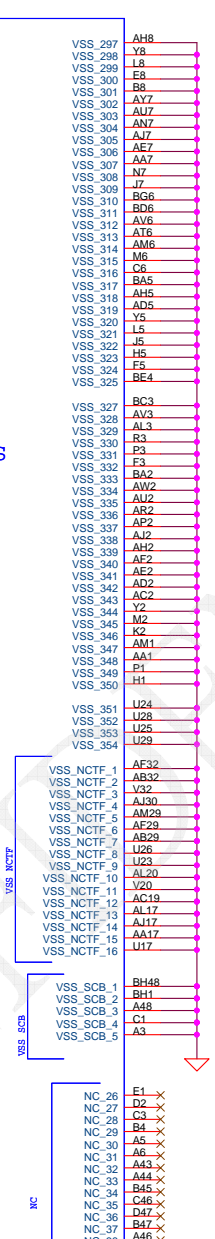
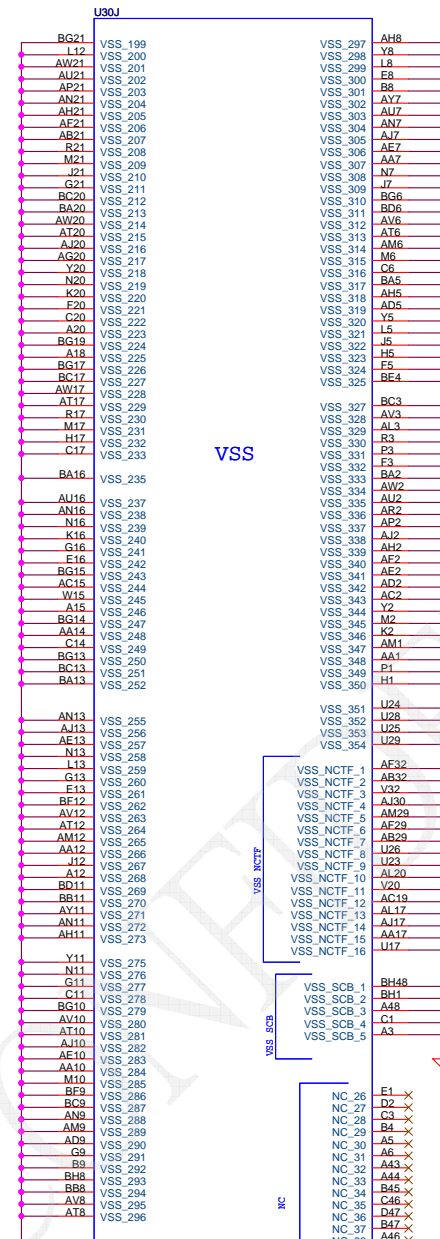
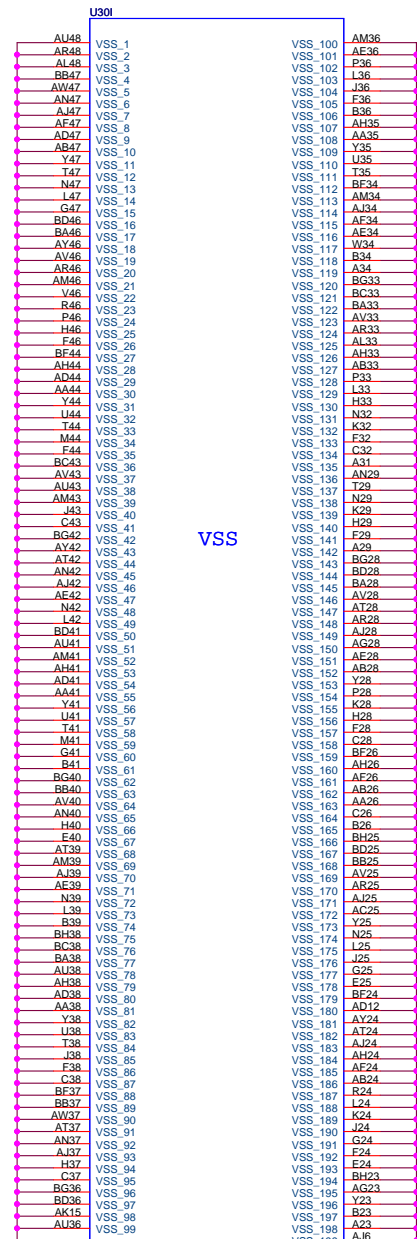
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DVT
CANTIGA GM: SA00001P930
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)
PVT
CANTIGA GM: SA00002JT10
(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)



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PVT2
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 (S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

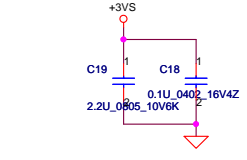
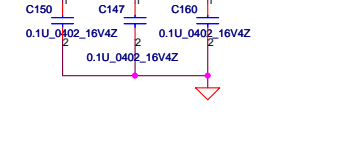
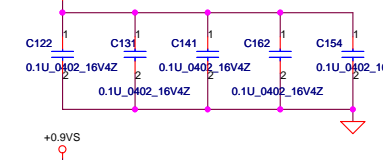
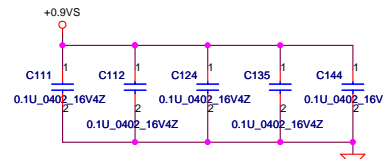
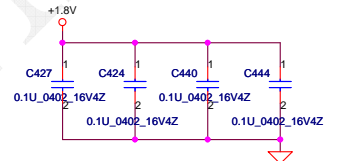
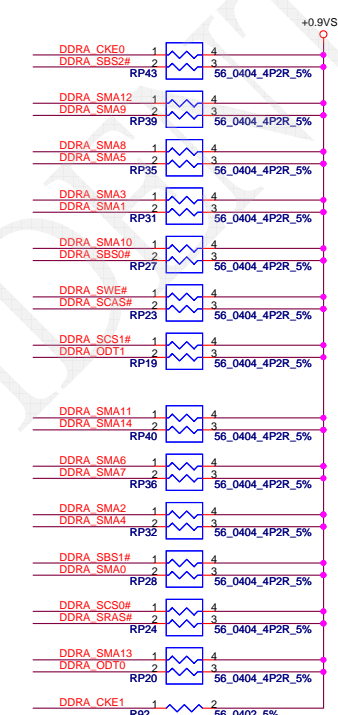
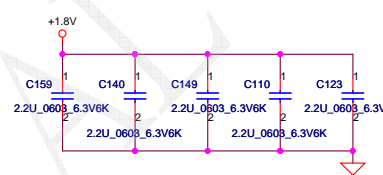
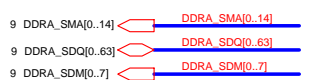
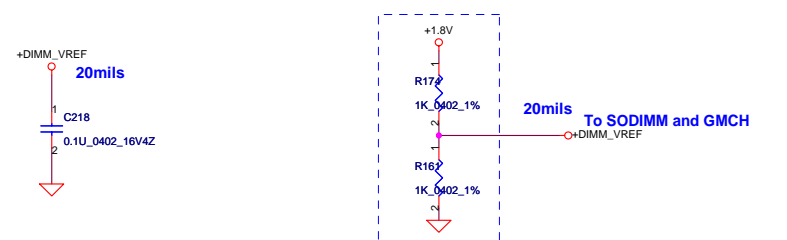
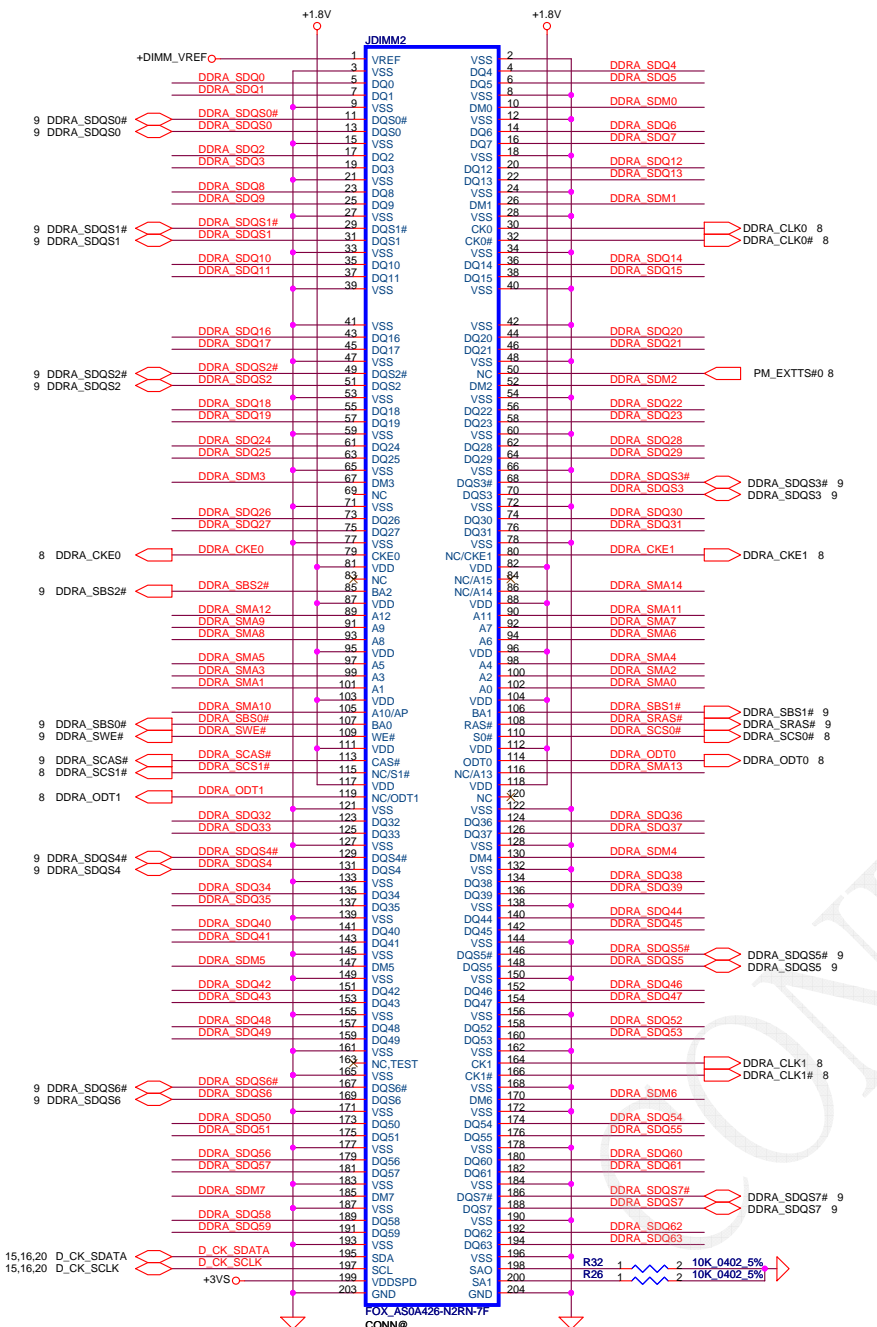
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 (S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABOI)

DVT
 CANTIGA GM: SA00001P930
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PVT
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 (S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

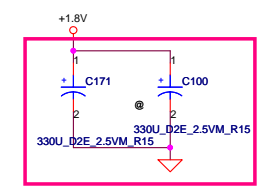
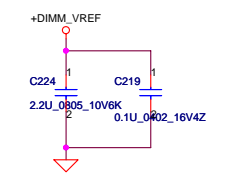
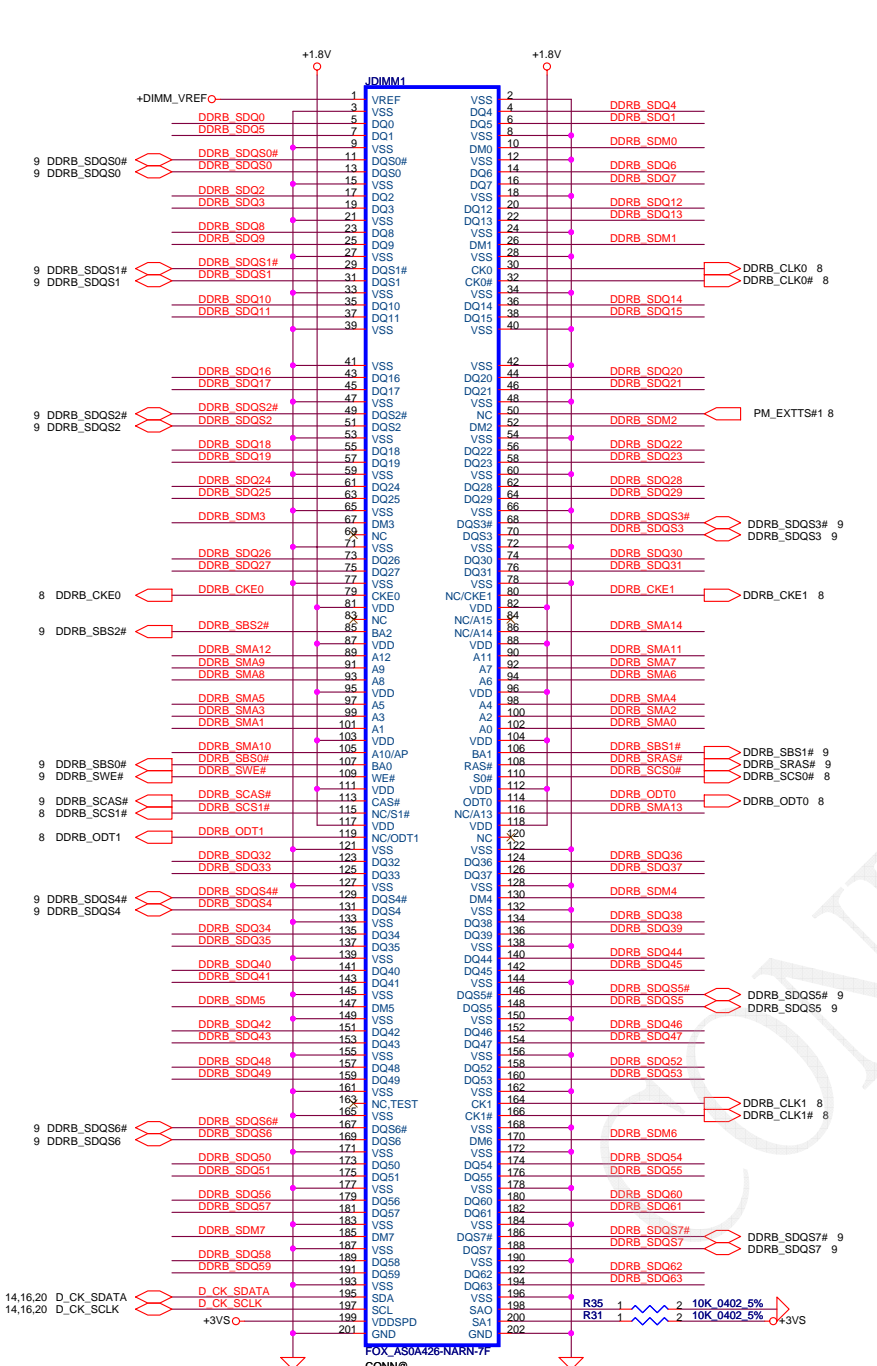
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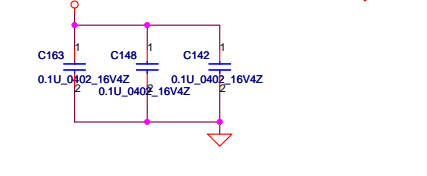
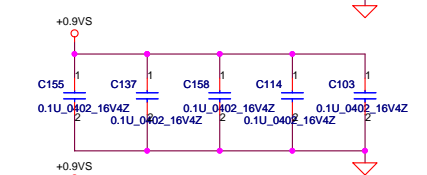
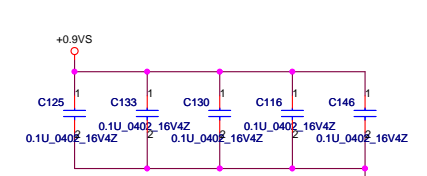
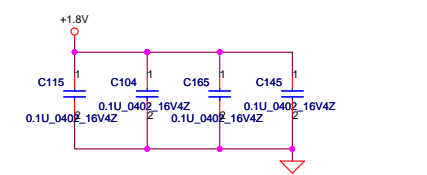
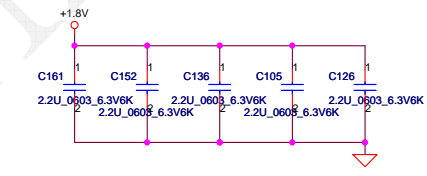
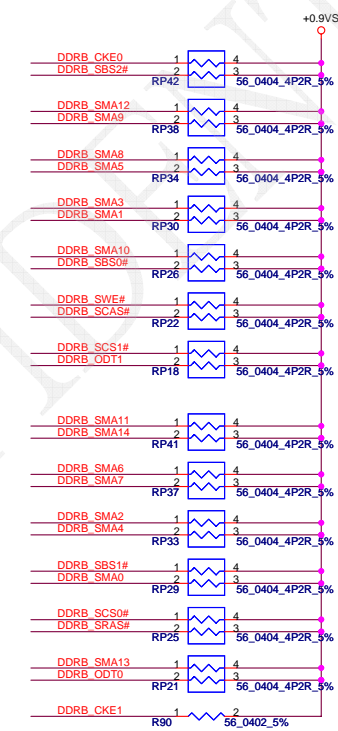


DIMM0 REV H:5.2mm (BOT)

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- 9 DDRB_SMA[0..14] <--> DDRB_SMA[0..14]
- 9 DDRB_SDQ[0..63] <--> DDRB_SDQ[0..63]
- 9 DDRB_SDM[0..7] <--> DDRB_SDM[0..7]



DIMM1 REV H:9.2mm (BOT)

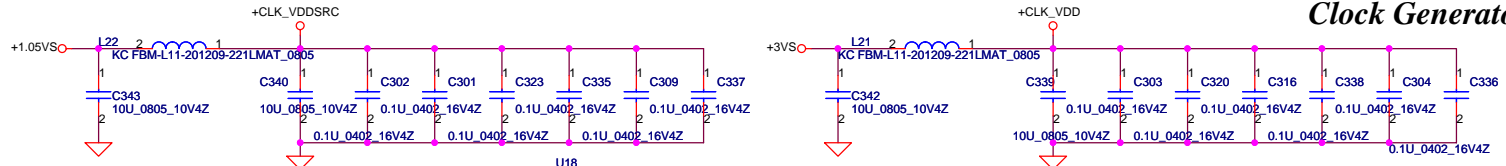
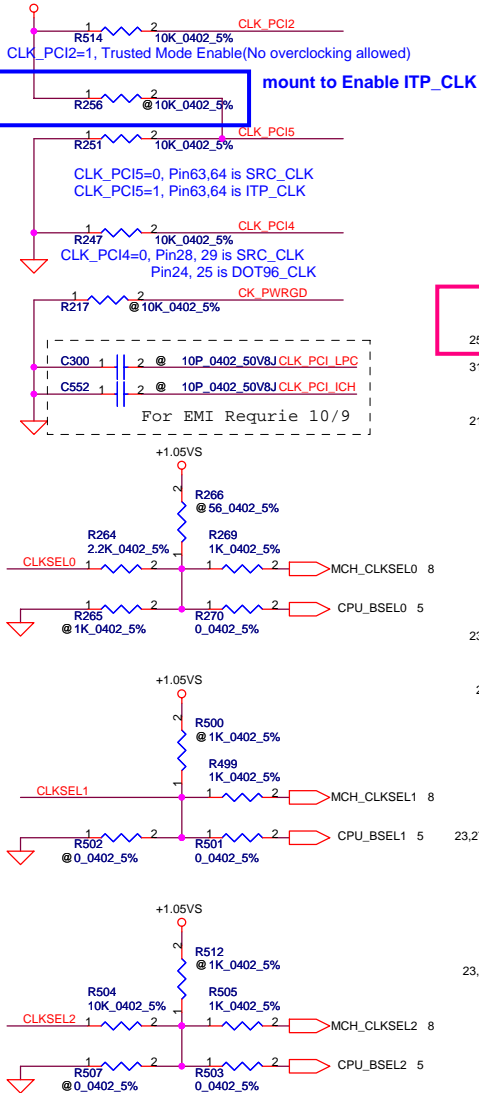
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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

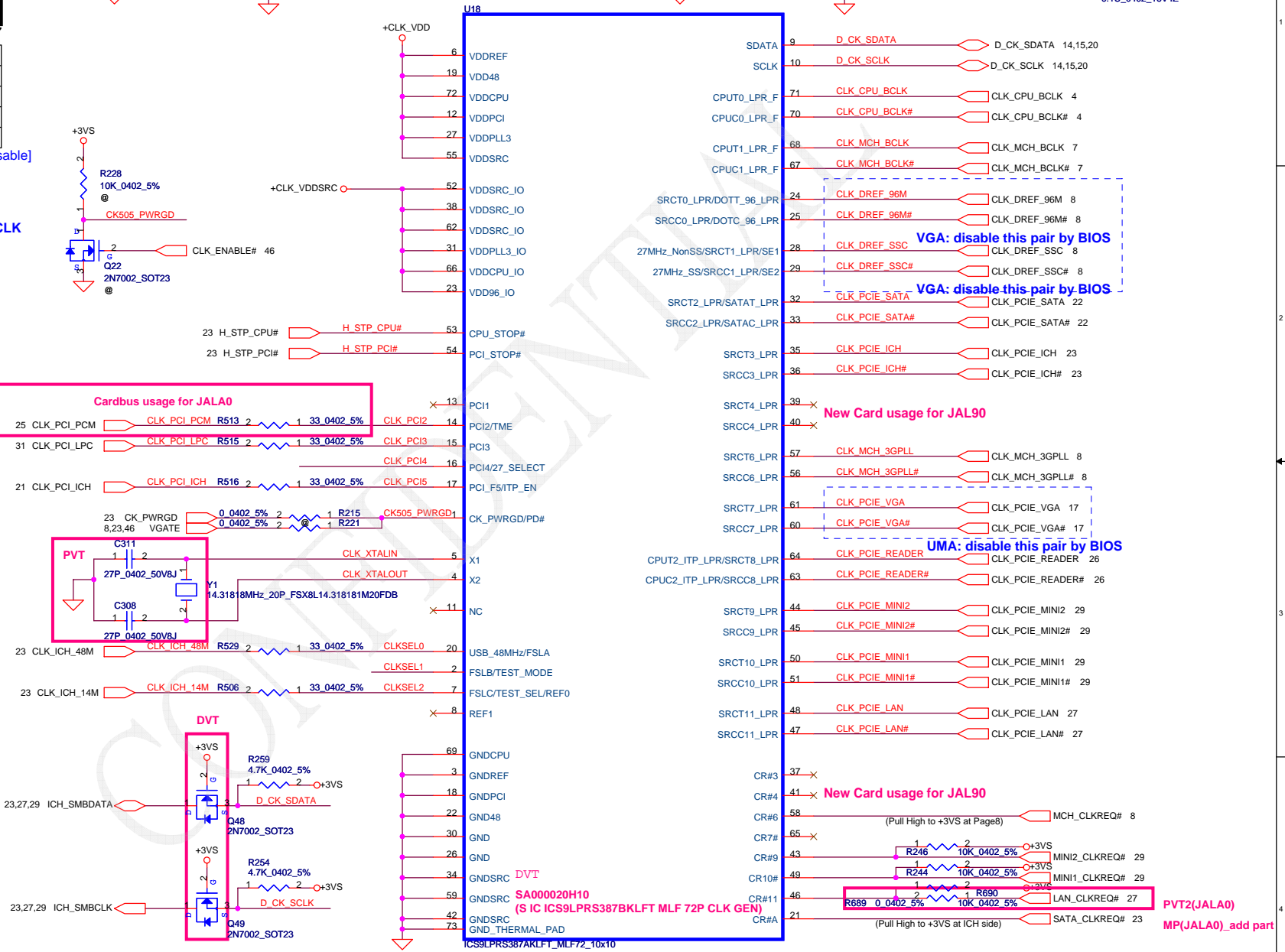
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

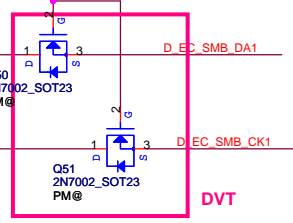
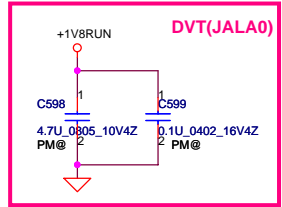
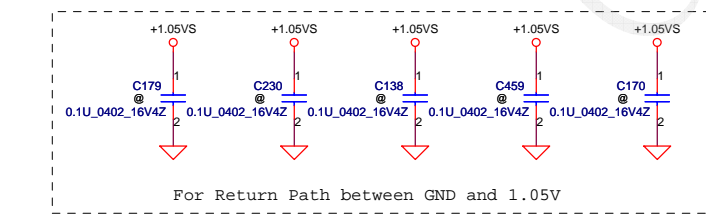
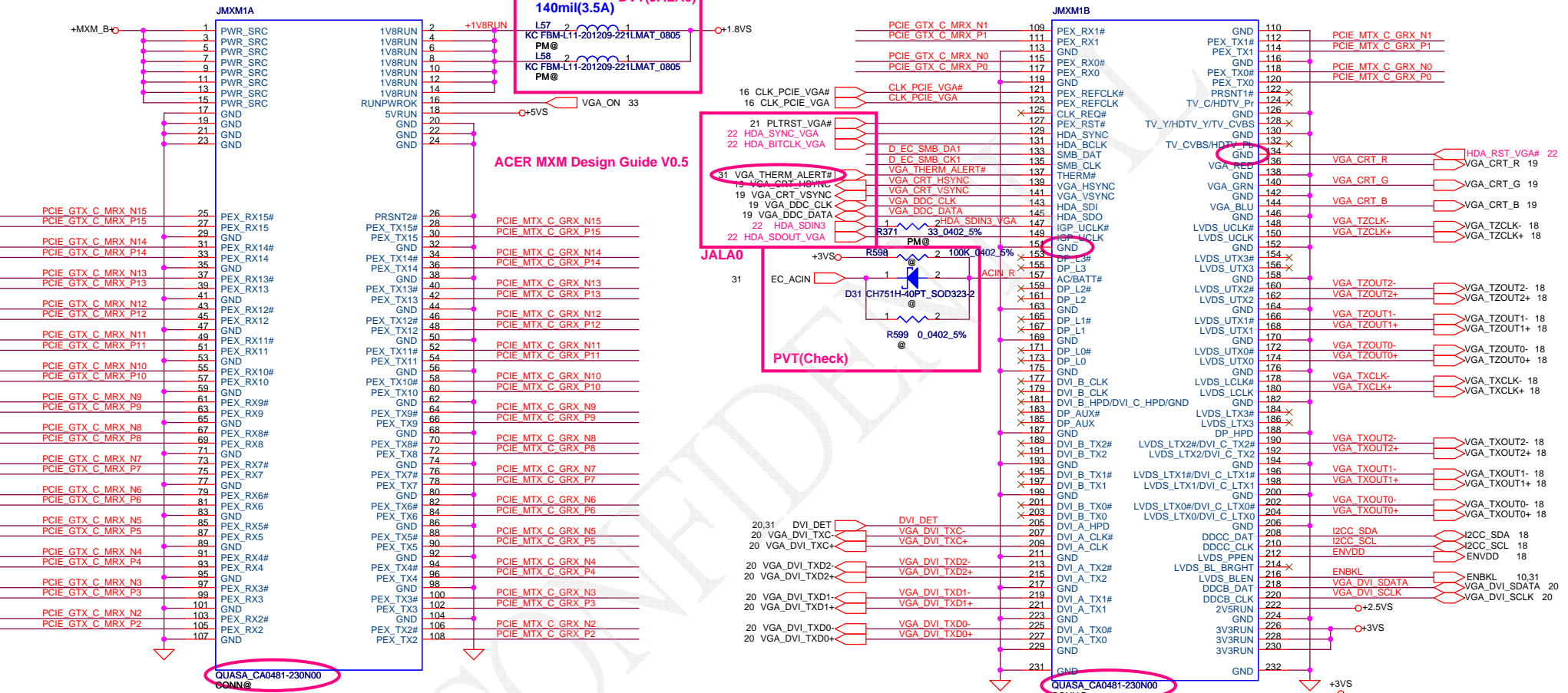


Clock Generator

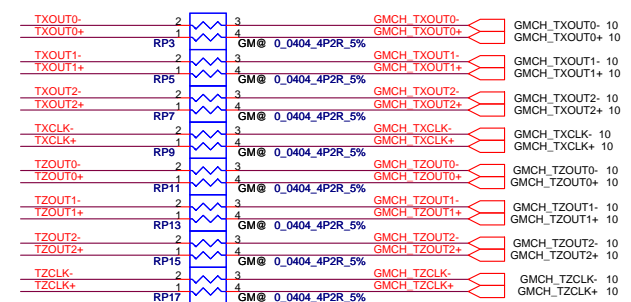
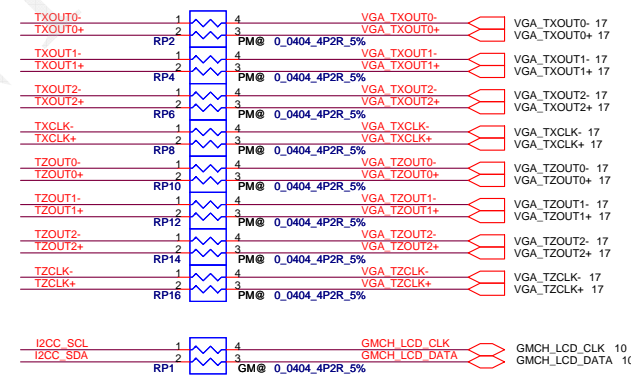
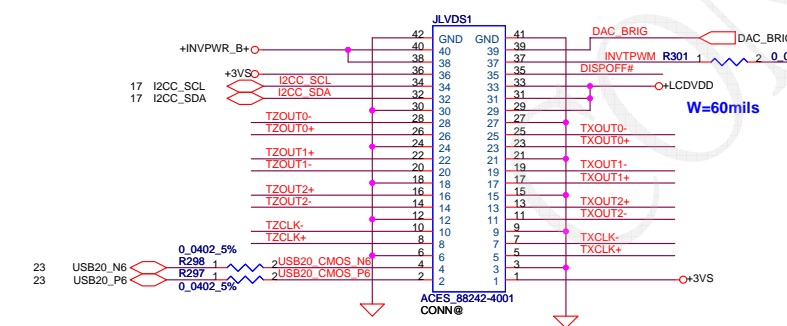
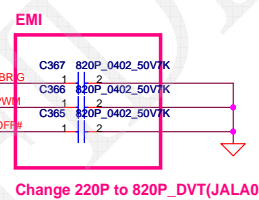
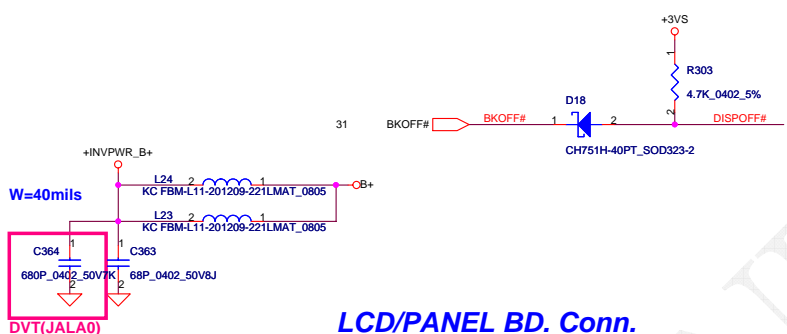
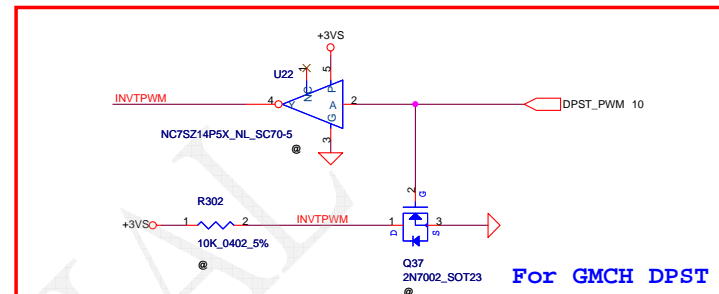
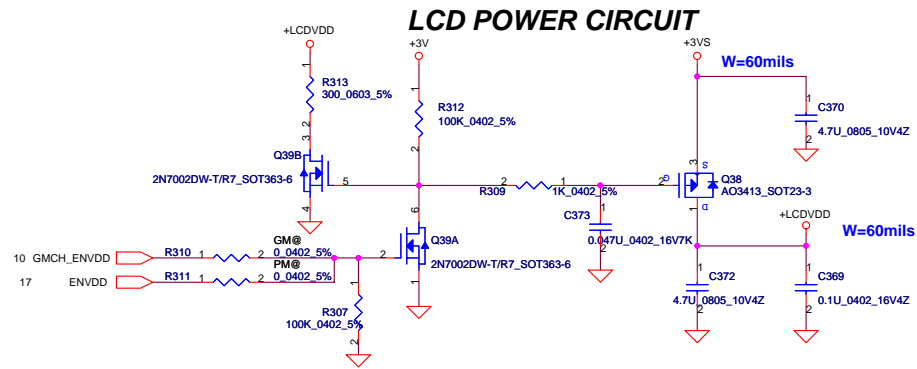


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- 10 PCIE_MTX_C_GRX_N[0..15] PCIE MTX_C GRX NIO.15I
- 10 PCIE_MTX_C_GRX_P[0..15] PCIE MTX_C GRX P[0..15]I
- 10 PCIE_GTX_C_MRX_N[0..15] PCIE GTX_C MRX NIO.15I
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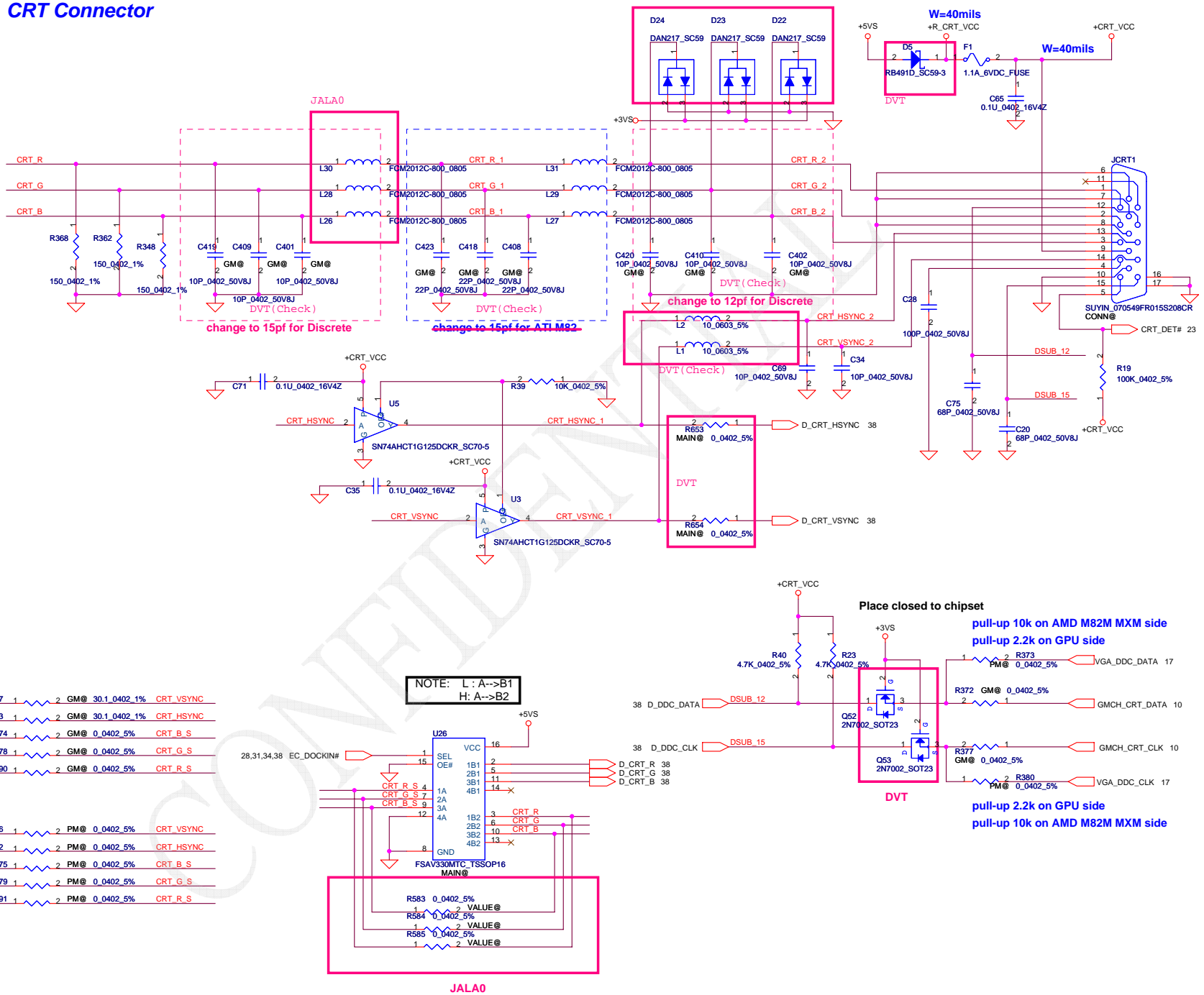


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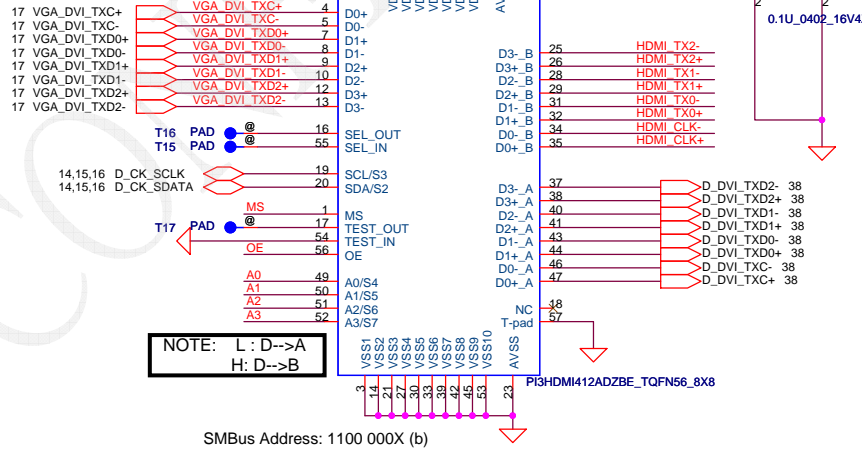
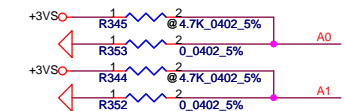
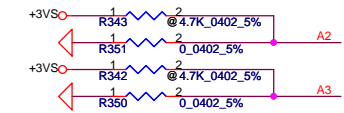
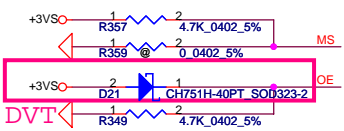
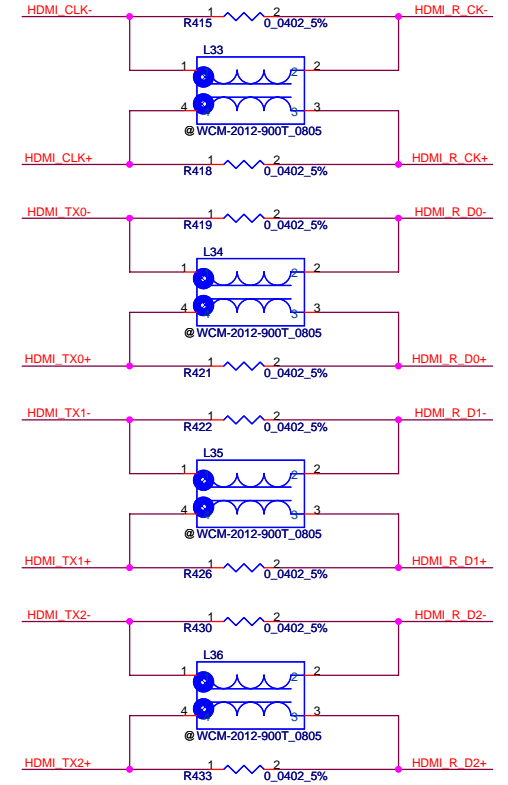
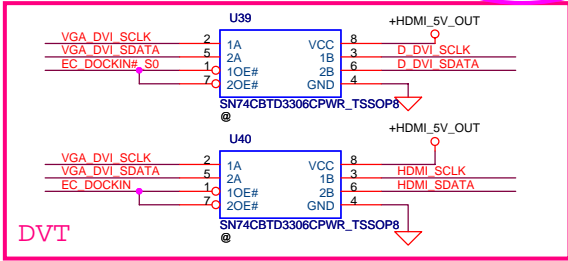
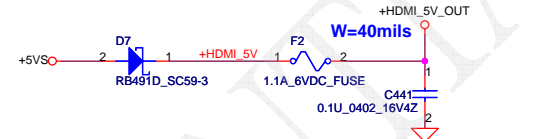
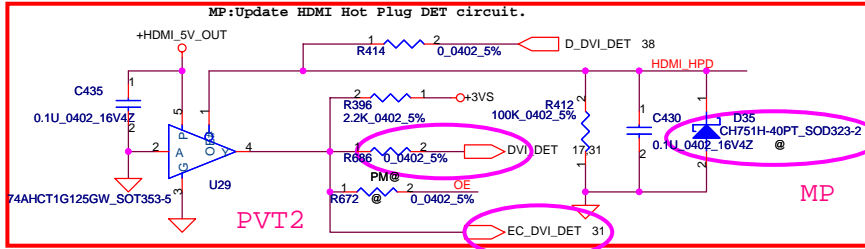
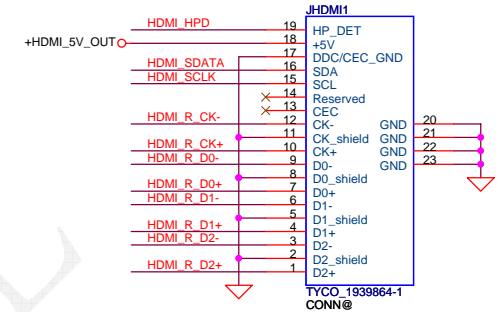
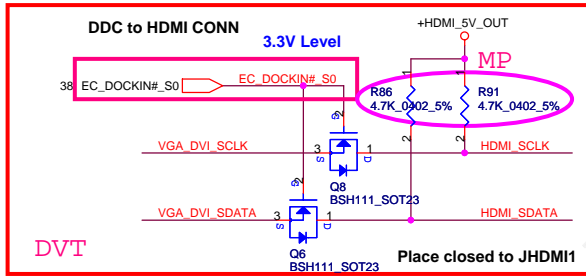
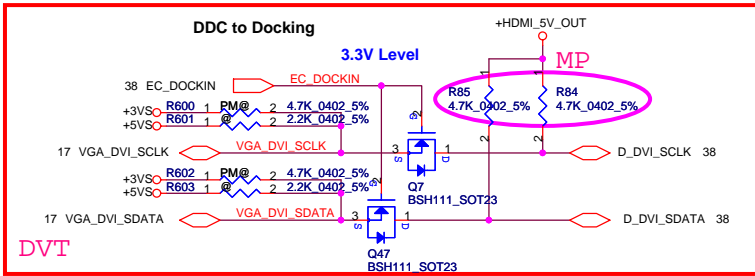
CRT Connector



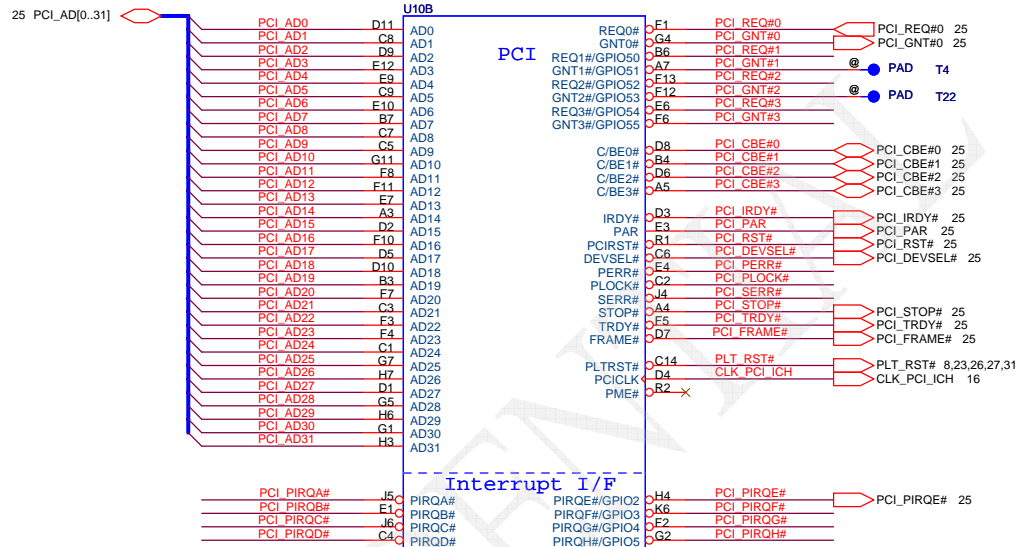
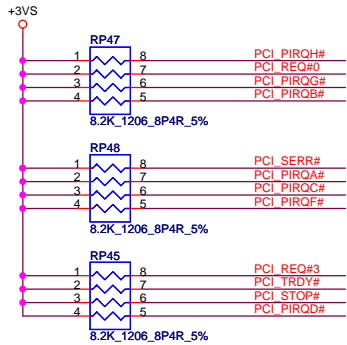
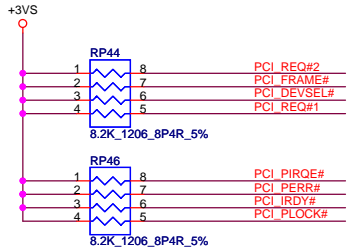
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- 10 GMCH_CRT_HSYNC R83 1 2 GM@ 30.1_0402_1% CRT_HSYNC
- 10 GMCH_CRT_B R374 1 2 GM@ 0_0402_5% CRT_B_S
- 10 GMCH_CRT_G R378 1 2 GM@ 0_0402_5% CRT_G_S
- 10 GMCH_CRT_R R390 1 2 GM@ 0_0402_5% CRT_R_S

- 17 VGA_CRT_VSYNC R66 1 2 PM@ 0_0402_5% CRT_VSYNC
- 17 VGA_CRT_HSYNC R82 1 2 PM@ 0_0402_5% CRT_HSYNC
- 17 VGA_CRT_B R375 1 2 PM@ 0_0402_5% CRT_B_S
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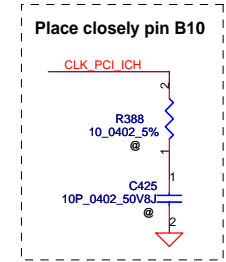
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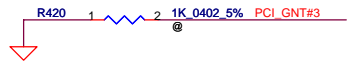
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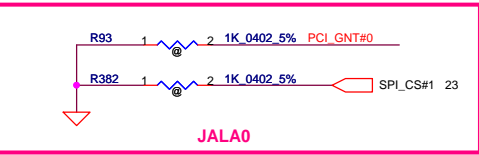
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)



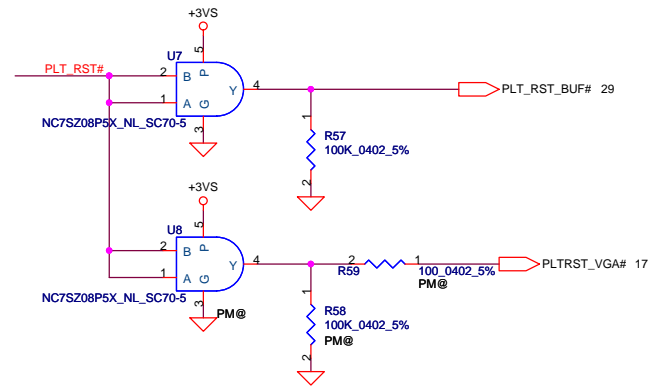
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



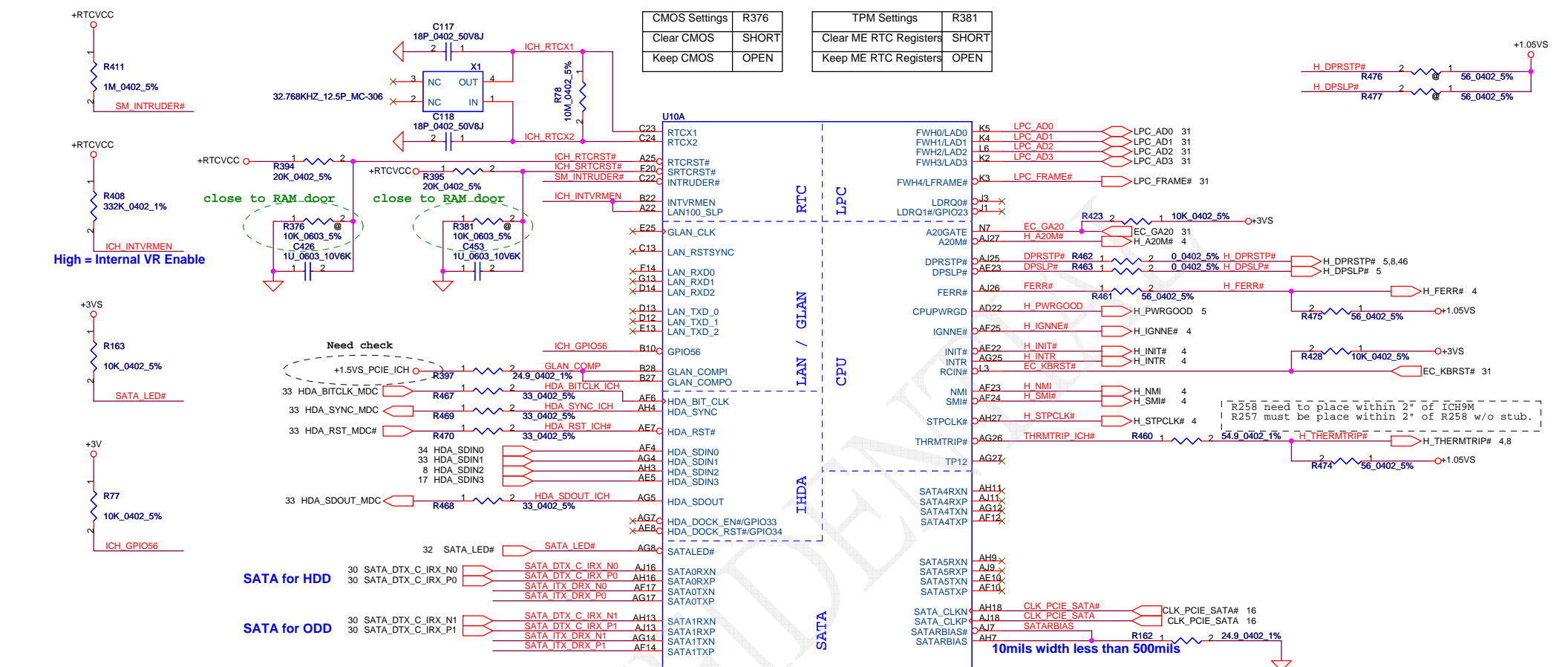
DVT ICH9-M: SA00002AN10 (S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)
 PVT ICH9-M: SA00002JH00 (S IC AF82801IBM QT09 A3 PBG 676P ICH9M)
 Pre-MP ICH9-M: SA00002JH70 (S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)



For VGA/B

CMOS Settings	R376
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R381
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN



SATA for HDD

SATA for ODD

HDA for AUDIO

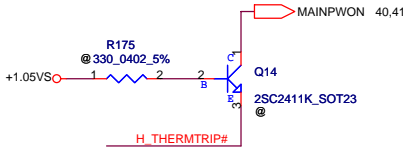
HDA for GMCH

HDA for VGA

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1

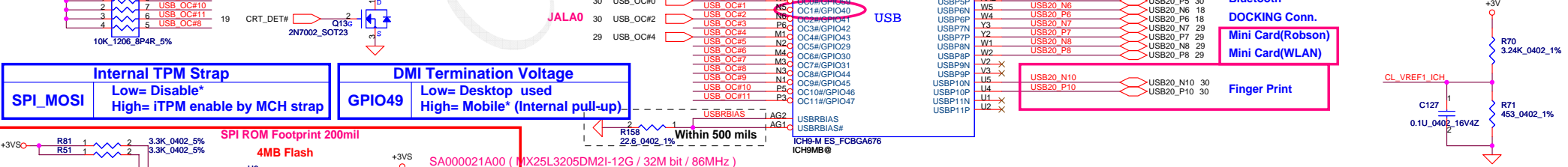
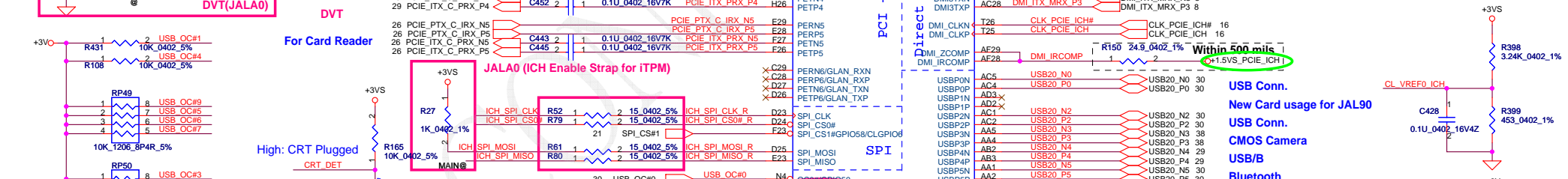
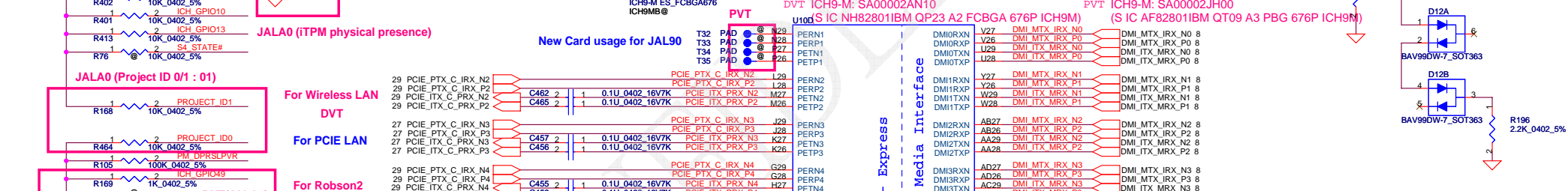
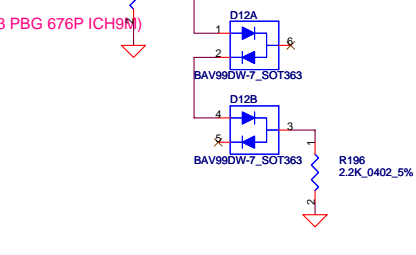
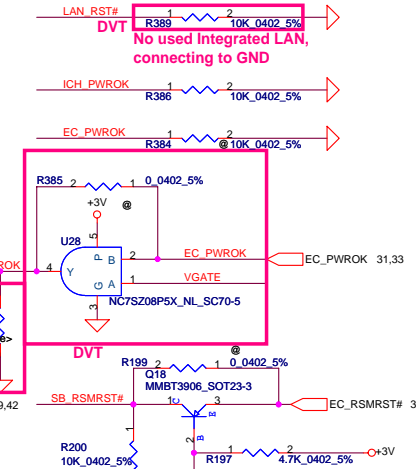
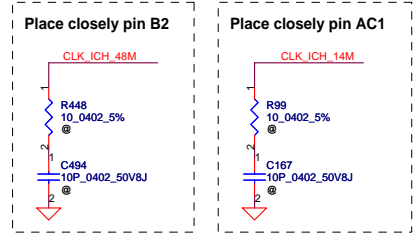
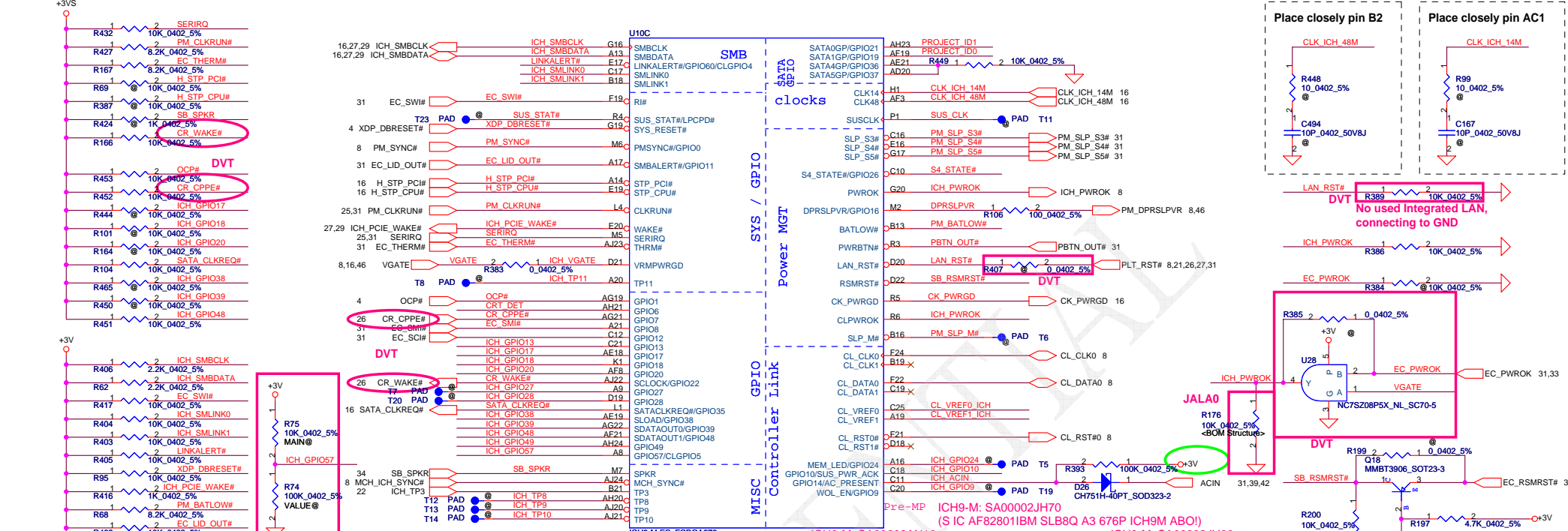
Flash Descriptor Security Override Strap
 GPIO33 Low= Descriptor Security override
 High= Default* (Internal pull-up)

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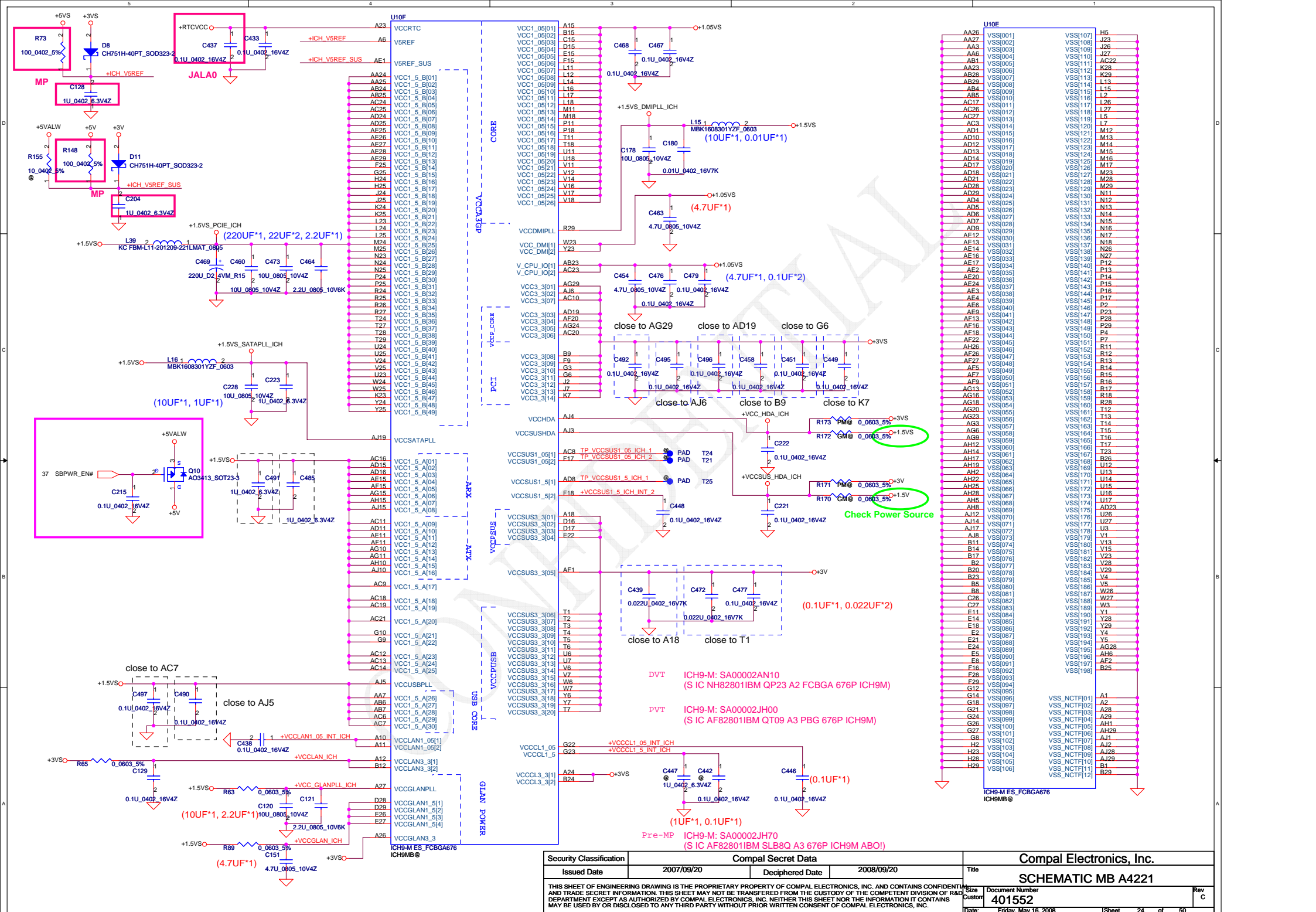
10mils width less than 500mils
 R162 1 2 24.9_0402_1%
 ICH9-M: SA00002AN10 (S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)
 PVT ICH9-M: SA00002JH00 (S IC AF82801IBM QT09 A3 PBG 676P ICH9M)
 Pre-MP ICH9-M: SA00002JH70 (S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)

R258 need to place within 2" of ICH9M
 R257 must be place within 2" of R258 w/o stub.



Internal TPM Strap Low= Disable* High= iTPM enable by MCH strap		DMI Termination Voltage Low= Desktop used High= Mobile* (Internal pull-up)	
SPI MOSI		GPIO49	
SPI ROM Footprint 200mil 4MB Flash SAO0002A100 (MX25L3205DM2L-12G / 32M bit / 86MHz)		No Reboot Strap Low= Default* High= "No Reboot"	
PVT(Add inner pad length for 150mil) ICH_SPI ROM for iTPM & ME		Security Classification Issued Date: 2007/09/20 Deciphered Date: 2008/09/20	
JALA0 (Project ID 0/1 : 01) For Wireless LAN For PCIE LAN For Robson2 For Card Reader		Compal Secret Data Title: SCHEMATIC MB A4221	

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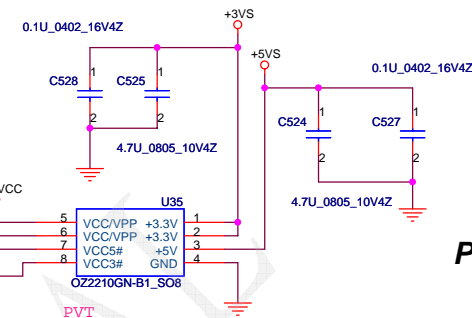
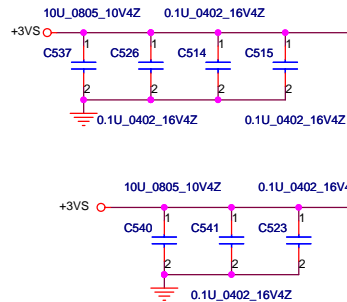
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Compal Electronics, Inc.		
SCHEMATIC MB A4221		
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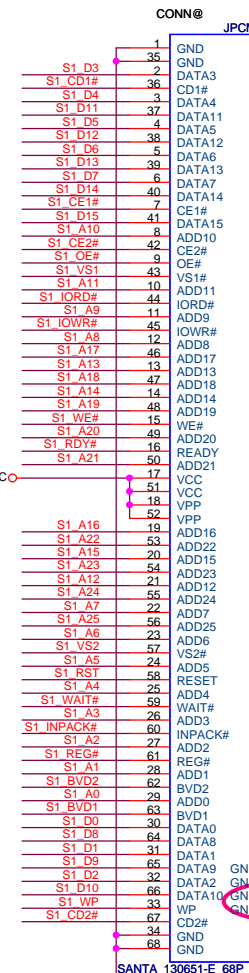
21 PCI_AD[0..31] PCI AD[0..31]

21 PCI_CBE#[0..3] PCI CBE#[0..3]

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



PCMCIA Socket



Footprint as SANTA_130651-E_68P_LT-S
DVT(JALA0)

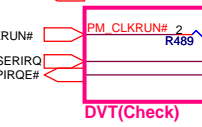
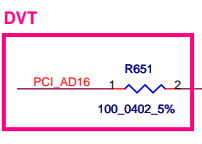
NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

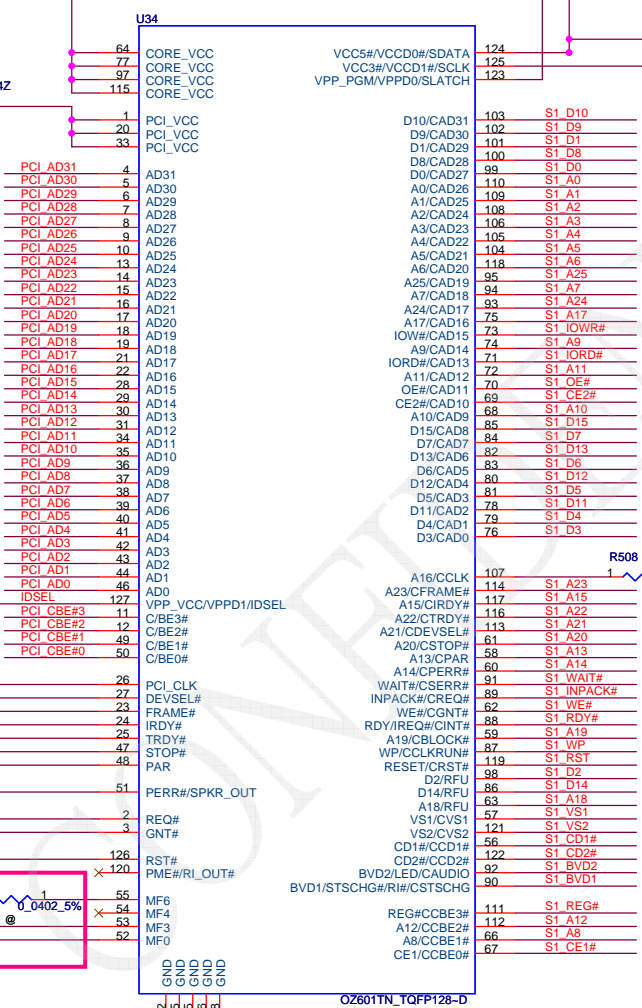
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

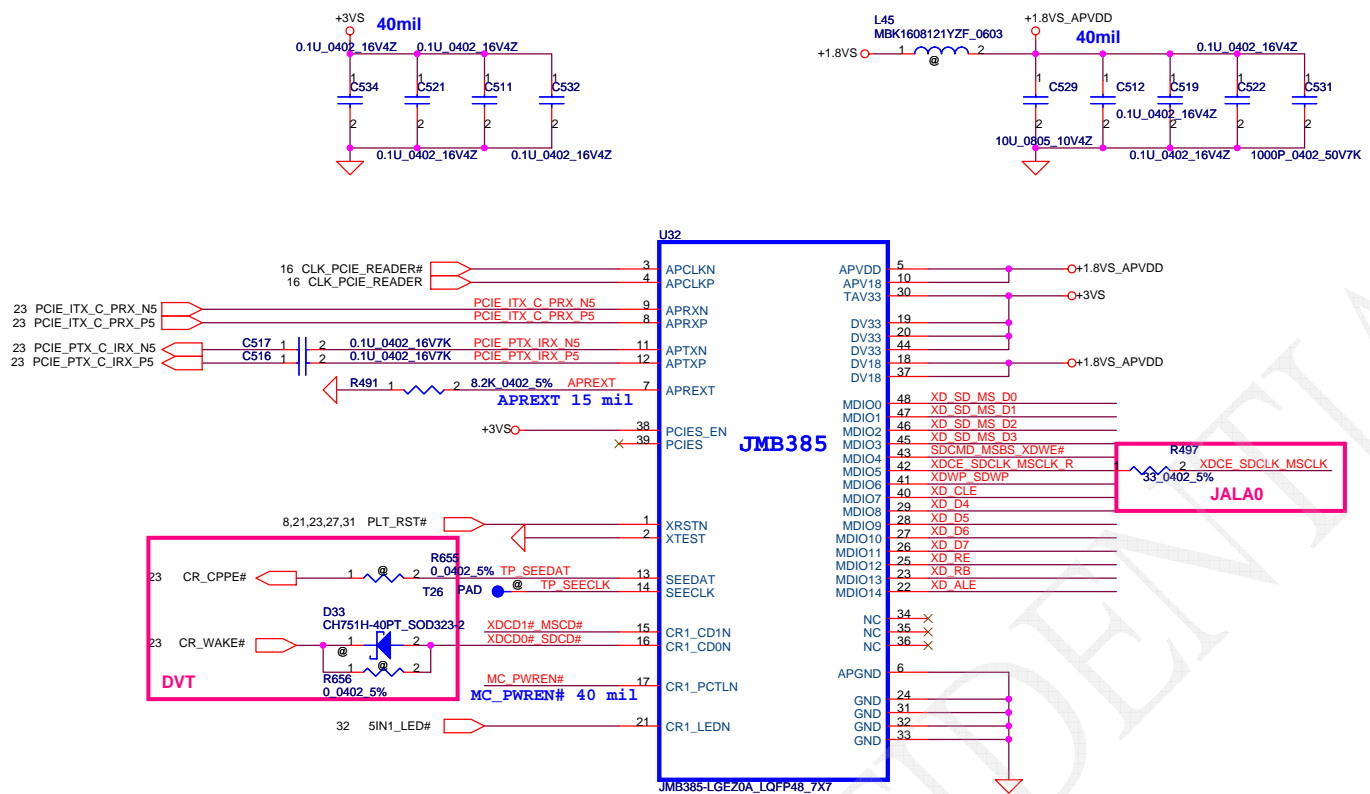
VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN F4



22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

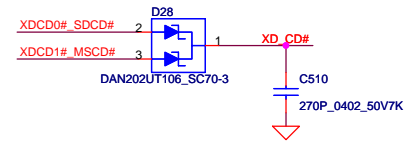
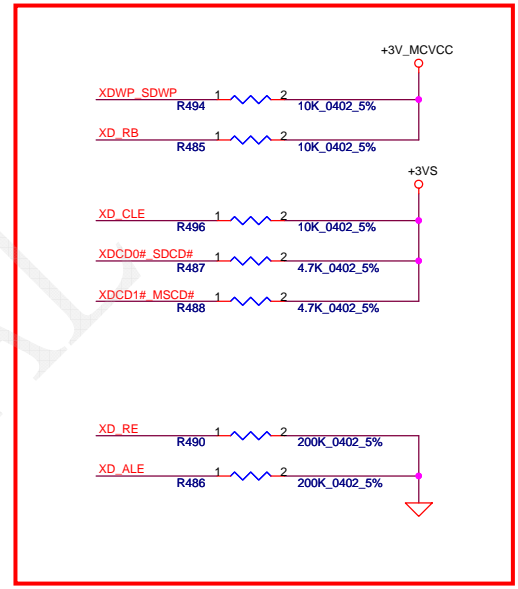


Pin	Signal	Pin	Signal
103	S1 D10	124	VCC5#/VCCD0#/SDATA
102	S1 D9	125	VCC3#/VCCD1#/SCLK
101	S1 D1	126	CORE_VCC
100	S1 D8	123	VPP_PGM/VPPD0/SLATCH
99	S1 D0		
98	S1 A0		
97	S1 A1		
96	S1 A2		
95	S1 A3		
94	S1 A4		
93	S1 A5		
92	S1 A6		
91	S1 A7		
90	S1 A24		
89	S1 A17		
88	S1 IOWR#		
87	S1 A9		
86	S1 IORD#		
85	S1 A11		
84	S1 A12		
83	S1 CE2#		
82	S1 A10		
81	S1 D15		
80	S1 D7		
79	S1 D13		
78	S1 D6		
77	S1 D5		
76	S1 D11		
75	S1 D4		
74	S1 D3		
73	S1 A23		
72	S1 A15		
71	S1 A22		
70	S1 A21		
69	S1 A20		
68	S1 A14		
67	S1 WAIT#		
66	S1 INPACK#		
65	S1 WE#		
64	S1 RDY#		
63	S1 VS2		
62	S1 A6		
61	S1 VS2		
60	S1 A23		
59	S1 A12		
58	S1 A24		
57	S1 A7		
56	S1 A25		
55	S1 A6		
54	S1 A23		
53	S1 A12		
52	S1 A24		
51	S1 A7		
50	S1 A25		
49	S1 A6		
48	S1 A23		
47	S1 A12		
46	S1 A24		
45	S1 A7		
44	S1 A25		
43	S1 A6		
42	S1 A23		
41	S1 A12		
40	S1 A24		
39	S1 A7		
38	S1 A25		
37	S1 A6		
36	S1 A23		
35	S1 A12		
34	S1 A24		
33	S1 A7		
32	S1 A25		
31	S1 A6		
30	S1 A23		
29	S1 A12		
28	S1 A24		
27	S1 A7		
26	S1 A25		
25	S1 A6		
24	S1 A23		
23	S1 A12		
22	S1 A24		
21	S1 A7		
20	S1 A25		
19	S1 A6		
18	S1 A23		
17	S1 A12		
16	S1 A24		
15	S1 A7		
14	S1 A25		
13	S1 A6		
12	S1 A23		
11	S1 A12		
10	S1 A24		
9	S1 A7		
8	S1 A25		
7	S1 A6		
6	S1 A23		
5	S1 A12		
4	S1 A24		
3	S1 A7		
2	S1 A25		
1	S1 A6		

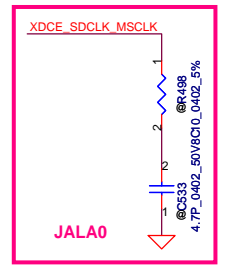
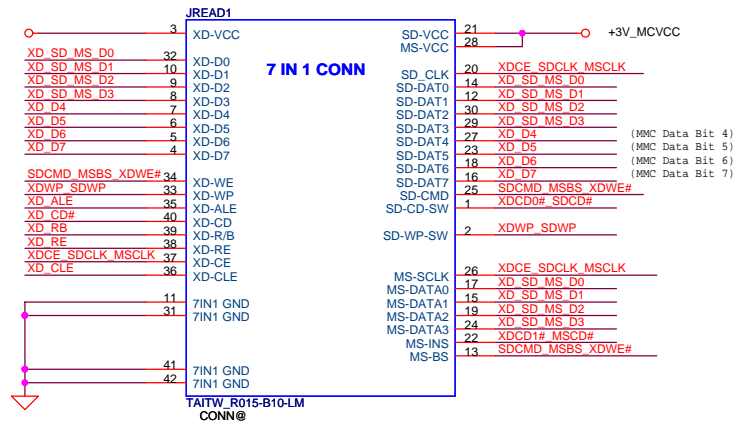


DVT SA00001W910 (S IC JMB385-LGEZ0B LQFP 48P)

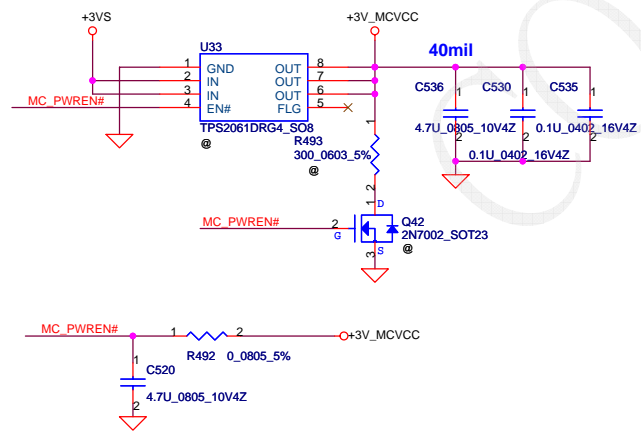
MDIO PULL HIGH/LOW ?



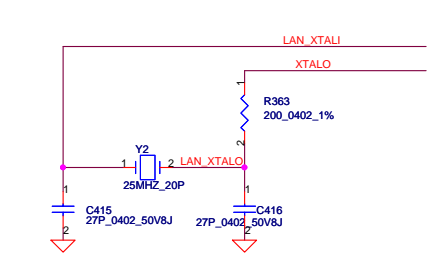
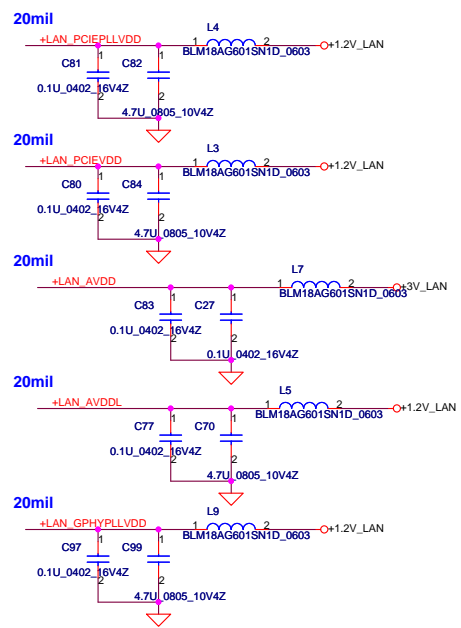
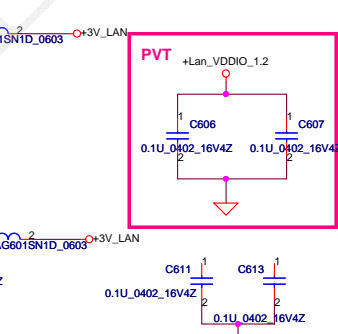
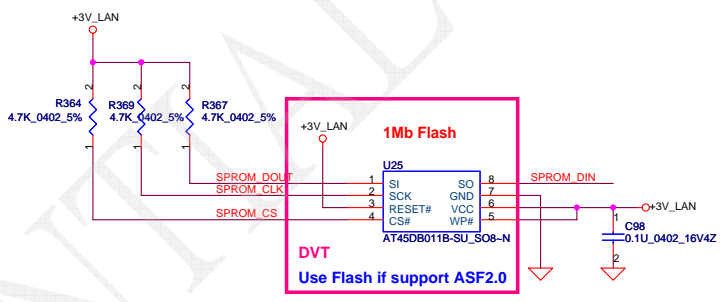
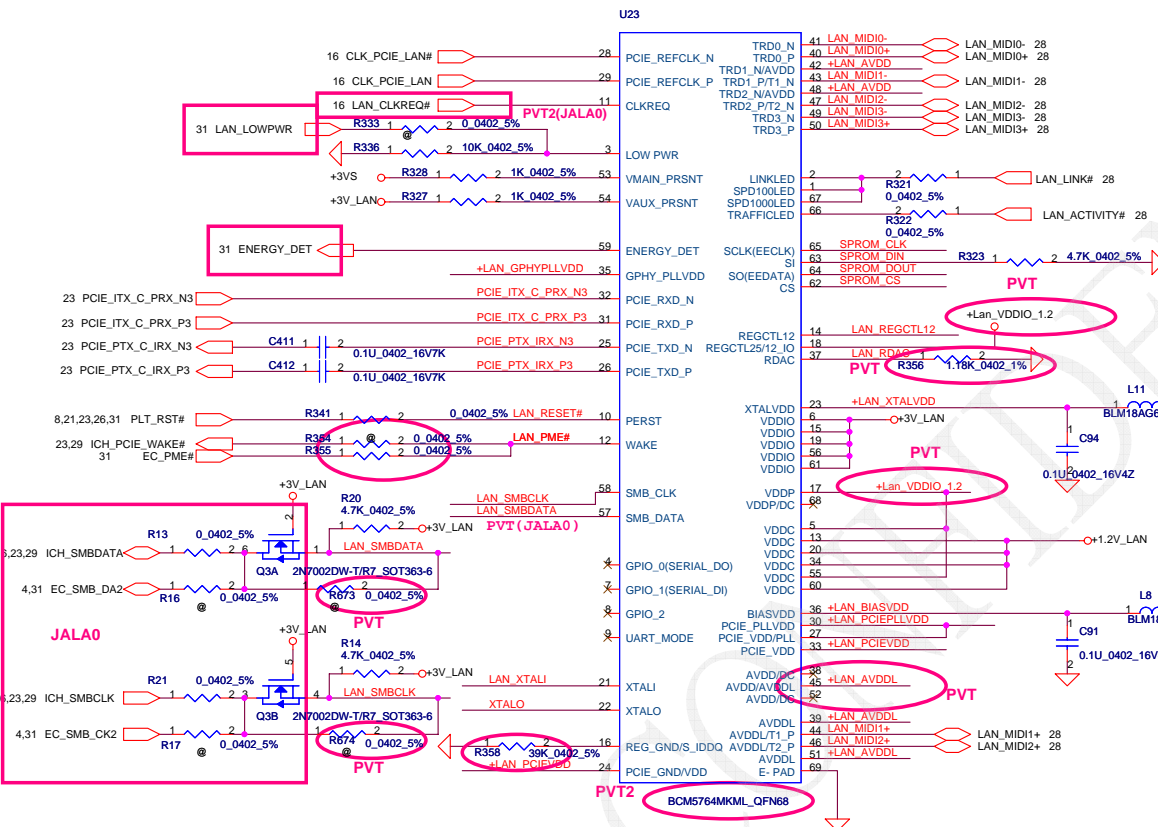
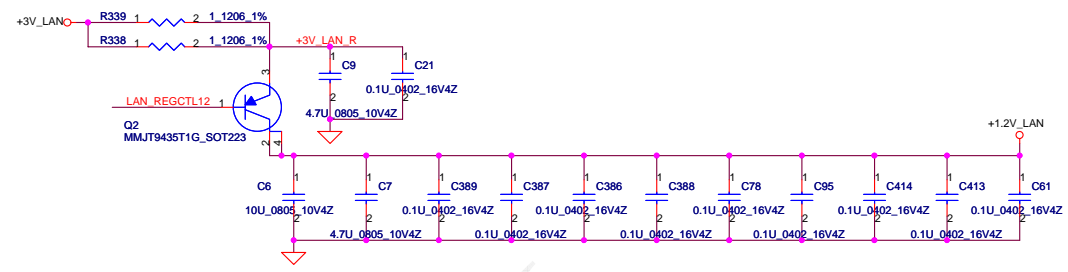
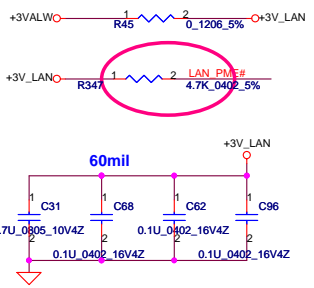
4 IN 1 Socket Push Type(New)



Memory Card Power Switch



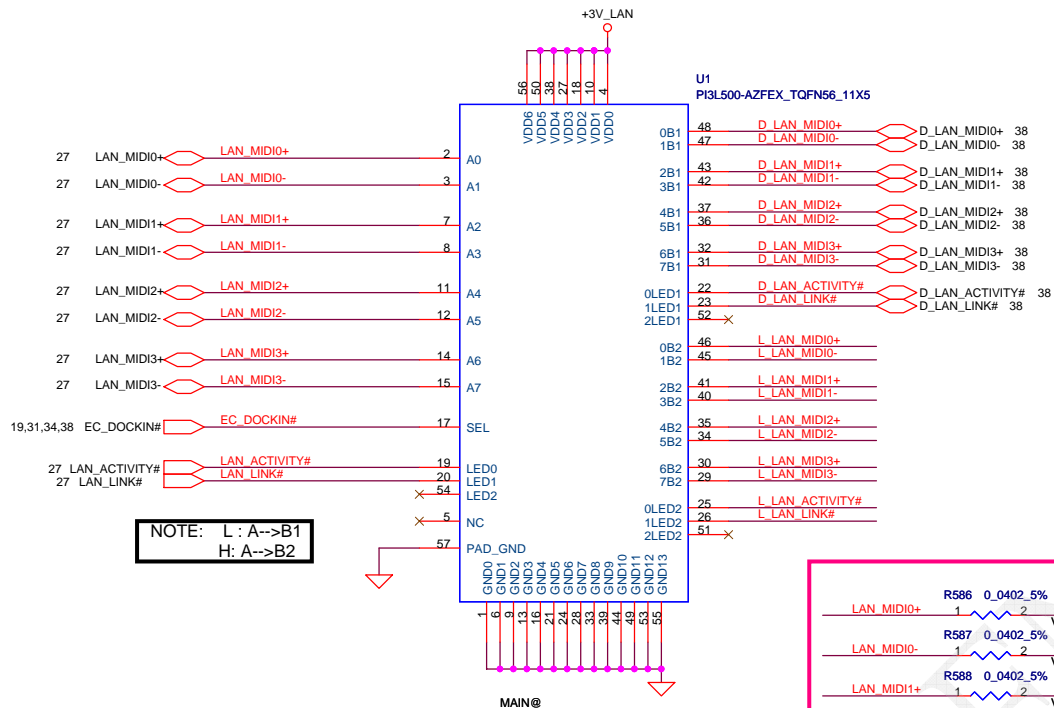
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Date:	Friday, May 16, 2008	Sheet	26	of	50



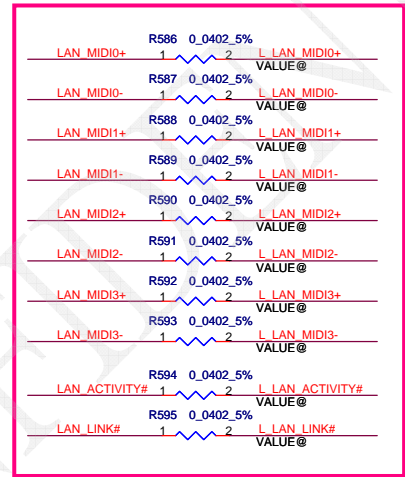
DVT SA000025P00
(S IC BCM5764MA0KMLG QFN 68P E-LAN CTRL)

PVT SA000025P20
(S IC BCM5764MKMLG P20 QFN 68P E-L)

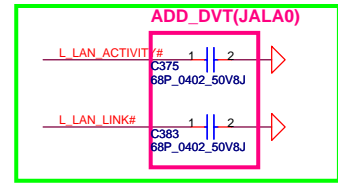
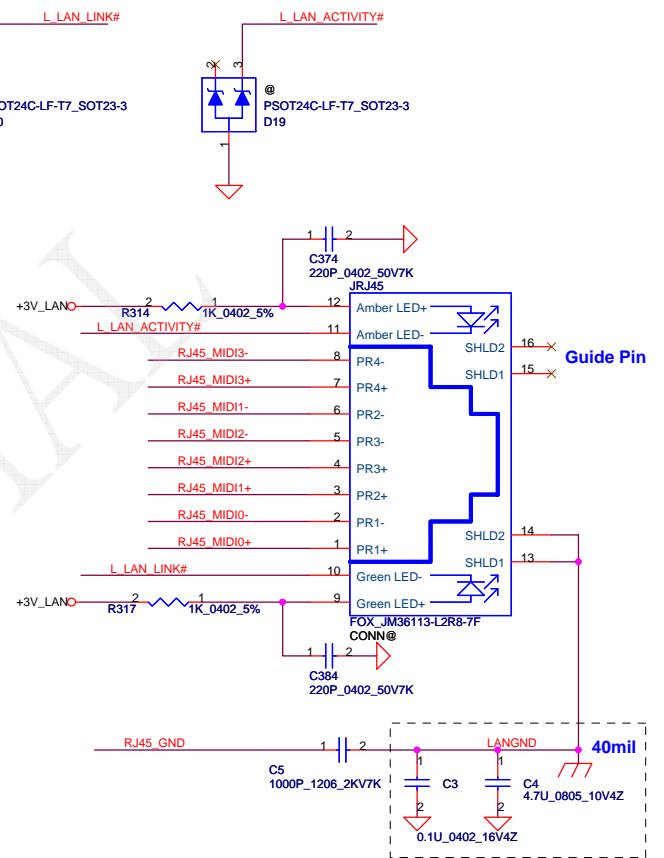
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				Date: Friday, May 16, 2008	Sheet 27 of 50



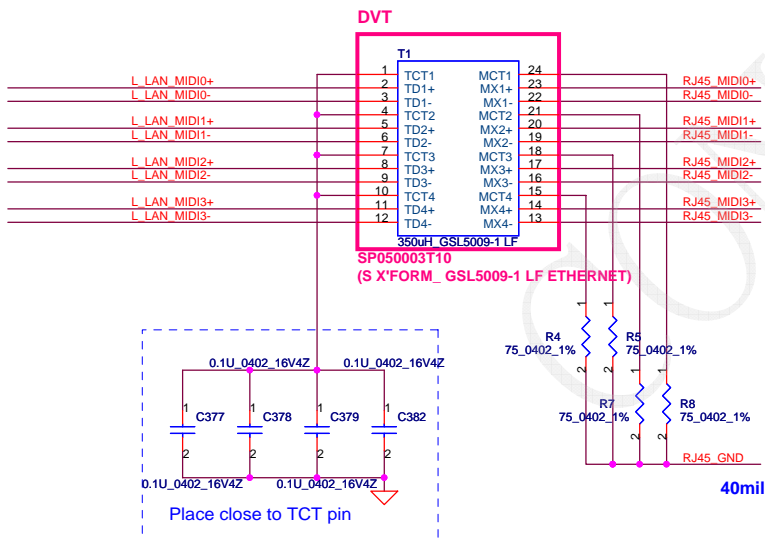
NOTE: L : A-->B1
H: A-->B2



JALA0



For EMI

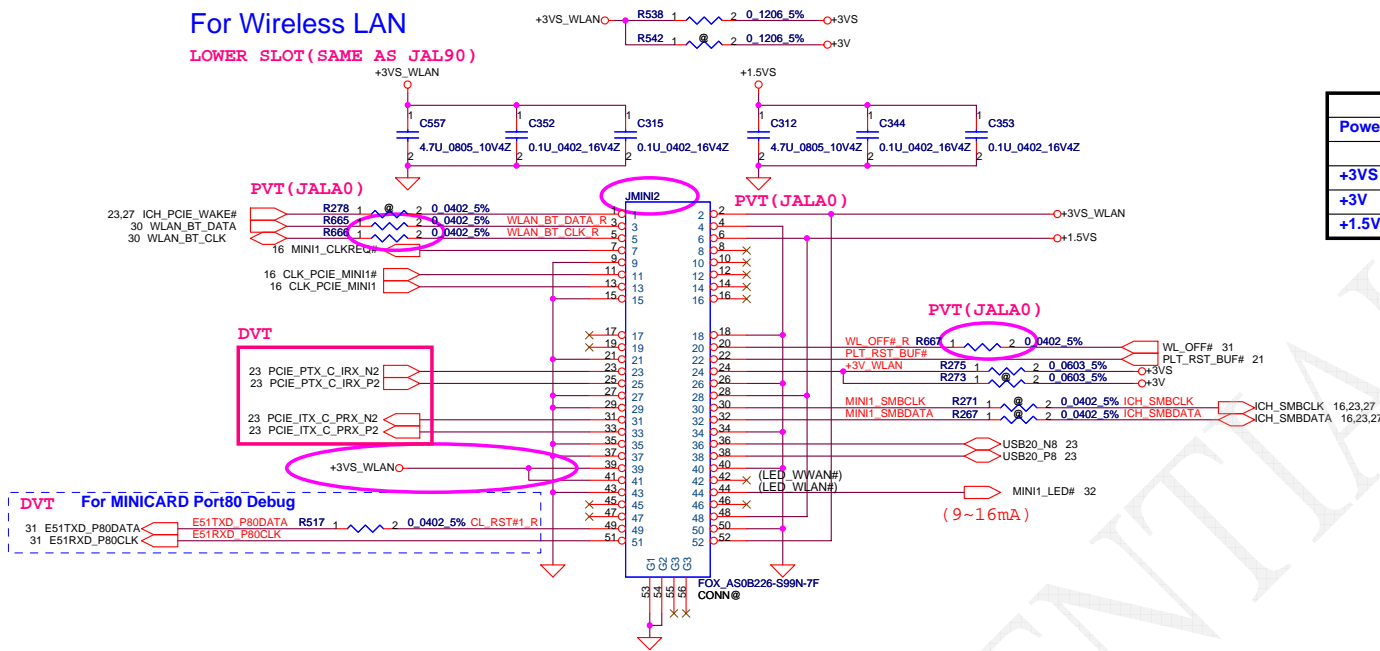


Place close to TCT pin

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				401552	C
Date: Friday, May 16, 2008				Sheet	28 of 50

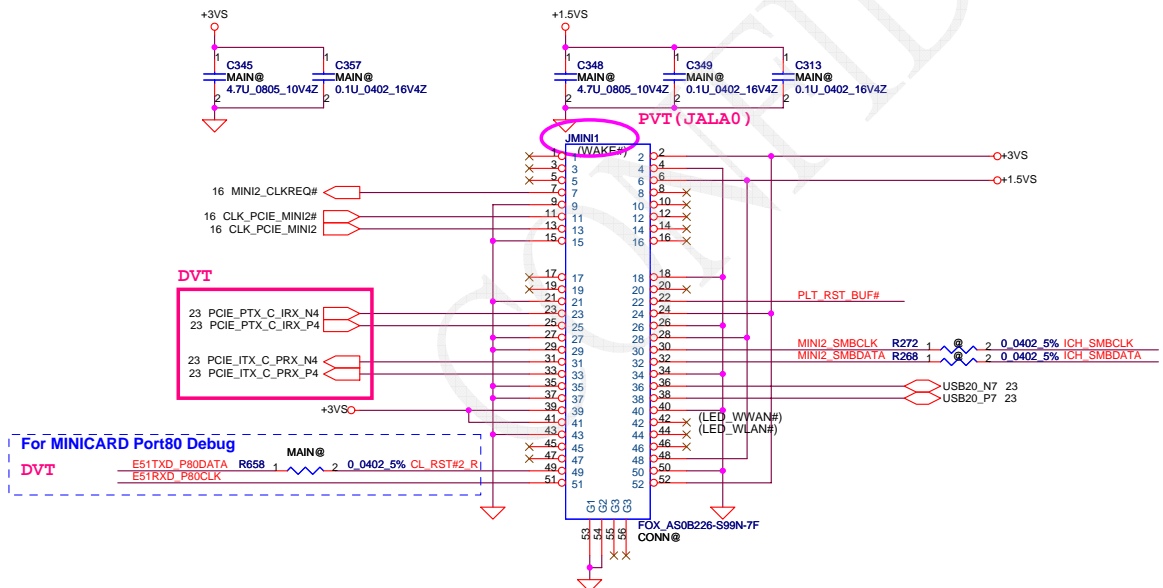
For Wireless LAN

LOWER SLOT (SAME AS JAL90)

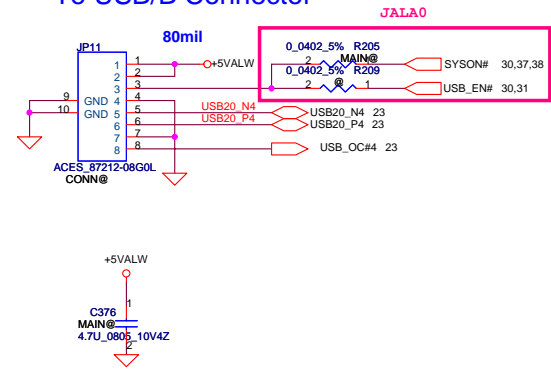


For Robson2

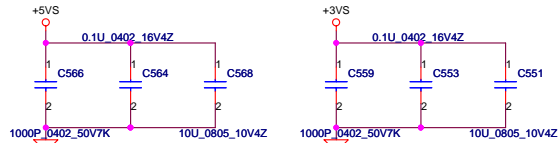
UPPER SLOT (SAME AS JAL90)



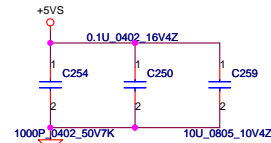
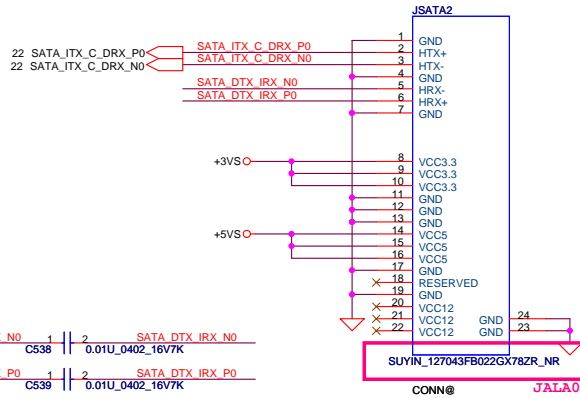
To USB/B Connector



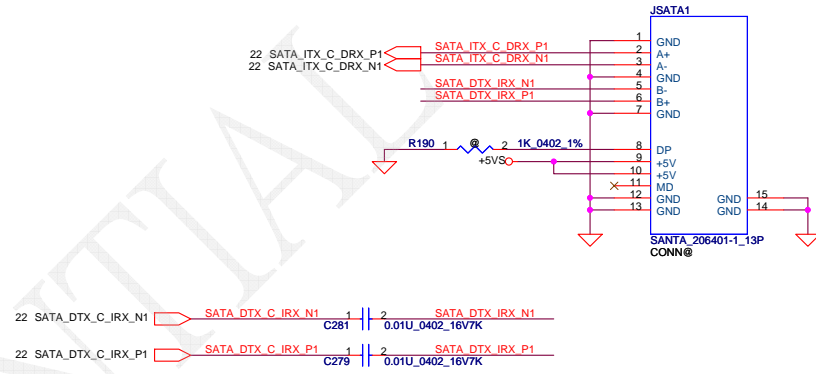
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	SHEMATIC MB A4221
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Date: Friday, May 16, 2008				Rev C



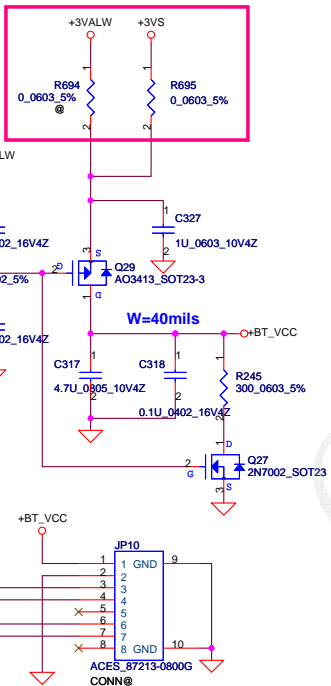
SATA HDD Conn.



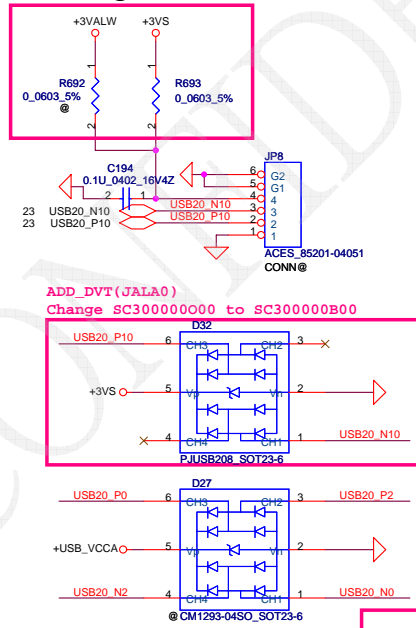
SATA ODD Conn.



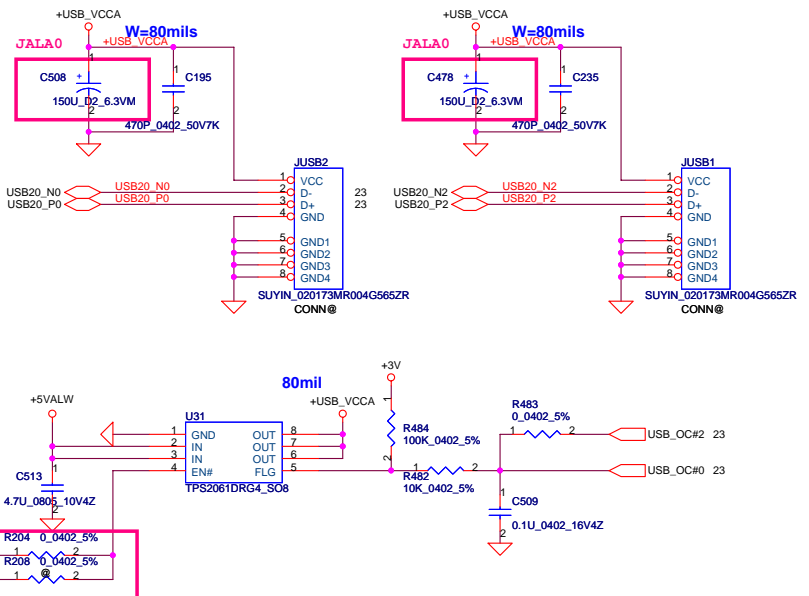
Bluetooth Conn.



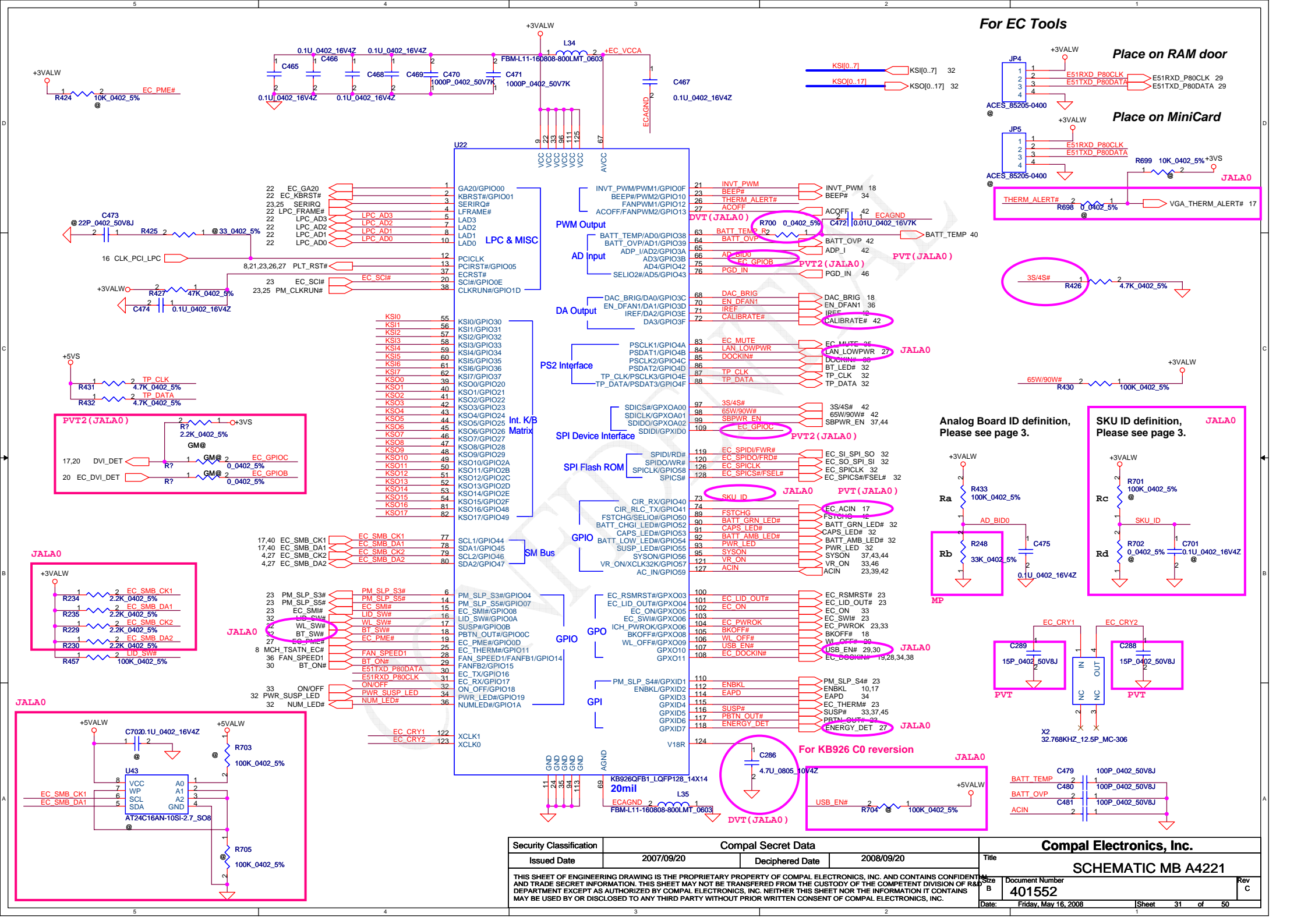
Finger Print Conn.



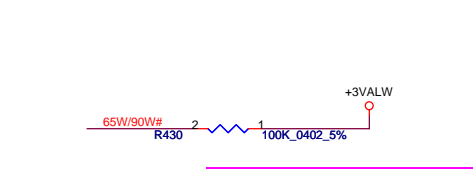
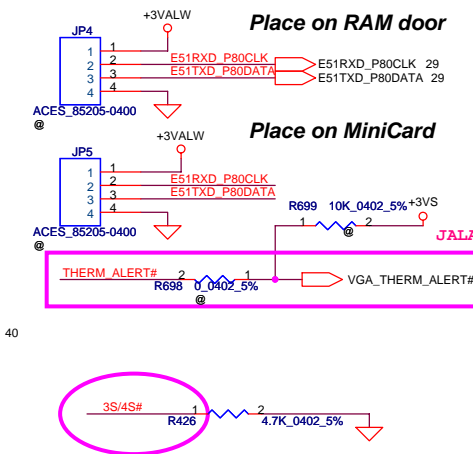
USB CONN. (Stack-up Type)



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Document Number	401552		Rev	C	
Date:	Friday, May 16, 2008		Sheet	30 of 50	

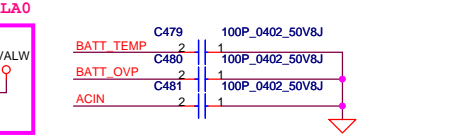
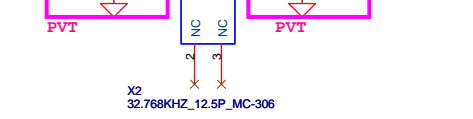
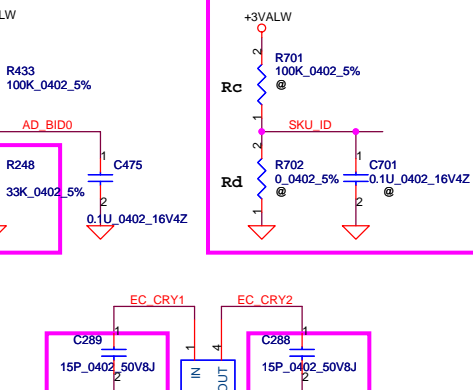


For EC Tools

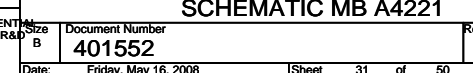


Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.



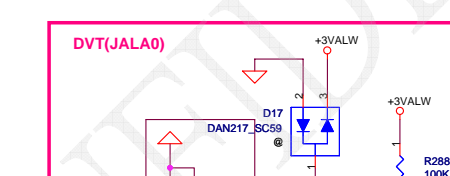
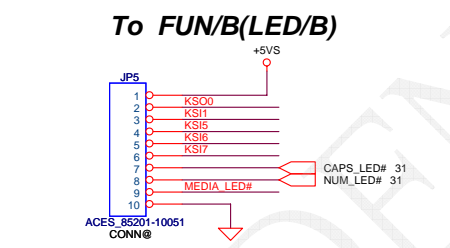
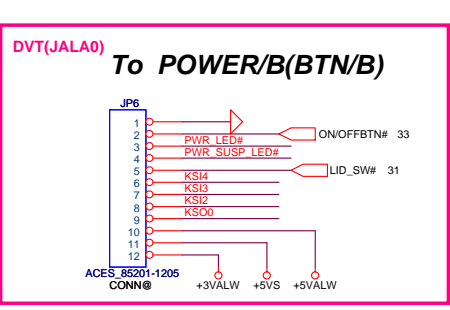
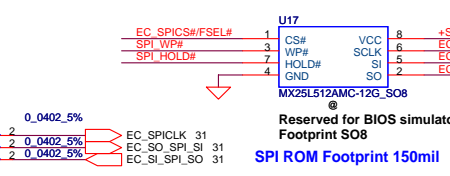
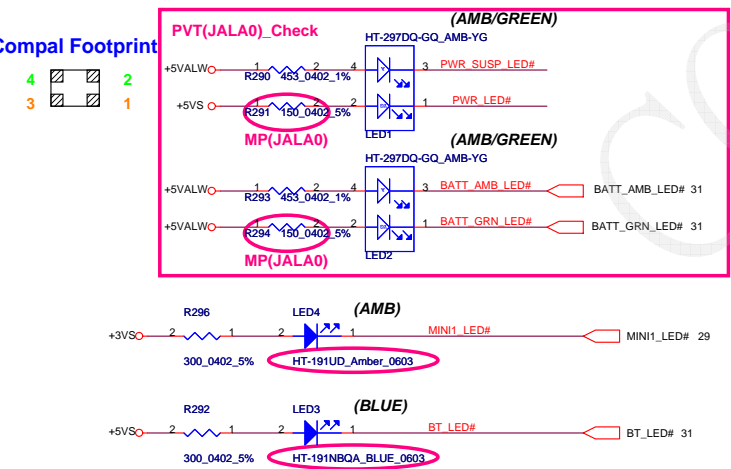
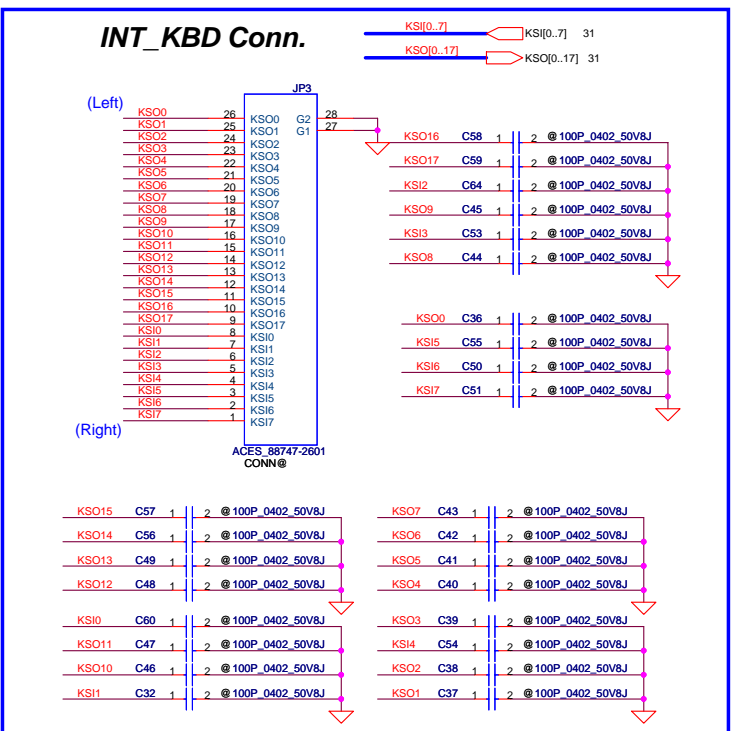
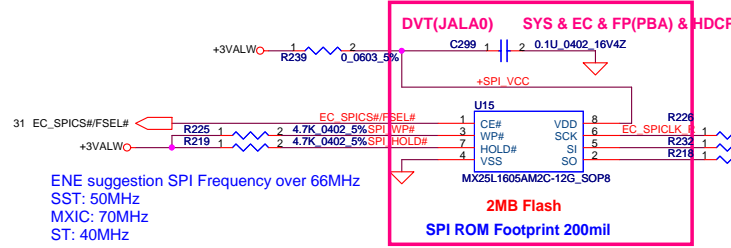
For KB926 C0 reversion



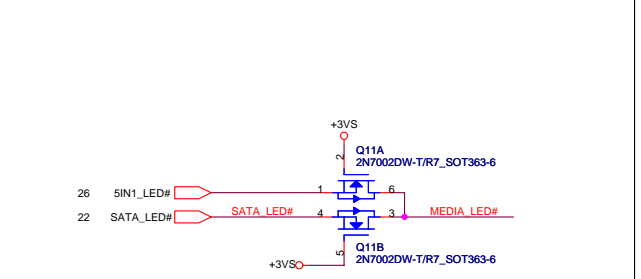
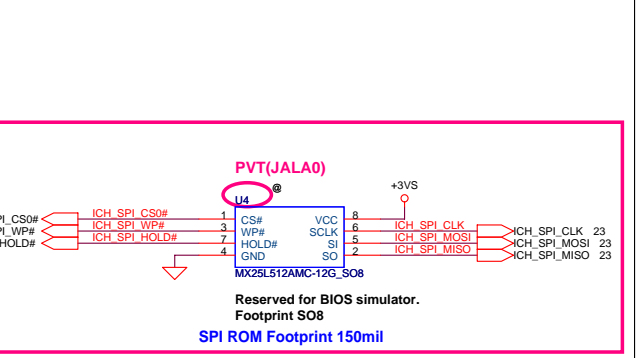
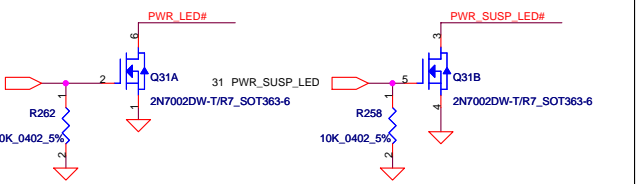
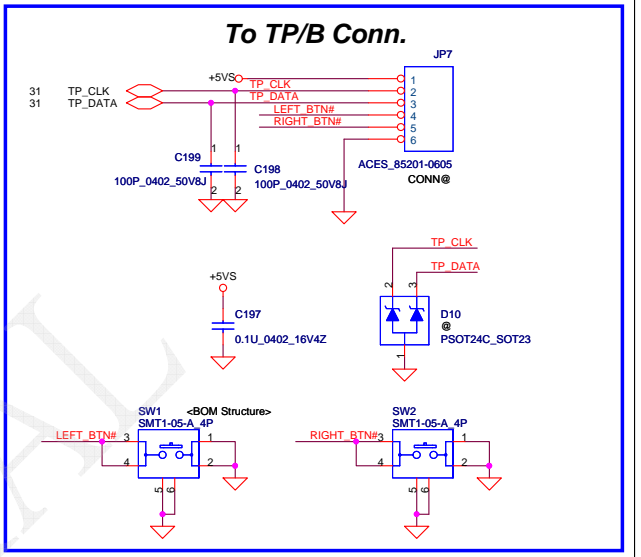
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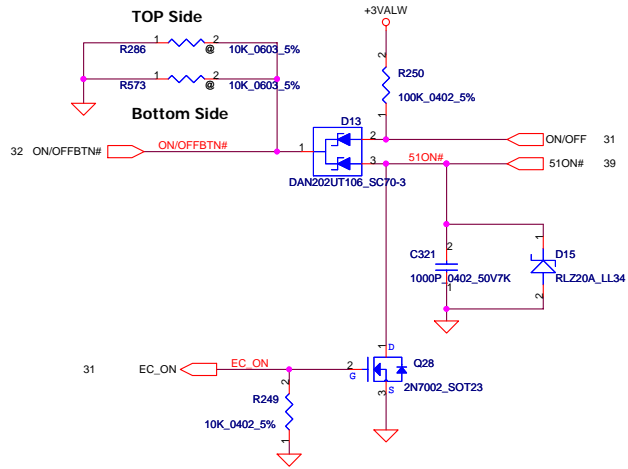
KSO0	
KSI1	PRESENTATION
KSI2	Program_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#
KSI6	SYNC
KSI7	LOCK



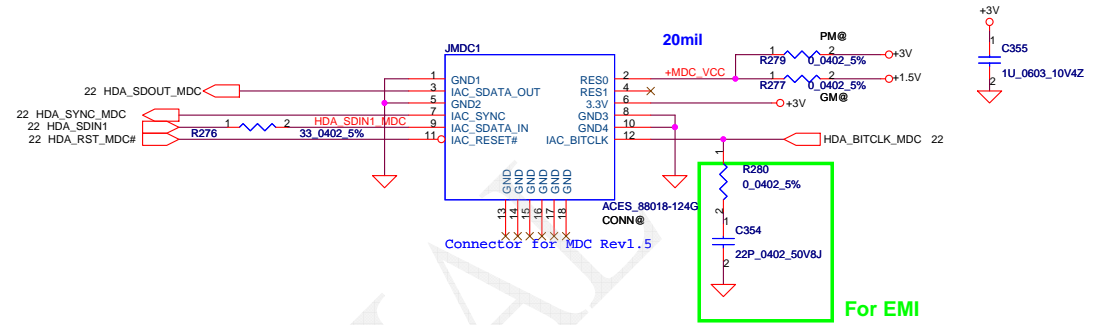
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Power Button

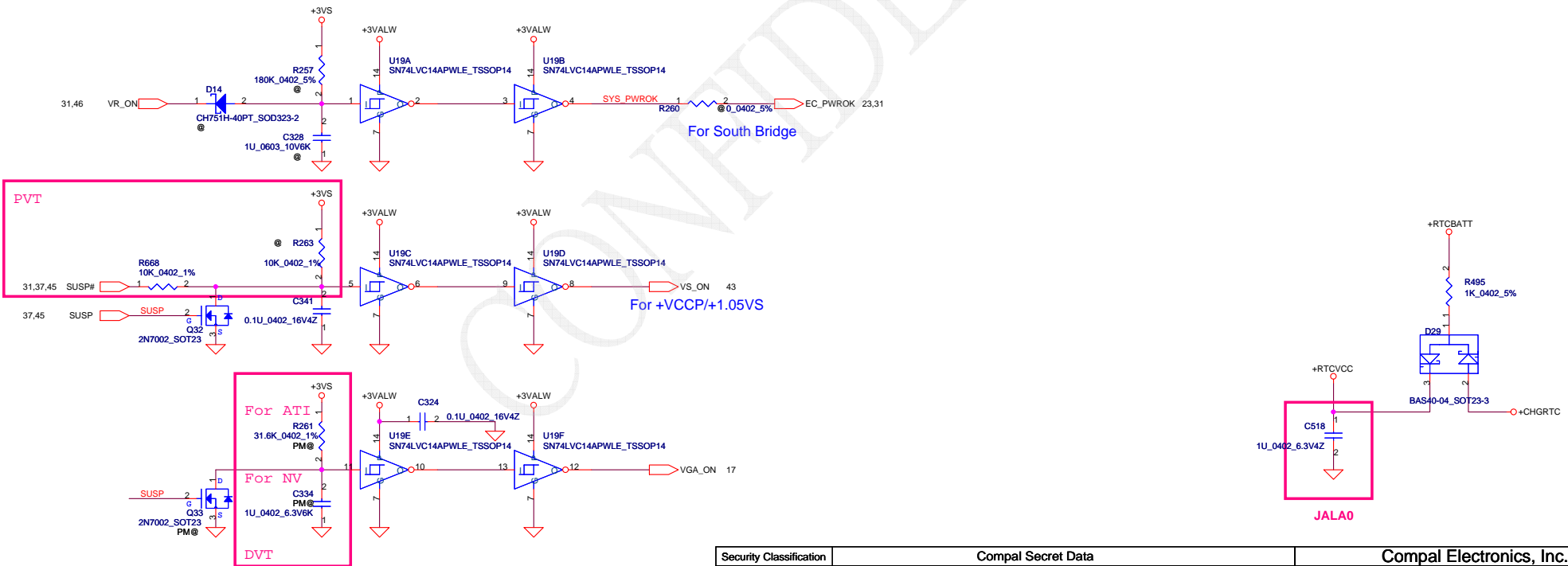
ON/OFF switch



HDA MDC Conn.

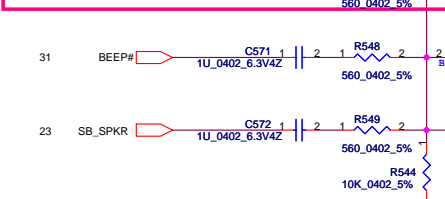


Power ON Circuit



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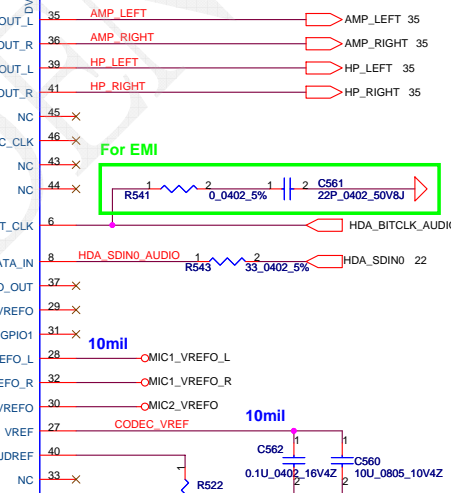
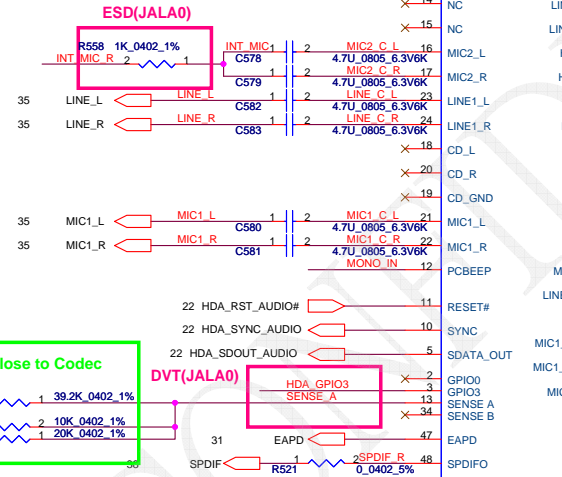
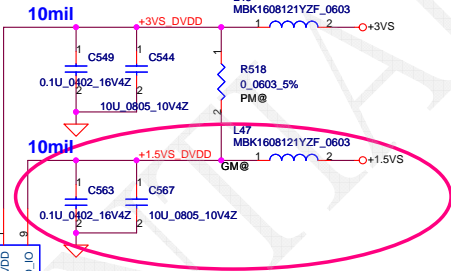
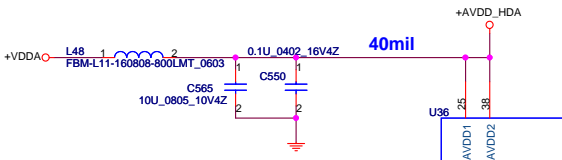
Cardbus usage for JALA0



BOM Option

ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@

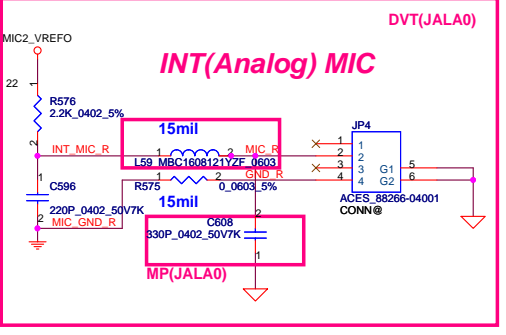
HD Audio Codec



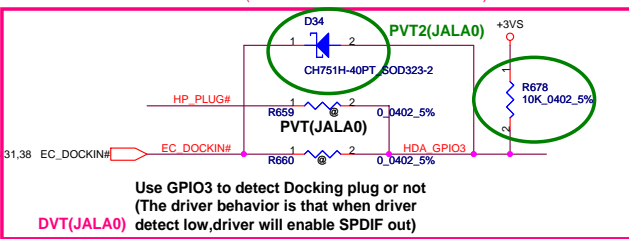
Place close to Codec

DVT(JALA0)

For EMI



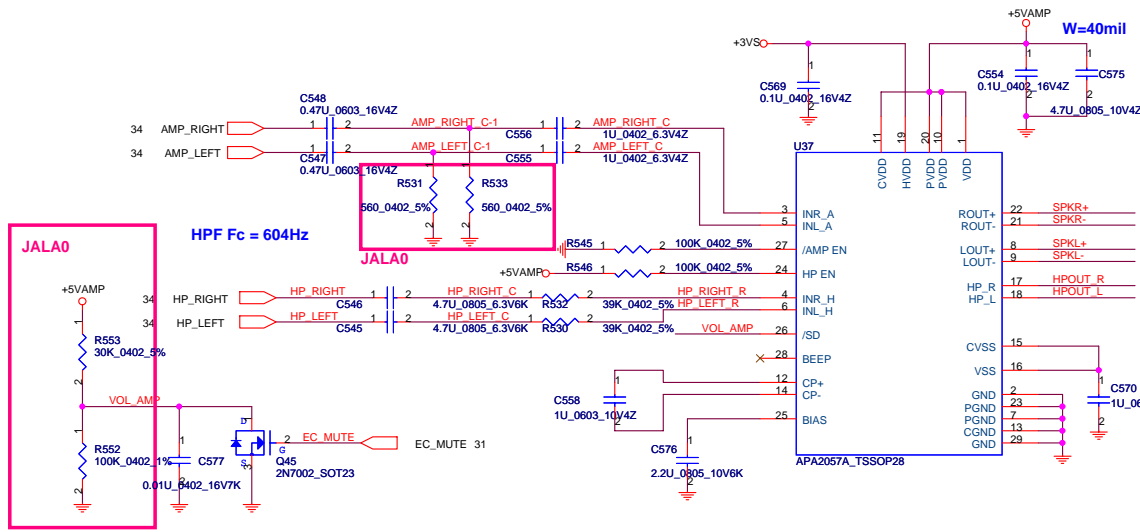
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



Use GPIO3 to detect Docking plug or not
(The driver behavior is that when driver detect low, driver will enable SPDIF out)

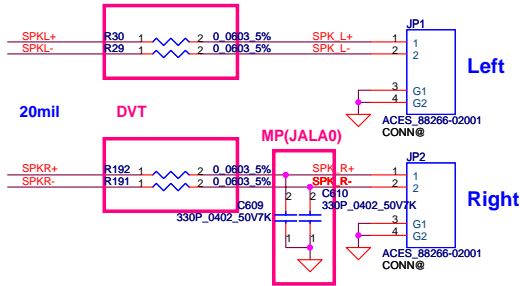
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Gain= 14dB

Int. Speaker Conn.



FSOV_MP(JALA0)
Change 75 to 54.9 ohm



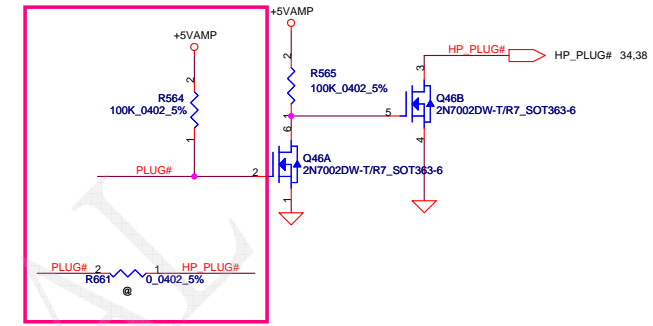
For Docking



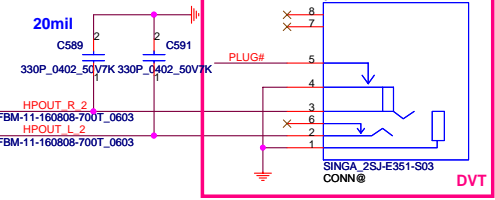
For Docking



For Docking

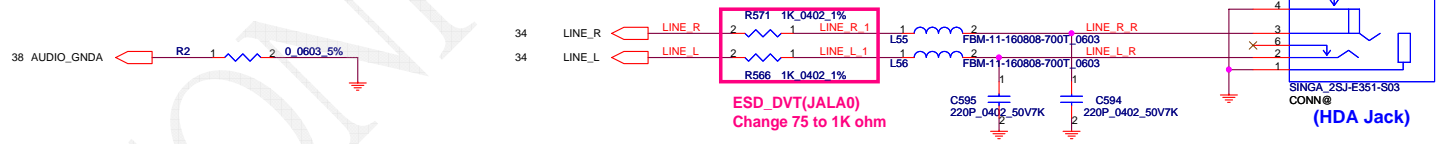


DVT(JALA0) LINE Out/HP Out JACK



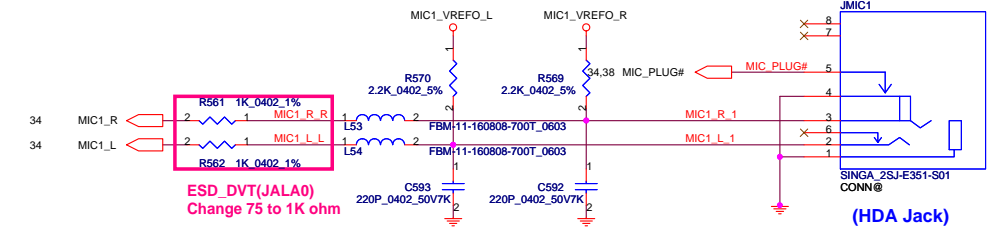
Change part

LINE-IN JACK



ESD_DVT(JALA0)
Change 75 to 1K ohm

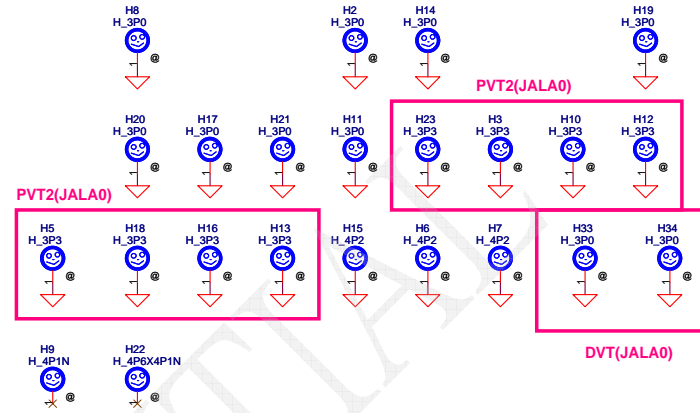
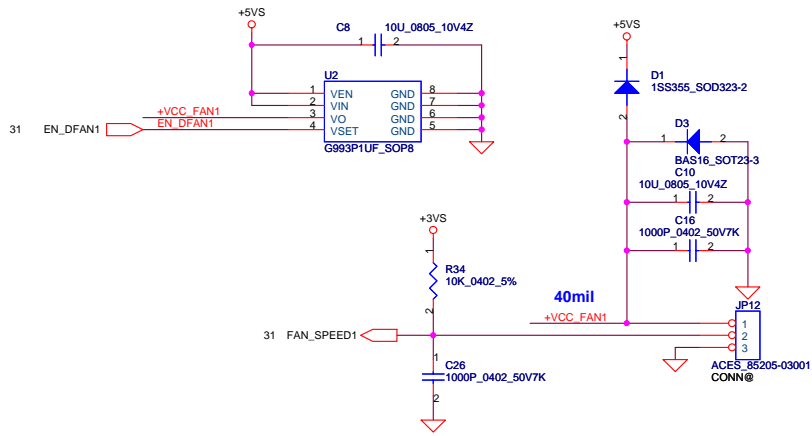
MIC JACK



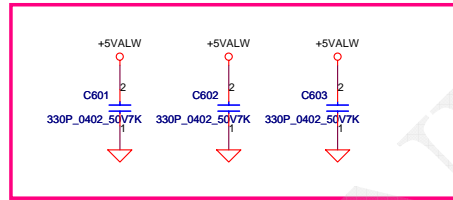
ESD_DVT(JALA0)
Change 75 to 1K ohm

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FAN1 Conn

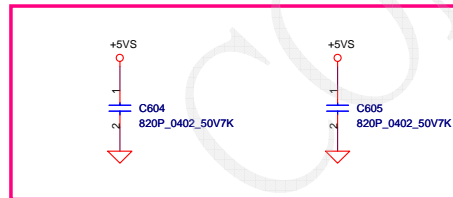


EMI



ADD_DVT(JALA0)

EMI

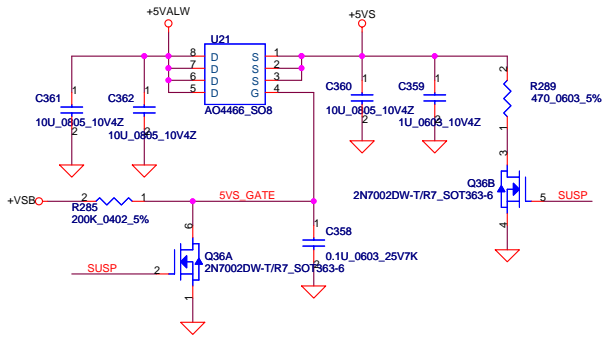


ADD_PVT(JALA0)

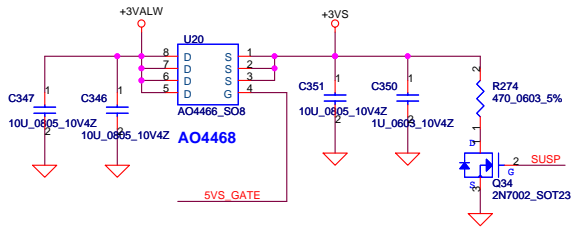


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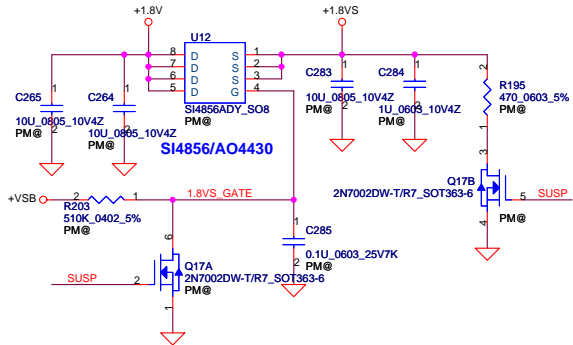
+5VALW TO +5VS



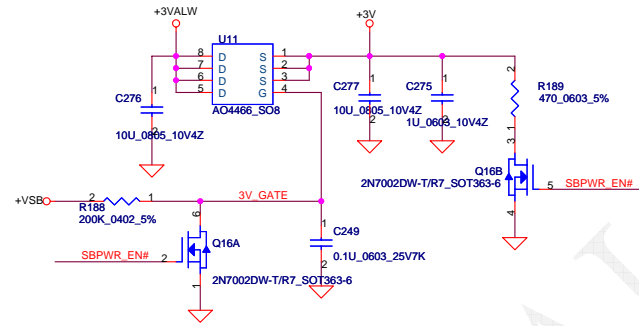
+3VALW TO +3VS



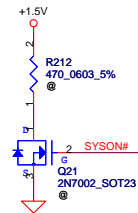
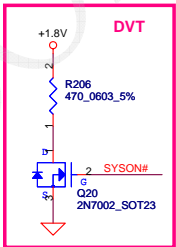
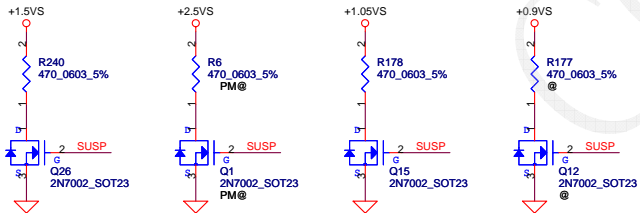
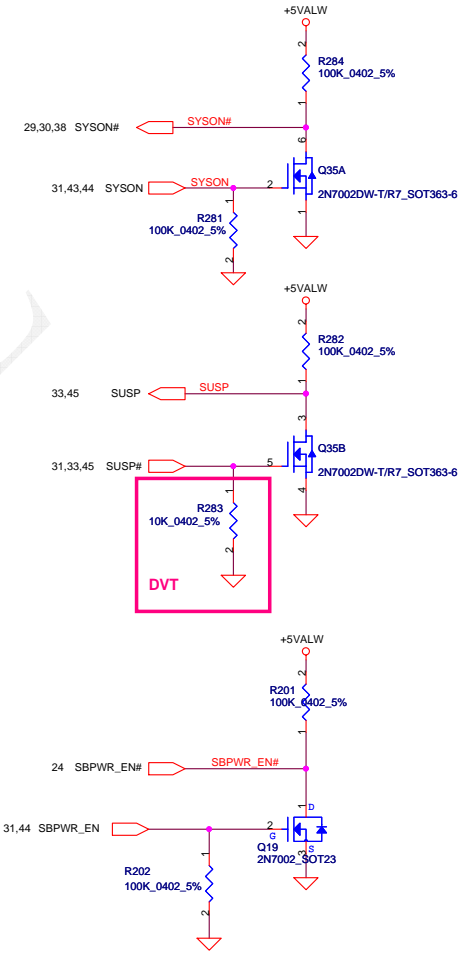
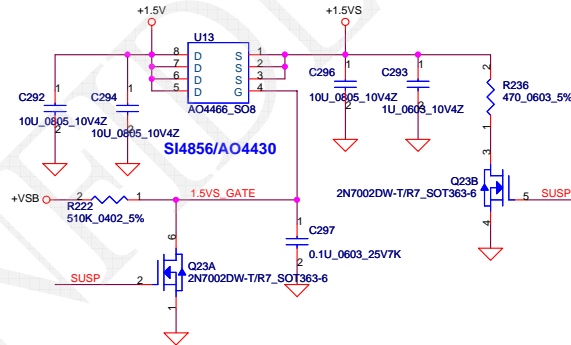
+1.8V to +1.8VS



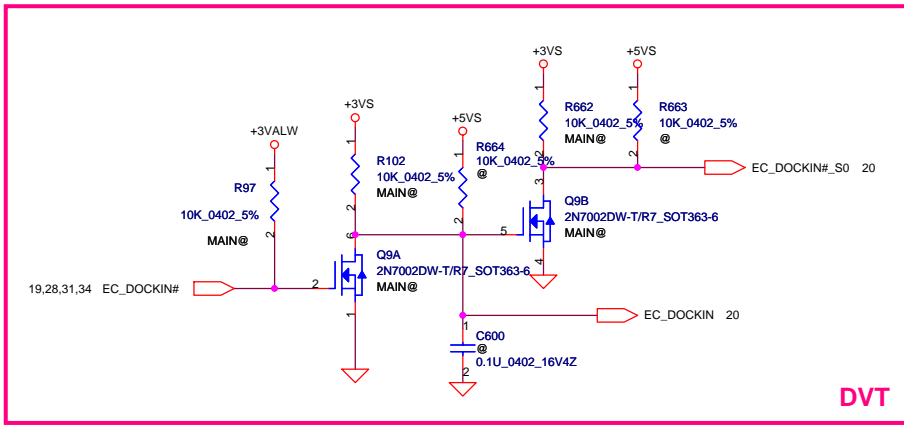
+3VALW TO +3V(ICH9M AUX Power)



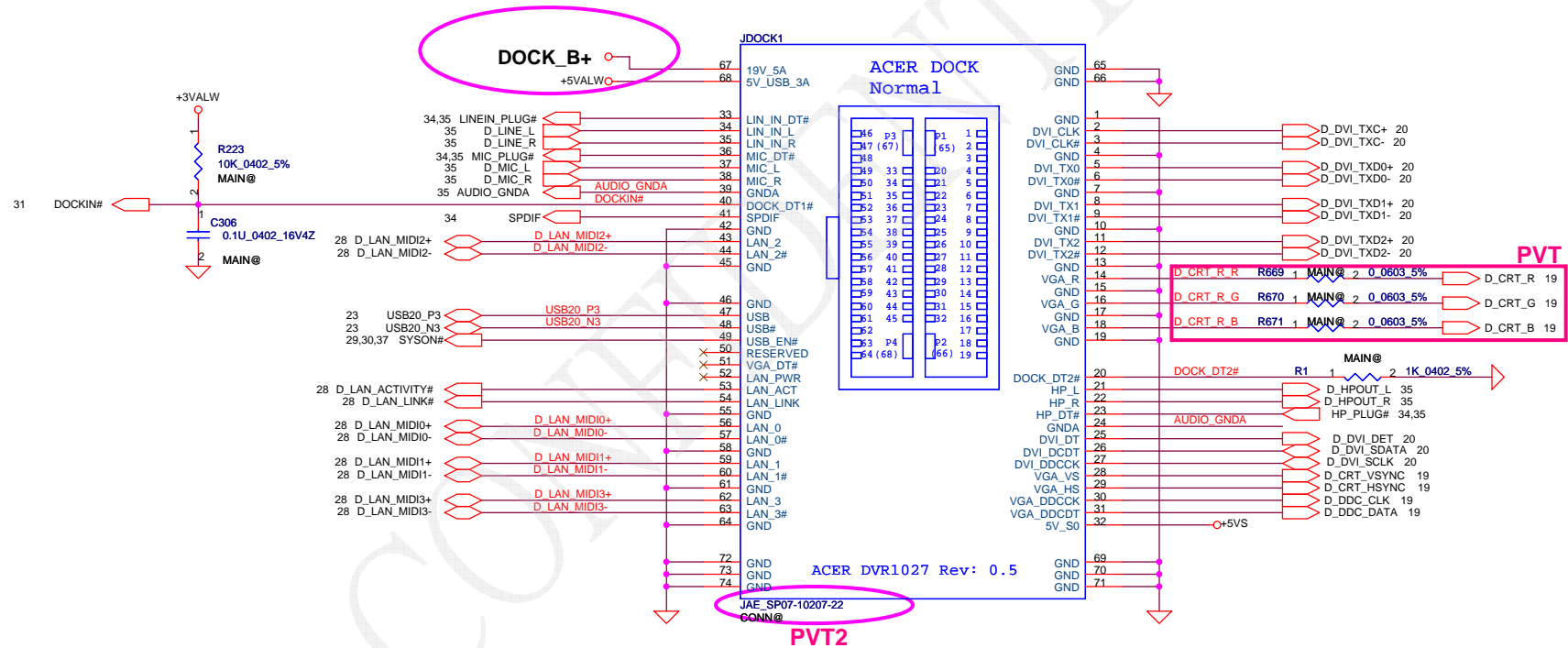
+1.5V to +1.5VS



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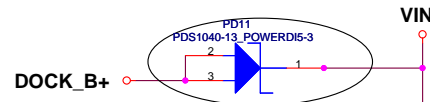


10/15 Acer DVR 1028 Rev0.3

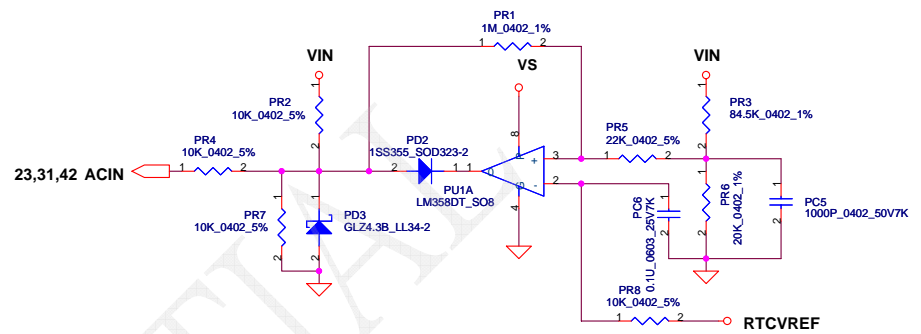
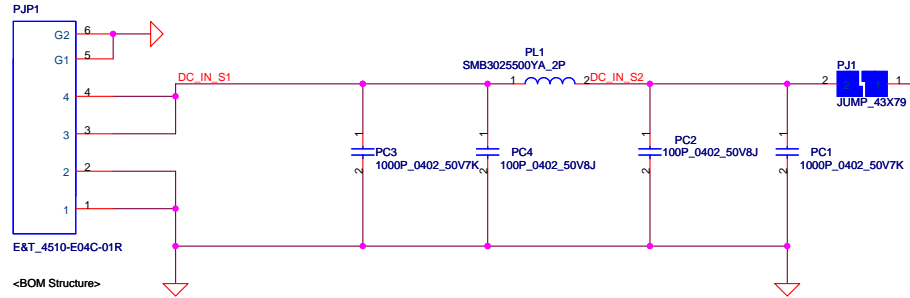


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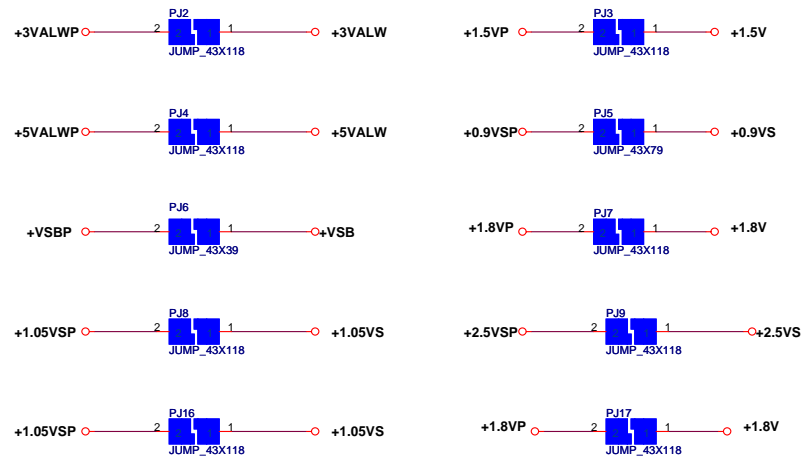
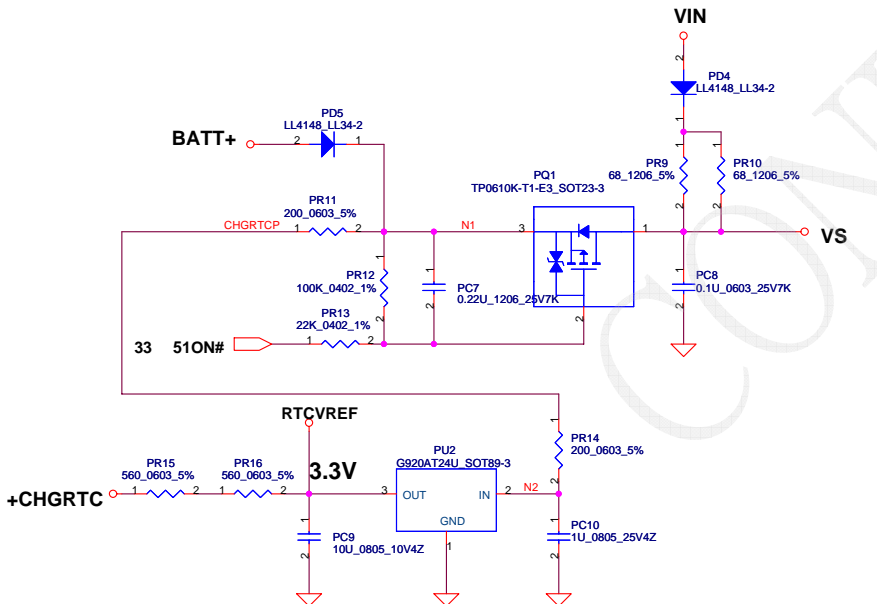
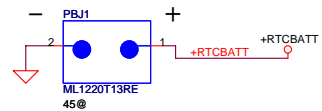
Place at HW side



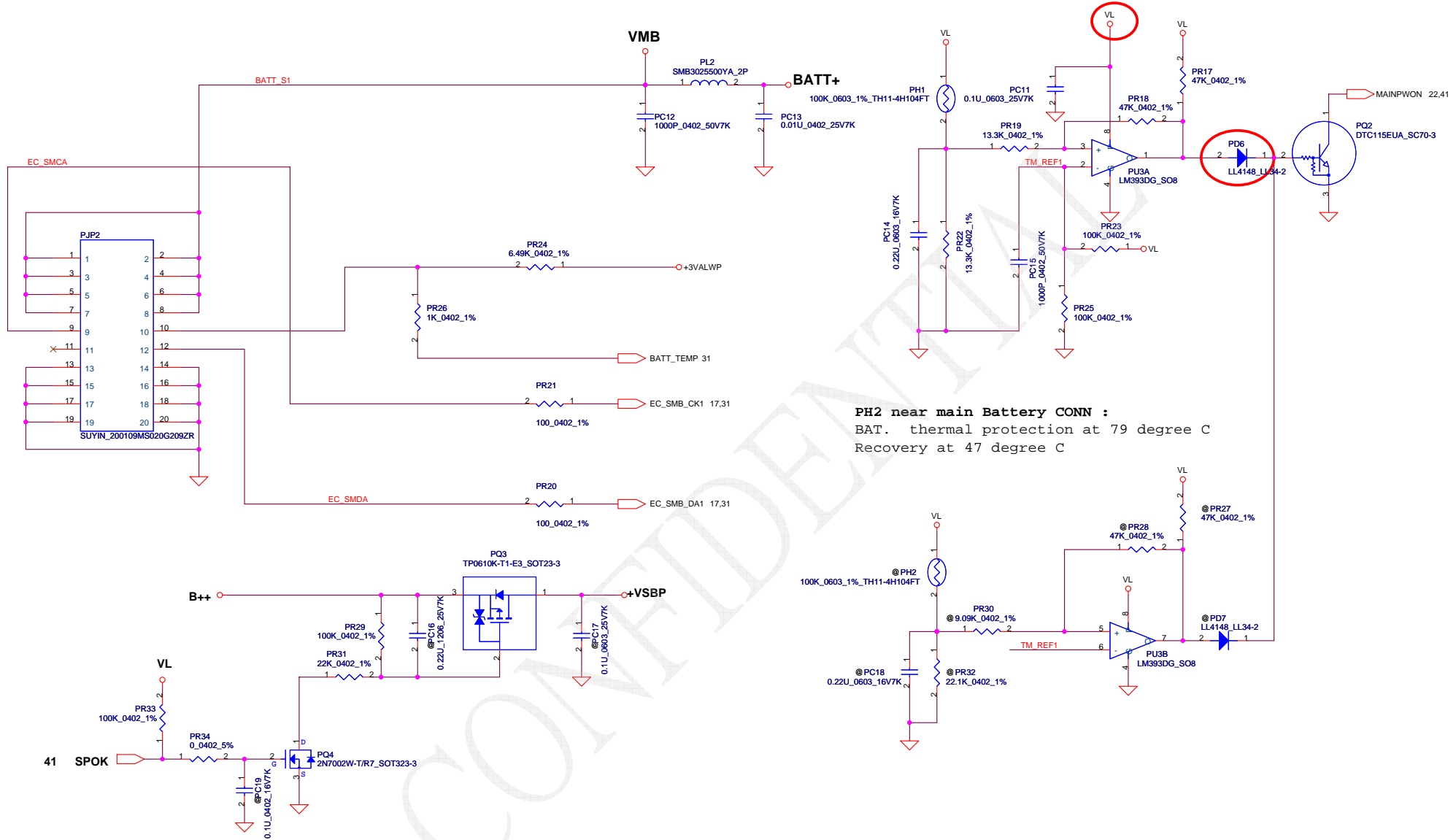
SP02000EF00



Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

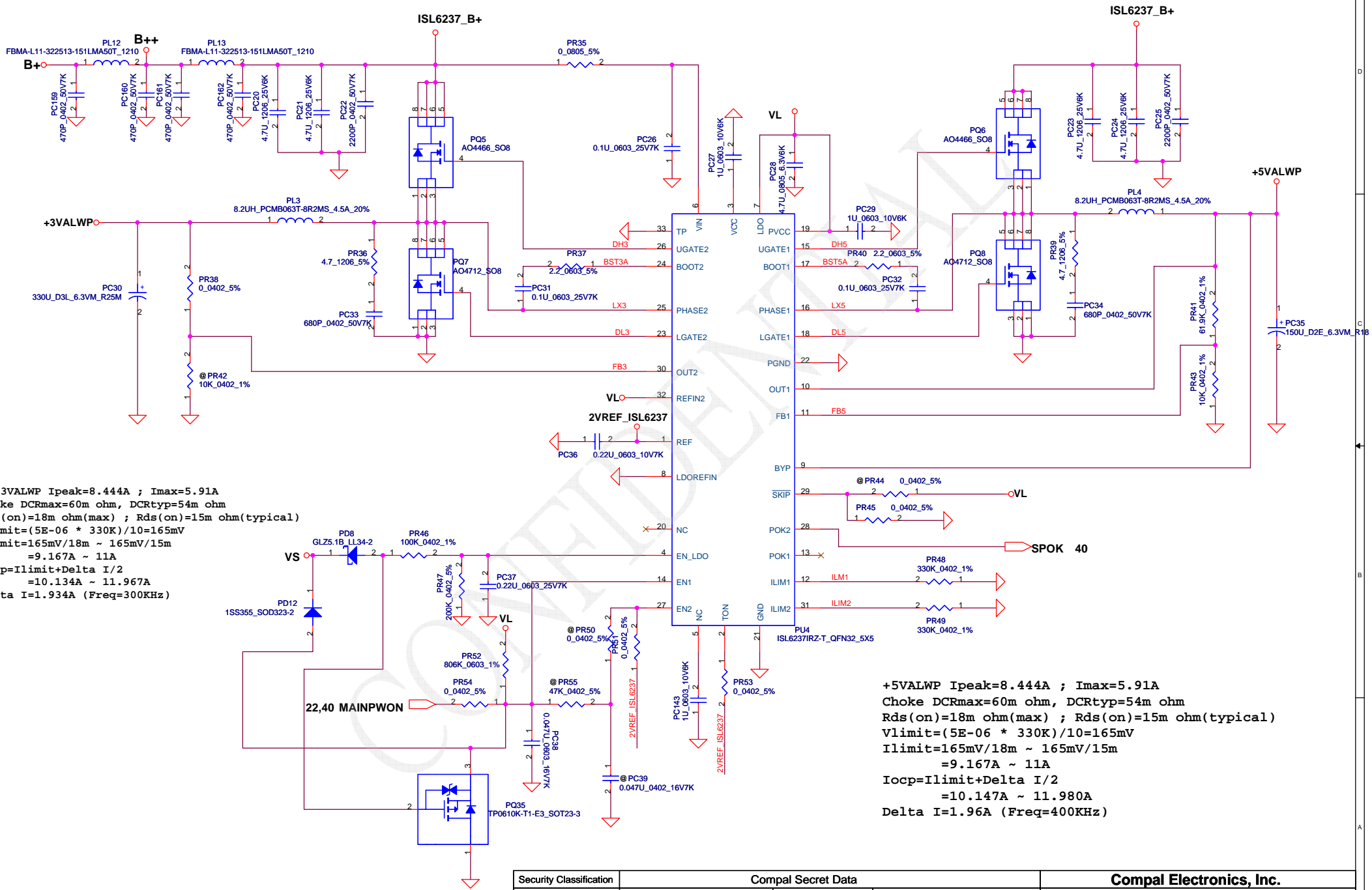


PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C

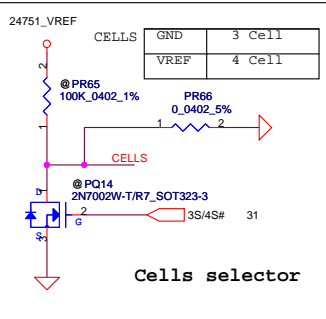
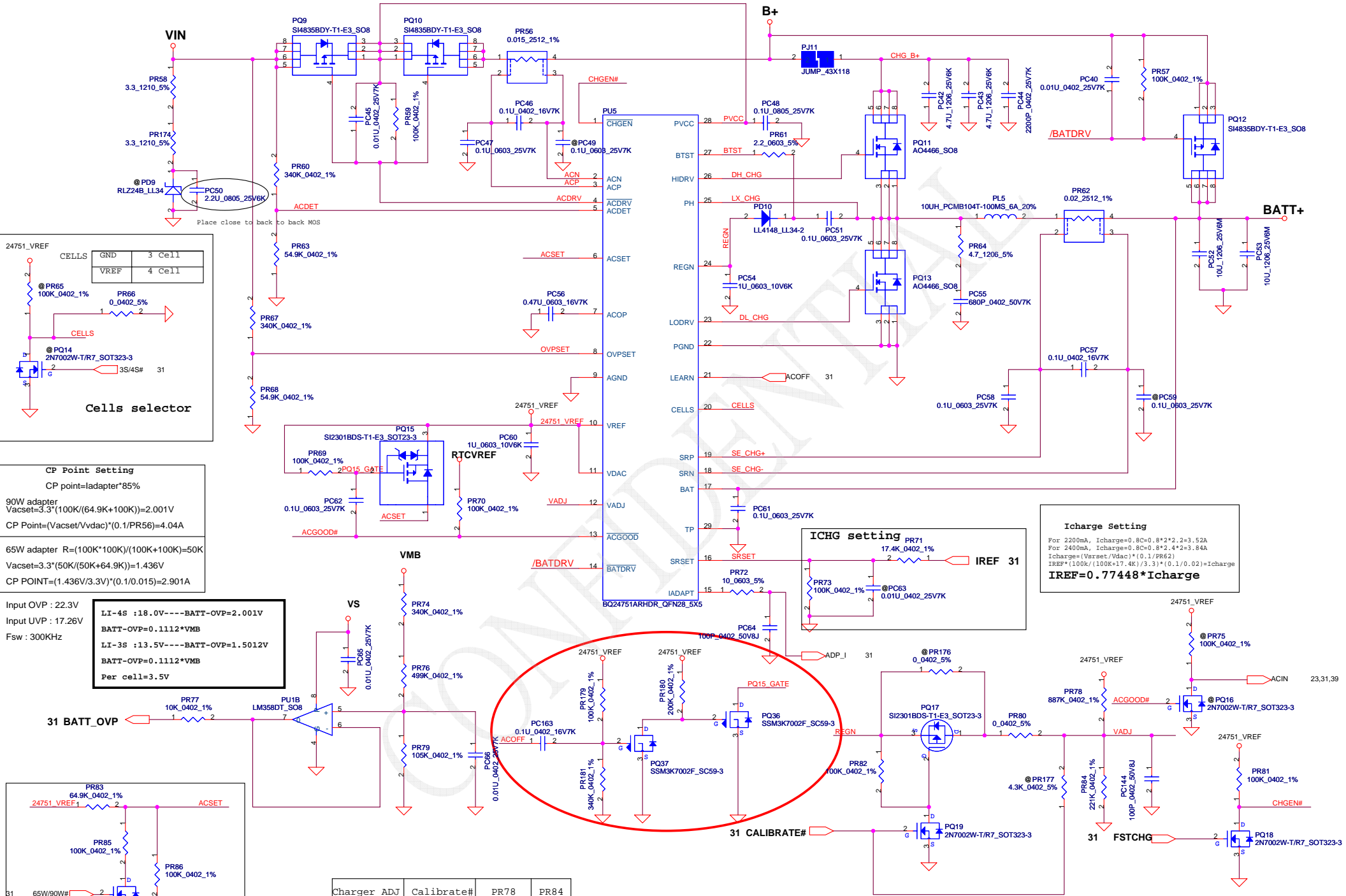
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 10.134A \sim 11.967A$
 $\Delta I = 1.934A$ (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 10.147A \sim 11.980A$
 $\Delta I = 1.96A$ (Freq=400KHz)

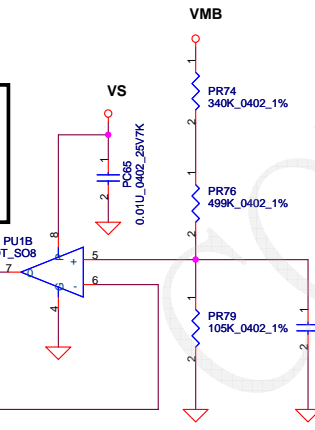
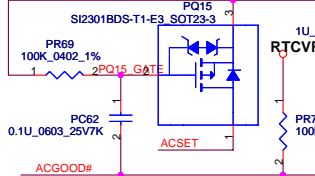
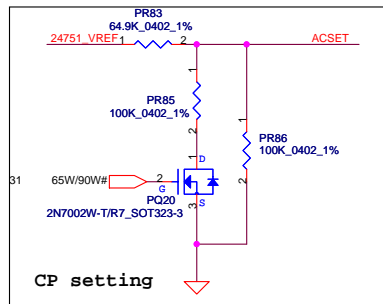
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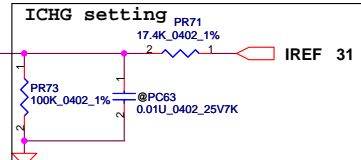
CP Point Setting
 CP point=ladapter*85%
 90W adapter
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$
 $CP\ Point = (V_{acset} / V_{vdac}) \cdot (0.1 / PR56) = 4.04A$
 65W adapter $R = (100K \cdot 100K) / (100K + 100K) = 50K$
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$
 $CP\ POINT = (1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V --- BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S : 13.5V --- BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=3.5V



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@



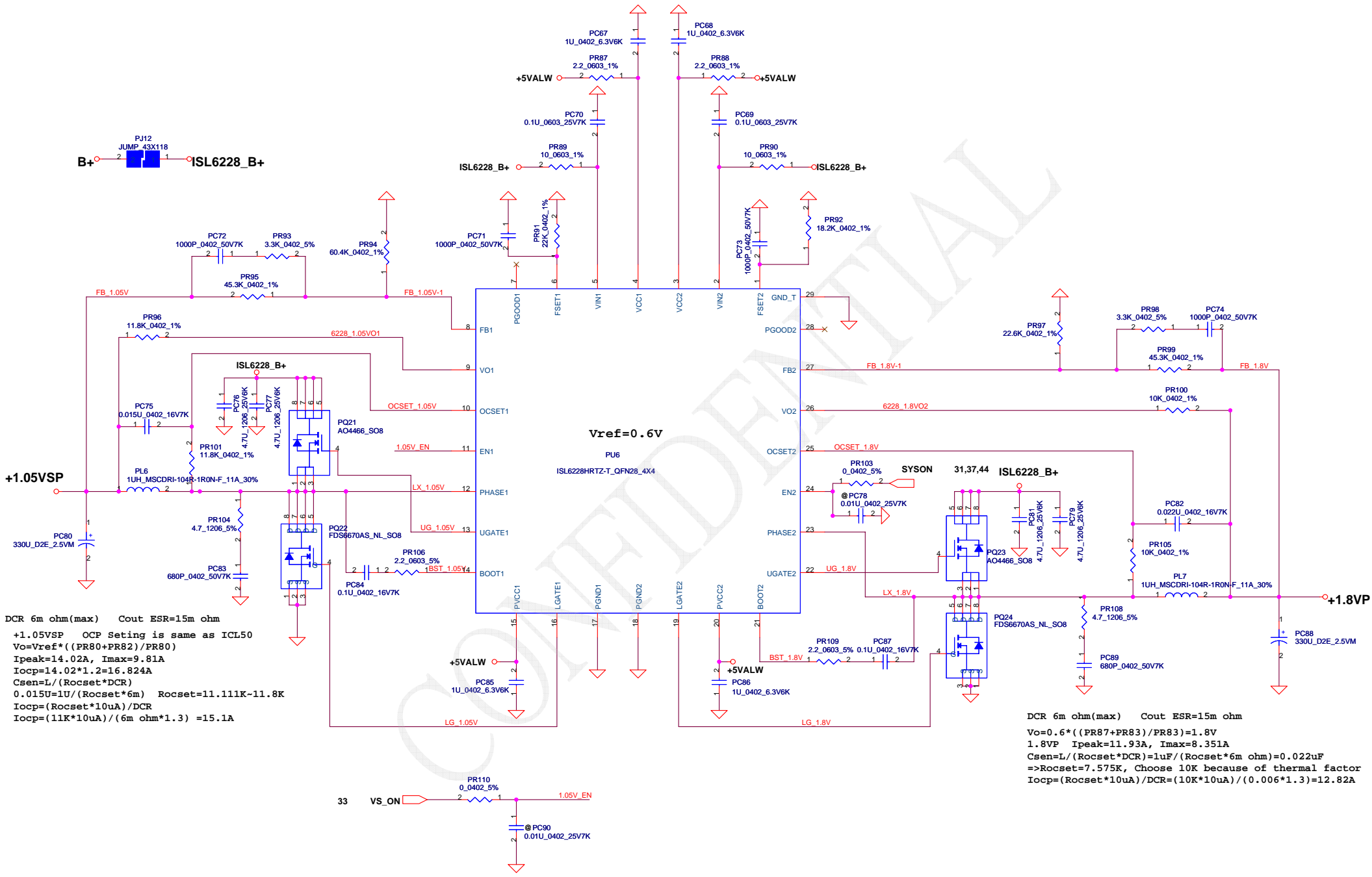
Icharge Setting
 For 2200mA, $I_{charge} = 0.8C = 0.8 \cdot 2.2 = 3.52A$
 For 2400mA, $I_{charge} = 0.8C = 0.8 \cdot 2.4 = 3.84A$
 $I_{charge} = (V_{acset} / V_{dac}) \cdot (0.1 / PR62)$
 $IREF = (100K / (100K + 17.4K)) \cdot (3.3) \cdot (0.1 / 0.02) = I_{charge}$
 $IREF = 0.77448 \cdot I_{charge}$

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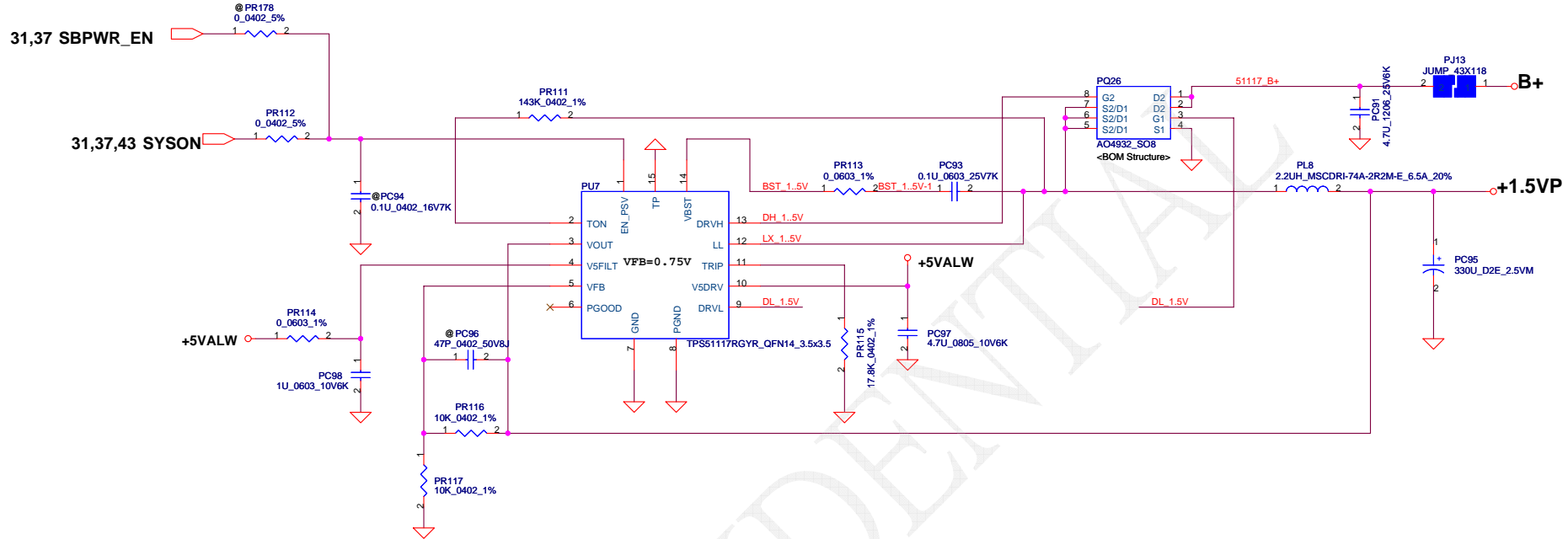
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DCR 6m ohm(max) Cout ESR=15m ohm
 +1.05VSP OCP Setting is same as ICL50
 $V_o = V_{ref} * ((PR80 + PR82) / PR80)$
 $I_{peak} = 14.02A$, $I_{max} = 9.81A$
 $I_{ocp} = 14.02 * 1.2 = 16.824A$
 $C_{sen} = L / (Rocset * DCR)$
 $0.015u = 1u / (Rocset * 6m)$ Rocset=11.111K-11.8K
 $I_{ocp} = (Rocset * 10uA) / DCR$
 $I_{ocp} = (11K * 10uA) / (6m ohm * 1.3) = 15.1A$

DCR 6m ohm(max) Cout ESR=15m ohm
 $V_o = 0.6 * ((PR7 + PR83) / PR83) = 1.8V$
 $1.8VP$ $I_{peak} = 11.93A$, $I_{max} = 8.351A$
 $C_{sen} = L / (Rocset * DCR) = 1uF / (Rocset * 6m ohm) = 0.022uF$
 $\Rightarrow Rocset = 7.575K$, Choose 10K because of thermal factor
 $I_{ocp} = (Rocset * 10uA) / DCR = (10K * 10uA) / (0.006 * 1.3) = 12.82A$

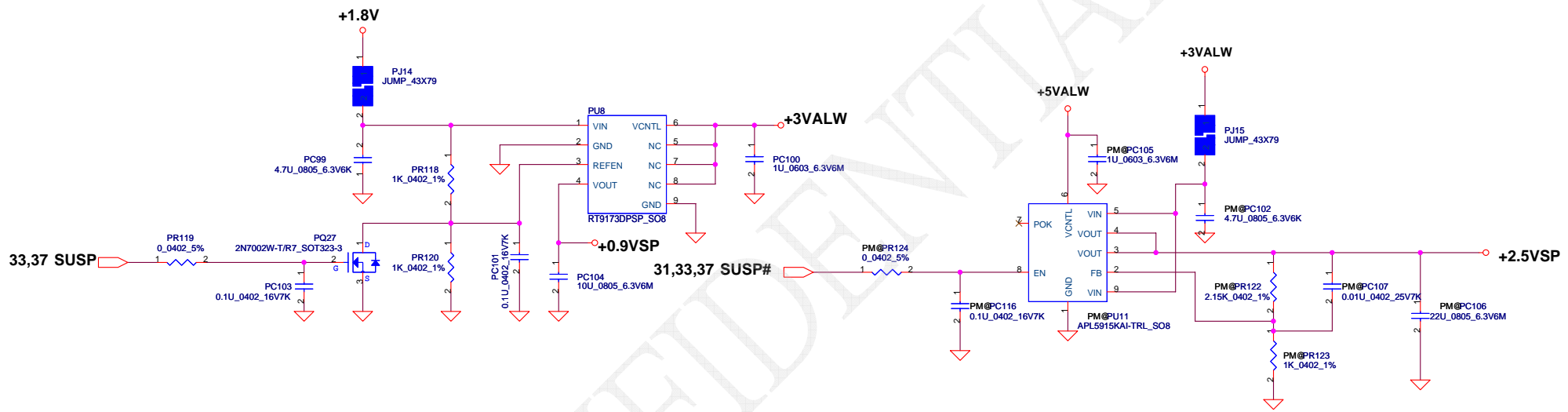
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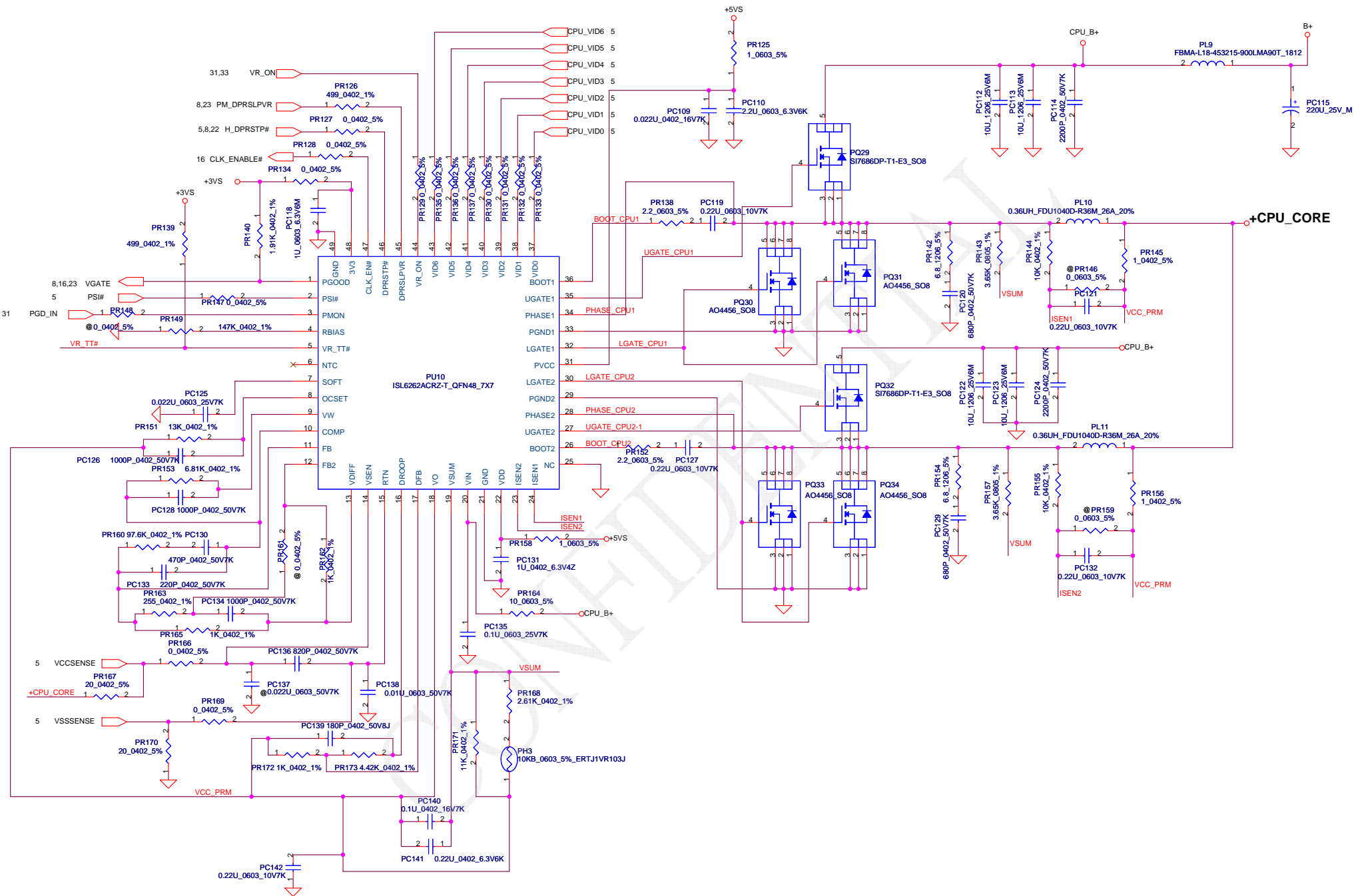
VFB=0.75V
 $V_o = VFB * (1 + PR87 / PR88) = 0.75 * (1 + 10K / 10K) = 1.5V$
 $Ton = 19 * e^{-12} * 143000 * ((2/3) * V_o + 100mV) / 19 + 50ns$
 $= 2.645e-7 \text{ us}$
 $=> V_o / V_{in} = D = Ton / T_s \Rightarrow T_s = 3.35us$
 $Fsw = 298KHz$

Cout ESR=15m ohm
 $I_{peak} = 4.71A, I_{max} = 3.297A, I_{ocp} = 5.652A$
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Fsw) = 2.107A$
 $=> 1/2 \Delta I = 1.053A$
 $V_{trip} = R_{trip} * I_{ocp} = 17.8K * 10uA = 0.178V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.053A$
 $= 0.178 / (0.027 * 1.2) + 1.053 = 5.493A + 1.053A = 6.546A$
 $I_{ocpmax} = (0.178 / (0.021 * 1.1)) + 1.053A = 7.705A + 1.053A$
 $= 8.758A$
 $I_{ocp} = 6.546A - 8.758A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Delete PD1.	Because we can cost down and DOCK_B+ has another one.	0.1	39	1 Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071108	EVT
2	3/5V exit on battery mode shutdown.	To prevent 3/5V exit on battery mode shutdown.	0.2	41	Add SC100001K00 (S DIO 1SS355 SOD323 T/R-5K	20071221	DVT
3	PD11 has over temp. issue.	Because PD11 has over temperature issue in JAQ60, we change it to a 10A diode.	0.2	39	Change PD11 from SCSB540C080 to SCS00002F00 .	20071221	DVT
4	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PR36 and PR39 to SD001470B80	20071221	DVT
5	Down size.	Down size. by sourcer request.	0.2	46	Change PC136 from SE025821K80 to SE000003W00	20071221	DVT
6	Down size.	Down size. by sourcer request.	0.2	46	Change PC120 and PC129 from SE024681J80 to SE074681K80	20071221	DVT
7	Down size.	Down size. by sourcer request.	0.2	43	Change PC72 and PC74 from SE068102J80 to SE074102K80	20071221	DVT
8	2nd source trial run TI controller.	2nd source trial run TI controller.	0.2	41	Add PC143 SE080105K80	20071221	DVT
9	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PC33 and PC34 SE074681K80	20071221	DVT
10	To meet Jeta SPEC.	To meet Jeta SPEC.	0.2	42	Add PC144 SE074102K80	20071221	DVT
12	Add EMI solution.	Add 3/5V boost resistor.	0.3	41	Add PR37, PR40 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
13	Add EMI solution.	Add charger boost resistor.	0.3	42	Add PR61 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
14	Add EMI solution.	Add charger snubber.	0.3	42	Add PR64 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC55 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
15	Add EMI solution.	Add 1.05V/1.8V boost resistor.	0.3	43	Add PR106, PR109 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
16	Add EMI solution.	Add 1.05V snubber.	0.3	43	Add PR104 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC83 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
17	Add EMI solution.	Add 1.8V snubber.	0.3	43	Add PR108 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC89 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
18	Add EMI solution.	Add CPU boost resistor.	0.3	46	Add PR138, PR152 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
19	Add EMI solution.	Add 3/5V input capacitor filter..	0.3	41	Add PC159, PC160, PC161, PC162 SE074471K80(S CER CAP 470P 50V K X7R 0402)	20080102	DVT
20	Add EMI solution.	Add 3/5V input beat	0.3	41	Add PL12, PL13 SM010016410(S SUPPRE KC FBMA-L11-322513-151LMA50T)	20080102	DVT
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.4	Change R25 , R18 , R11 , R19 from 56 to 54.9 ohm	Reference standard circuit
	P.4	Delete R10	Foe ESD
	P.4	Change CPU temp sensor U9 , R55 / R56 from 100 to 0 ohm , delete R64 / R652	ADI had issue , for SMSC / Fintek temp sensor , no used for OD output
	P.8	Change R525 , R527 connected from +1.05Vs to GND	Reference standard circuit
		Change Cantiga GM U30 as SA00001P930 (Ver:B0)	Revision upgrade
		Change Cantiga PM U30 as SA00001Z030 (Ver:B0)	
	P.12	Change L42 , L18 , C499 , C229 , C280 , C232 as GM@	Reference standard circuit
	P.12	Change R596 , R597 as PM@	For UMA CRT
	P.12	Add C597 (220U)	Reserved
	P.12	Add C597 (220U)	Reference standard circuit
	P.12	Change R110 , C187 , C196 as stuff , R117 un-stuff	DFX
	P.12	C461 down size as 10U_0603	NA
	P.16	Change Q30 (dual N-MOS) as Q48 , Q49 (2 single N-MOS)	NA
	P.17	C500 down size as 680P_0402	For BOM
	P.17	Add L57 , L58 , C598 , C599 for +1V8RUN	+1V8RUN ripple (+1V8RUN is for MXM +PEX1V2)
	P.17	Add R599 as 0ohm	Reserve R598 , D31
	P.17	Update JMXM1 footprint	NA
	P.17	Change Q41 (dual N-MOS) as Q50 , Q51 (2 single N-MOS)	NA
	P.18	C364 down size as 680P_0402	For BOM
	P.18	C365 , C366 , C367 change from 220P to 820P	For EMI
	P.19	D5 change as RB411DT146_SOT23-3	Common part
	P.19	Change Q40 (dual N-MOS) as Q52 , Q53 (2 single N-MOS)	NA
	P.19	Change C401 , C409 , C419 as 15P	For DISCRETE CRT
	P.19	Change C402 , C410 , C420 as 12P	For DISCRETE CRT
	P.19	C408 , C418 , C423 (22P) stuff for UMA only	For UMA CRT only
	P.19	Change L1 , L2 from FCM1608C-121T_0603 as 10ohm_0603	For CRT
	P.20	Change Q7 from 2N7002_SOT23(Dual N-MOS) as Q7 & Q47(Single BSH111 N-MOS)	For DVI SMBUS level shifter
	P.20	Add R600 & R602 (4.7K ohm) pull high +3Vs	For DVI SMBUS
	P.20	Reserve R601 & R603 (2.7K ohm) pull high +5Vs	For DVI SMBUS
	P.20	Reserve U39 & U40 (SN74CBTD3306CPWR_TSSOP8)	For DVI & HDMI SMBUS
	P.20	Change D21 from RB751V_SOD323 as CH751H-40PT_SOD323-2	NA
	P.22	Change R478 from 33 ohm as 1K ohm	Customer request
	P.22	LAN_RST# connect to GND	No used Integrated LAN
	P.22	R169 un-stuff	For mobile
	P.22	Add CR_CPPE#(GPIO7) & CR_WAKE#(GPIO22)	For JMB385 power management
	P.22	Swap PCIE(x1) port 2 & port 4	NA
	P.22	R385 un-stuff , U28 stuff	For sequence
	P.25	U34.127 is used as external IDSEL	NA
	P.25	R489 un-stuff	For PCMCIA Lan card not support PM_CLKRUN# function
	P.25	Update JPCM1 footprint	For DFX
	P.26	Reserve R655 , R656 , D33 for CR_CPPE# & CR_WAKE#	For JMB385 power management
	P.26	Cantiga JMB385 U32 as SA00001W910 (Ver:B)	Revision upgrade
	P.27	Delete BCM5787M co-lay schematic	NA
	P.27	Update U25 footprint	For DFX
	P.28	Change T1 from GSL5009 as GSL5009-1(SP050003T10)	NA
	P.28	Add C375 , C383 (68P)	For EMI
	P.29	Add R658	Add 80 port function on JMINI2
	P.30	D32(SC300000B00) stuff	For ESD
	P.31	Add R604	NA
	P.31	R248 change from 0 ohm as 8.2K ohm	Foe Board ID as 1 define


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PHASE	PAGE	MODIFICATION LIST	PURPOSE	
DVT	P.31	C286 change from 3.3U as 4.7U	Stable KB926 internal +1.8V regulator , ENE suggestion value	
	P.32	JP6 pin define reverse	NA	
	P.32	Change SW3 & SW4 type	NA	
	P.32	U15 change from 1MB as 2MB capacity SPI ROM	Add Finger print code	
	P.33	R261 change from 10K as 31.6K	Fix ATI MXM sku can't power on for battery mode issue	
	P.33	C334 change from 0.1U as 1U	Fix nVIDIA MXM sku power on issue	
	P.34	Delete Internal(Digital) MIC reserved circuit	NA	
	P.34	Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI	
	P.34	Add R660 to connect HDA_GPIO3 with DOCKIN#	For docking spdif feature enable	
	P.34	Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI	
	P.35	R559 / R560 change from 47 ohm as 75 ohm	For Audio precision FSOV	
	P.35	R561 / R562 / R566 / R571 change from 75 ohm as 1K ohm	For ESD , Realtek suggestion value	
	P.36	Add C601 , C602 , C603 (330P) on +5VALW	For EMI	
	P.37	R283 change from 100K to 10K	NA	
	P.37	R206 , Q20 stuff	For +1.8V discharge	
	P.38	Add switch to enable/disable EC_DOCKIN#_S0 for HDMI SMBUS	NA	
	P.38	Update JDock1 footprint	NA	
	PVT1	P.16	Change C308 / C311 (33P) as 27P	For RTC accuracy
P.23		Use 4MB SPI ROM	For Kinabalu_High & Kinabalu_Low	
P.23		Add test point T32 / T33 / T34 / T35	Reserved for PCIE(X1) port 1	
P.25		Change U35 as SA000026P10(OZ2210GN-B1)	For B1 version	
P.27		Change U23 as SA000025P20(BCM5764MKMLG P20)	For B0 version	
P.27		Reserved R673 , R674 (0 ohm)	For Lan SMBUS	
P.27		Reserved Lan GPIO0(LAN_ALERT#) / LAN_ALERT#_EC / R675 , R676 , R677 to EC	For Lan ASF workaround	
P.27		U23 Pin17 / Pin5 / Pin55 connect to U23 Pin18 for power +Lan_VDDIO_1.2	U23 Pin18 is power source +Lan_VDDIO_1.2 for U23 Pin17 / Pin5 / Pin55	
P.27		U23 Pin38 / Pin52 NC	NA	
P.29		Change JMINI1 for Robson2 , chnagne JMINI2 for Wireless	NA	
P.31		Add LAN_ALERT#_EC & EC_ACIN for EC	Reserved for ASF workkrund & Nvidia MXM power saving	
P.33		Add R668(10K) & reserved R263(10K)	Fine tune +1.05VS timing for UMA boot display flash	
P.34		Change U36 as ALC268-VB1-GR(SA00001GD10)	Version upgrade	
P.34		Stuff R659 & un-stuff R660	For SPDIF feature on docking	
P.36		Add C604 , C605 (820P_0402)	For EMI	
P.50		Chipset change as GM(SA00002JT10) / PM(SA00002JJ00) / ICH9M(SA00002JH00)	Version upgrade	
PVT2		P.27	Update U23 CIS symbol	U23 Pin38 , 52 can't be changed as NC
		P.34	Add D34 , R678	For ACER docking SPDIF feature (No SPDIF on board)
	P.38	Update JDock1 CIS symbol	Docking connector modify (add boss x 2) for DFX	
	P.35	Delete D2 , D4 (Int SPK ESD diode)	NA	
	P.34	Delete D9 (Int MIC ESD diode)	NA	
	P.35	Add C609 , C610 (330P_0603) on Right SPK	For EMI	
	P.34	Add C608 (330P_0603) on Int MIC	For EMI	
	P.08	Add Test point (T39 , T40 , T41 , T42)	Add Management Engine JTAG pins	
	P.27	Add C612 , C614 (0.1u_0402) for +LAN_AVDD	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV	
	P.27	Add C615 , C616 , C617 (0.1u_0402) for +LAN_AVDDL	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV	
	P.08	Add U41, R679 , R680 , R681 , R682 , R683 , R684 , R685 , T43	Reserved for Management Engine JTAG debug	
	P.07	Chipset change as GM(SA00002JT50) / PM(SA00002JJ50)	Version upgrade	
	P.20 , P.31	Add EC_DVI_DET , EC_GPIOB , EC_GPIOC , R687 , R688 , R691	Reserved for DVI detect delay control (by EC)	
	MP	P.24	R73 , R148 change from 10_0402 to 100_0402 C128 , C204 change from 0.1U_0402 to 1U_0402	For USB issue on ICH9M A3 stepping
		P.34 , P.35	C608 , C609 , C610 change from 330P_0603 to 330P_0402	For 330P_0402 is standard part
		P.31	Change R248 as 33K	Board ID upgrade
		P.30	Add R692 / R693 (0_0603)	Reserved S3 power rail for check finger print sensor S3 resume too slow



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PHASE	PAGE	MODIFICATION LIST	PURPOSE
P.20		Add D35	Reserved for HDMI_HPD
P.30		Add R694 / R695 (0_0603)	Reserved for check
P.27		Delete C612 , C614 , C615 , C616 , C617 (0.1u_0402)	No need
P.16		Stuff R689 / R690	Reserved for LAN power saving
P.35		R559 , R560 change from 75 to 54.9 ohm Chipset change as GM(SA00002JTB0) / PM(SA00002JJA0) / ICH9M(SA00002JH70)	For FSOV between 420mv~480mv Version upgrade
P.32		R291 , R294 change from 300_0402_5% to 150_0402_5%	For ACER Hank's request to fine tune brighter
P.20		R84 , R85 , R86 , R91 change from 2K_0402_5% to 4.7K_0402_5%	For UMA DVI/HDMI monitor P193WA (x) detect issue (On JAL90)

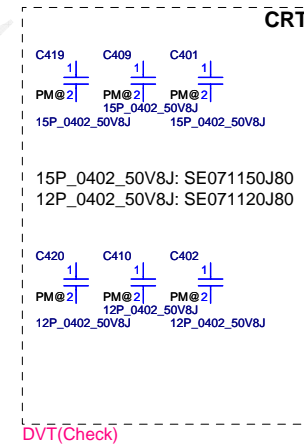
PCB

ZZZ

 LA4221MB Rev0: DA600007R00
 LA4221MB Rev1: DA600007R10
 LA4221MB with Sub/B Rev1: DAZ04800100
 PCB 047 LA-4221P REV1 M/B


IC


U30

 CANTIGA ES_FCBGA1329
 DVT CANTIGA PM: SA00001ZO30 (S IC EB88CTPM QR34 B0 FCBGA 1329 ES)
 PVT CANTIGA PM: SA00002JJ00 (S IC AC88CTPM QT78 B2 FCBGA 1329 PM)
 PVT2 CANTIGA PM: SA00002JJ50 (S IC AC88CTPM QU38 B3 FCBGA 1329 PM)
 Pre-MP CANTIGA PM: SA00002JJA0 (S IC AC82PM45 SLB97 B3 FCBGA1329 PM ABO!)
 U30

 CANTIGA ES_FCBGA1329
 DVT(Check_TBD) CANTIGA GL: SA000023Z00 (S IC CANTIGA ES FCBGA 1329 MCH GL)

For Discrete




DC Cable

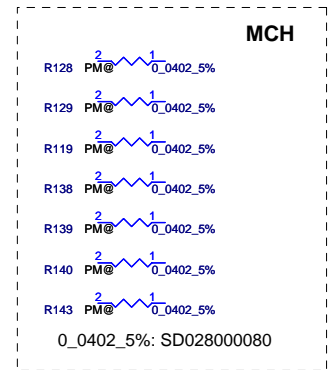
ZZZ

 DC Cable (65W)
 @ PVT(54 Rank)
 DC301003R00(CONN SET 048 DCJACK-MB 2DW-G756-I50 65W)

ZZZ

 DC Cable (90W)
 @ PVT(54 Rank)
 DC301003S00(CONN SET 048 DCJACK-MB 2DW-G756-I49 90W)

U10

 ICH9ME@
 ICH9-M ES_FCBGA676
 ICH9-M: SA00002G120
 (S IC AF82801IEM QT10 A3 PBGA 676P ICH9M)

U6

 SPI2MB@
 W25X16-VSSIG_S08
 MP Winbond: SA00001KN00
 (S IC FL 16MBIT W25X16-VSSIG SOIC 8P)



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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				Date: Friday, May 16, 2008	Sheet 50 of 50