

First International Computer, Inc

Portable Computer Group HW Department

Board name : Mother Board Schematic

Project : LM7R

Version : 0.1

Initial Date : March 1 , 2005

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2. PCI & IRQ & DMA Description :
3. Block Diagram :
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Manager Sign by:

Drawing by : AHARRY_HUANG

Total confirm by: CC_TSAO

LAN Circuit check by:

Audio Circuit check by:

 First International Computer, Inc. 2FL, NO.300, Yang Guang St., Neihu 114 TAIPEI, TAIWAN, R.O.C. (886-2)8751-8751		
Title: LM7R < VIA VN800 + VT8237R >		
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1. Schematic Page Description :

LM7 Schematic Ver : 0.1

- | | | |
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| 17. VN800 (4/4) | 39. DIP Switch & LED | |
| 18. DDR SO-DIMM1 | 40. Firm Ware Hub / LID Switch | |
| 19. DDR SO-DIMM0 | 41. Reset Circuit | |
| 20. VT1631 LVDS Transmitter | 42. OVP / SCREW | |
| 21. LCD Connector | 43. ALC655 Audio Codec | |
| 22. CRT Connector | 44. GMT1420 Audio Amplifier | |

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)
AD23	CardBus

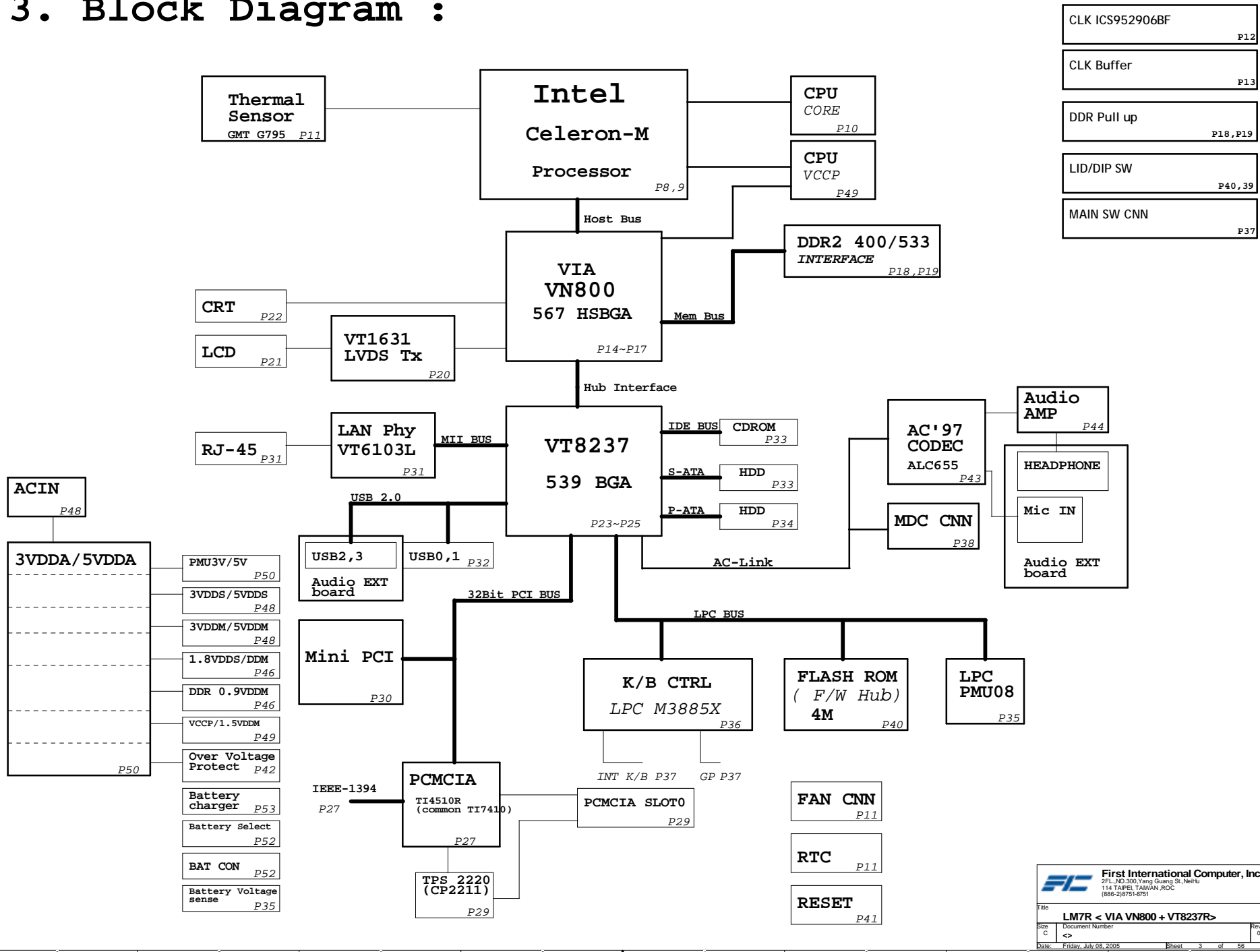
PCIINT	CHIP
IRQA	MiniPCI/NB
IRQB	MiniPCI/CardBus
IRQC	MiniPCI
IRQD	

BUSMASTER	CHIP
REQ0 / GNT0	MiniPCI
REQ1 / GNT1	CardBus
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Description
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Cascade)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	FLOPPY DISK
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSCO
3VDDA	3.3V always on power rail by DCON or PSUSCO
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU

VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR_0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	= Capacitor
CN	= Connector
D	= Diode
F	= Fuse
L	= Inductor
Q	= Transistor
R	= Resistor
RP	= Resistor Pack
U	= Arbitrary Logic Device
Y	= Crystal and Osc

Net Name Suffix







0	= Active Low signal
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Signal Conditioning

D	= Damped (by a resistor)
Q	= Isolated (by a Q-switch)
L	= Filtered (by an inductor or bead)


5.Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Stripline Layer (AGTL, CLOCK, DDR)
Layer 4		Stripline Layer (Analog, LVDS, other)
Layer 5		Ground Plane
Layer 6		Solder Side, Microstrip signal Layer

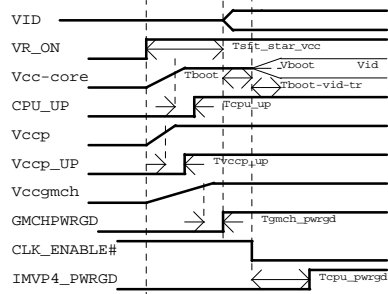
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6.Schematic modify Item and History :

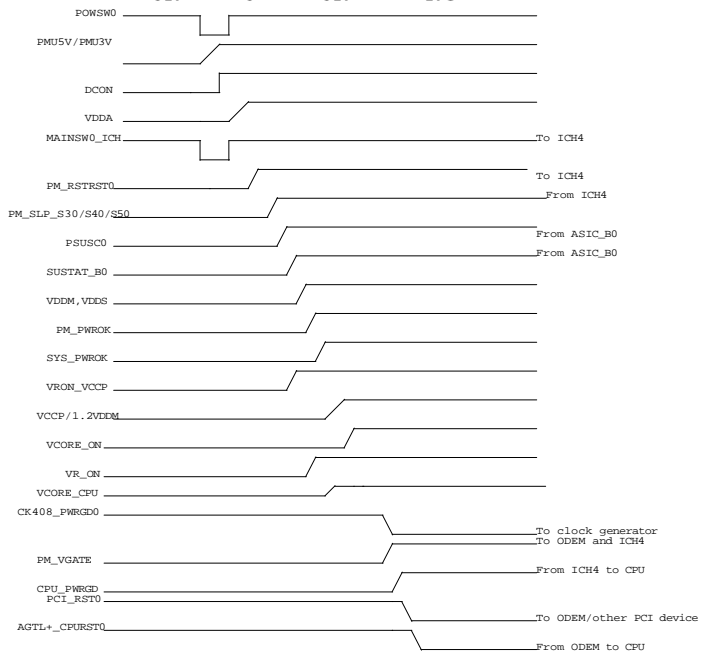
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7. power on & off & S3 Sequence :

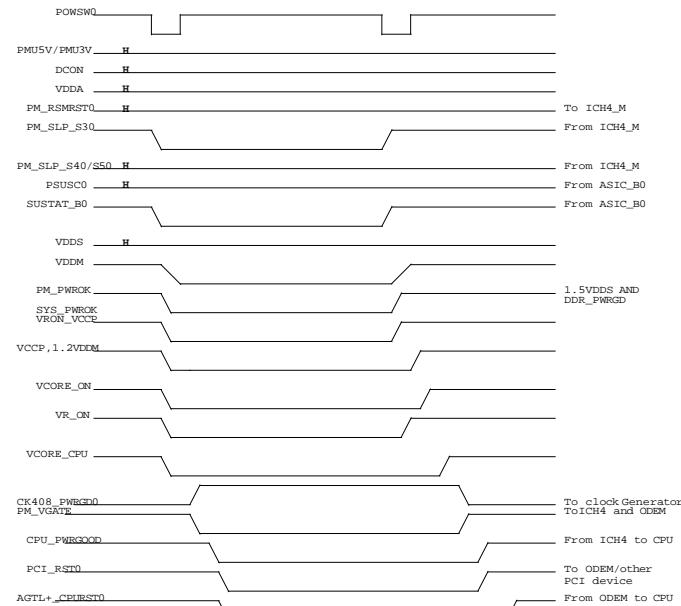
Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



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8. Layout Guideline :

Montara-GM DDR Layout Guidelines

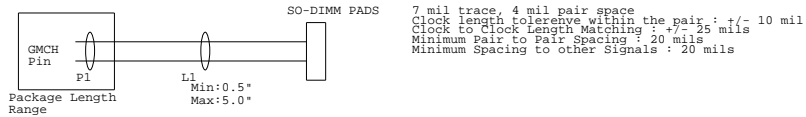
Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

DDR Signal Groups

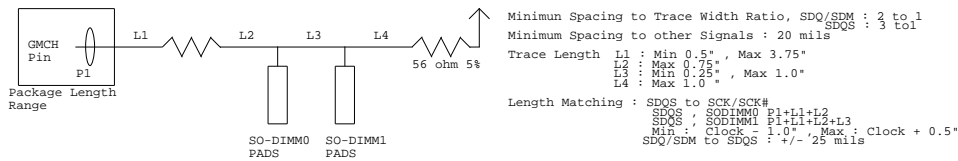
Group	Signal Name	Signal Group	Minimum Length	Maximum Length
Clocks	SCK[5:0]	Control to Clock	Clock - 1.0"	Clock + 0.5"
	SCK#[5:0]	Command to Clock	Clock - 1.0"	Clock + 2.0"
	SDQ[7:0]	CPC to Clock	Clock - 1.0"	Clock + 0.5"
Data	SDQS[8:0]	Strobe to Clock	Clock - 1.0"	Clock + 0.5"
	SDM[8:0]	Data to Strobe	Strobe - 25 mils	Strobe + 25 mils
	SCKE[3:0]			
Command	SMA[12:6,3:0]			
	SBA[1:0]			
	SRAS#			
	SCAS#			
CPC	SMA[5,4,2,1]			
	SMAB[5,4,2,1]			
Feedback	RCVENOUT#			
	RCVENIN#			

Length Matching Formulas

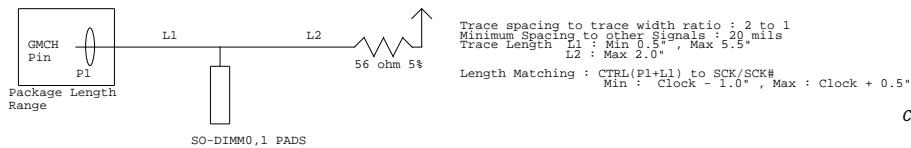
Clock Signals Topologies and Routing Guidelines



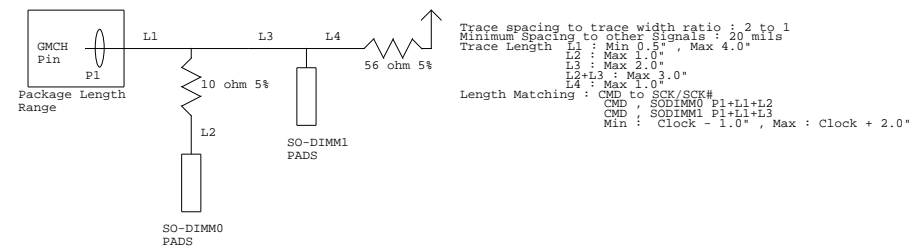
Data Signals Topologies and Routing Guidelines



Control Signals Topologies and Routing Guidelines



Command Signals Topologies and Routing Guidelines

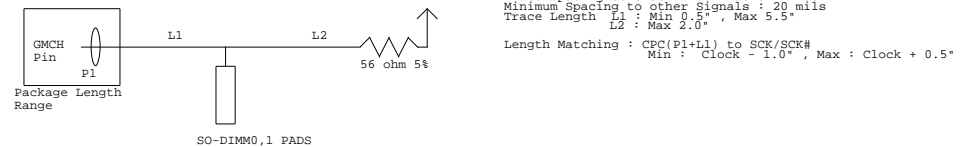


CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" - 8"	5 / 20 mils (5 mil space between + & -)	1. Differentials pairs with the same length (within 10 mil) 2. CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH AGPCLK_ATI	4.5" - 9.0" MAX : 8.5"	5 / 20 mils	* 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5"-9.0"	5 / 20 mils	1. Making PCI length with minimum various 2. Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5"-9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" - 12.5"	5 / 20 mils	

SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

CPC Signals Topologies and Routing Guidelines

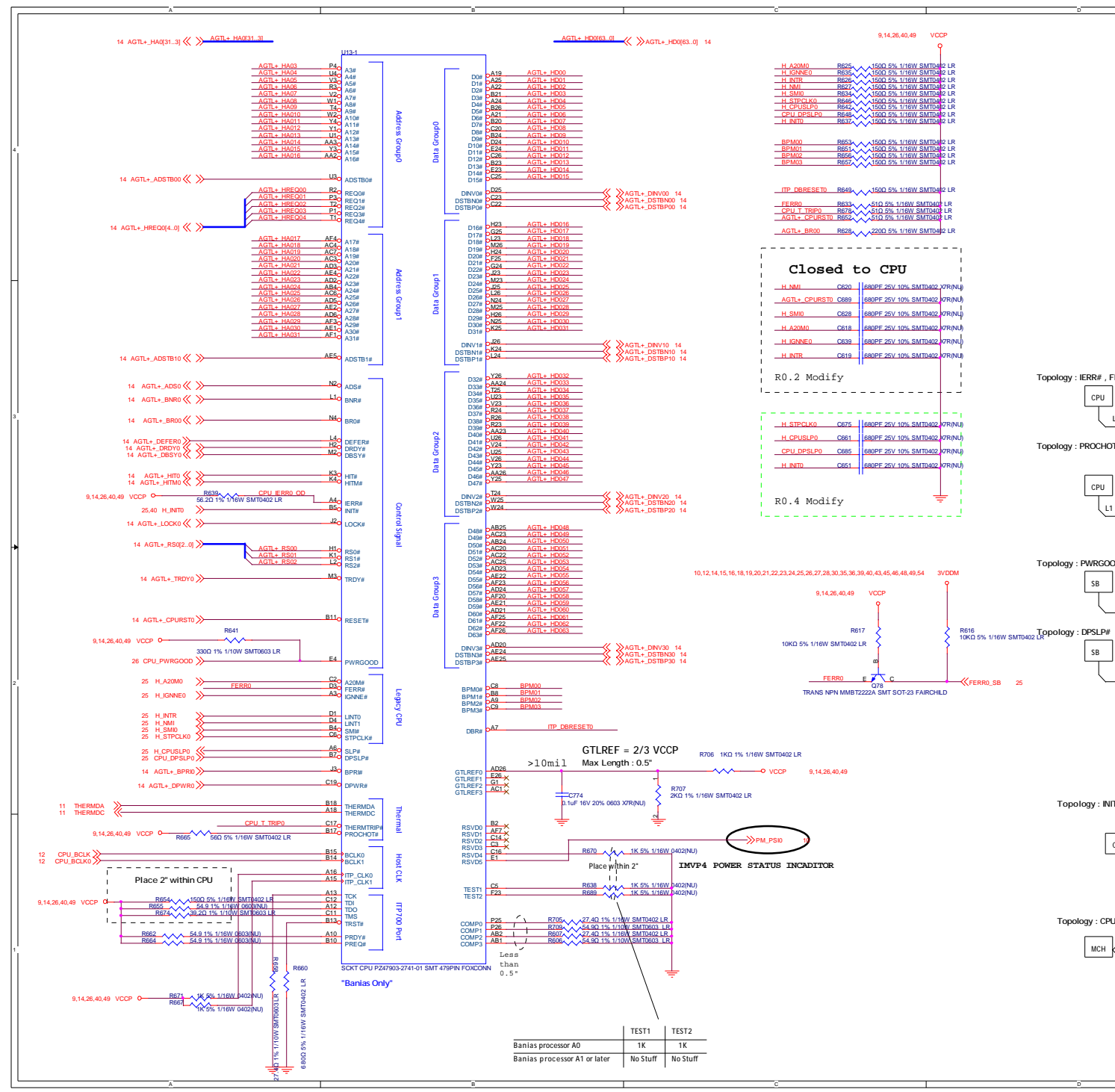


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System Bus Common Clock Signal Layout Guide :

ADS#, BNR#, BPR#, BR#, DBSY#, DEFER#, DPWR#, DRDY#, HIT#, HTM#, LOCK#, RSQ2_0#, TRDY#, RESET#	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 - 6.5 inch	55 +/- 10%	4 & 8(Int. Layer)
Micro-strip(Ext. Layer)			5 & 10(Ext. Layer)

Source Synchronous DATA :

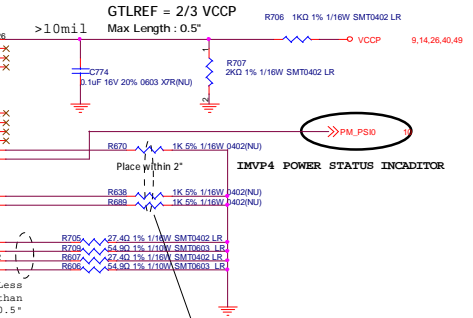
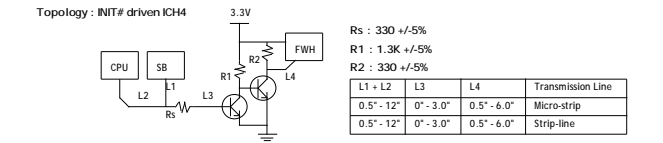
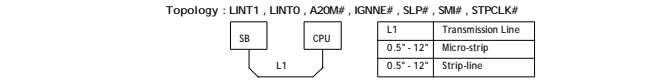
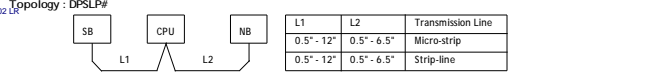
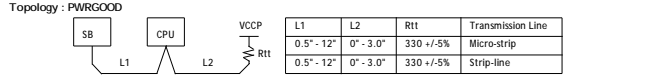
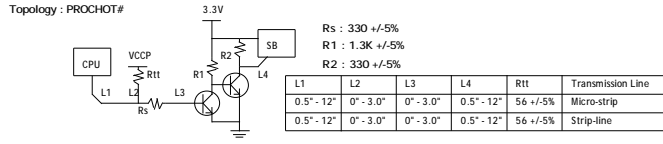
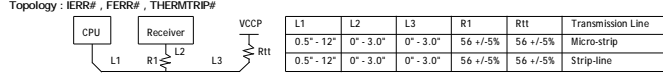
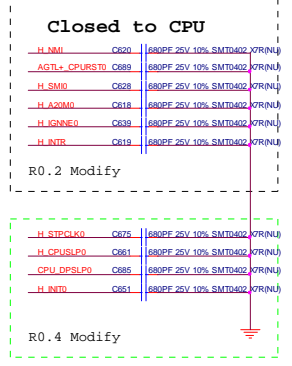
DATA#[63..0], DINW#[3..0], DSTBP#[3..0]	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	1.0 - 5.5 inch	55 +/- 10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
DATA#[15..0], DINVO#	+/- 100 mils	DSTBP0#, DSTBN0#	+/- 25 mils
DATA#[31..16], DINV1#	+/- 100 mils	DSTBP1#, DSTBN1#	+/- 25 mils
DATA#[47..32], DINV2#	+/- 100 mils	DSTBP2#, DSTBN2#	+/- 25 mils
DATA#[63..48], DINV3#	+/- 100 mils	DSTBP3#, DSTBN3#	+/- 25 mils

Source Synchronous ADDRESS :

Address#[31..3], REQ#[4..0], ADSTB#[1..0]	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	1.0 - 6.5 inch	55 +/- 10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
A#[16..3], REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 25 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 25 mils



	TEST1	TEST2
Banias processor A0	1K	1K
Banias processor A1 or later	No Stuff	No Stuff

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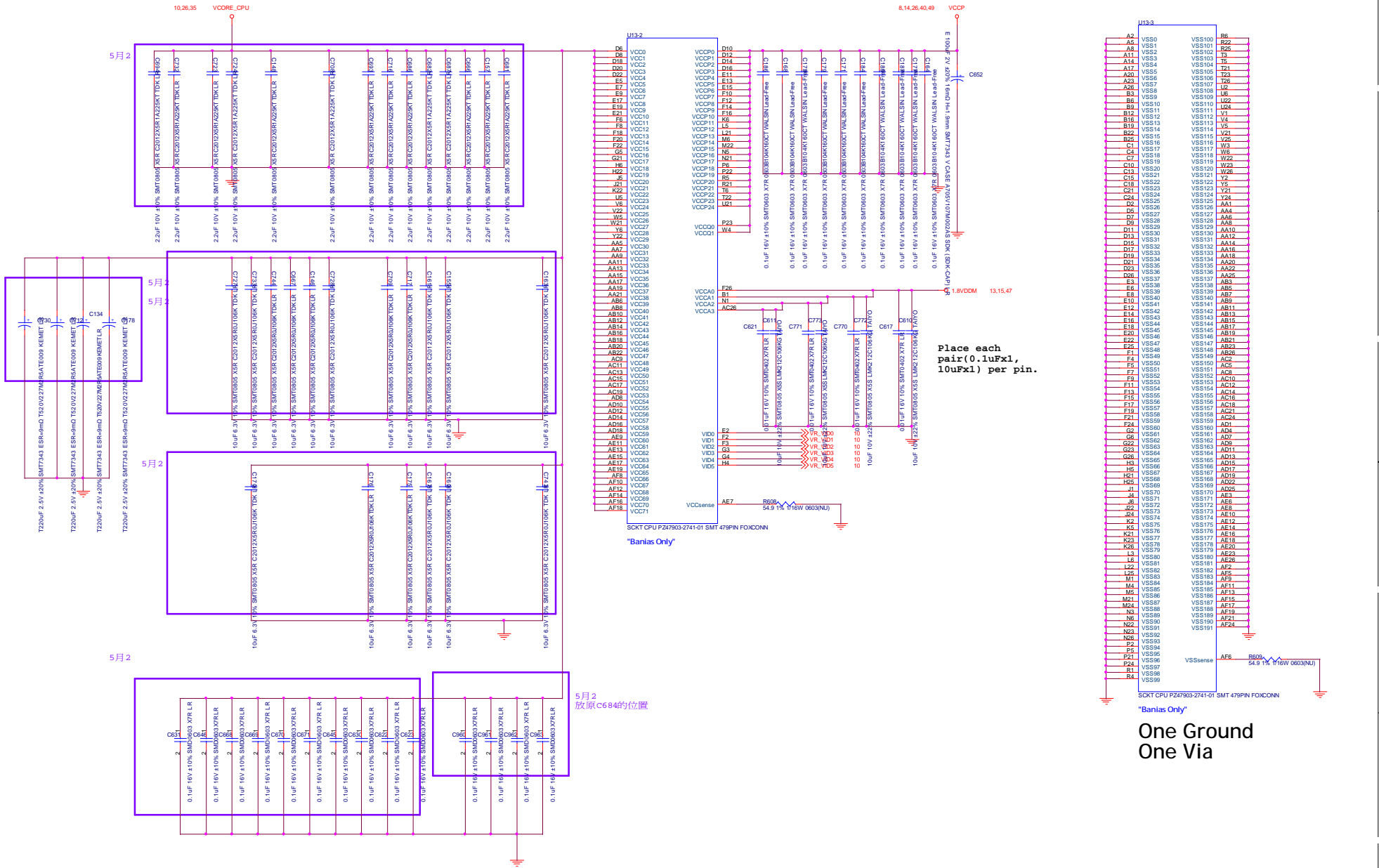
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< CPU I/2 >

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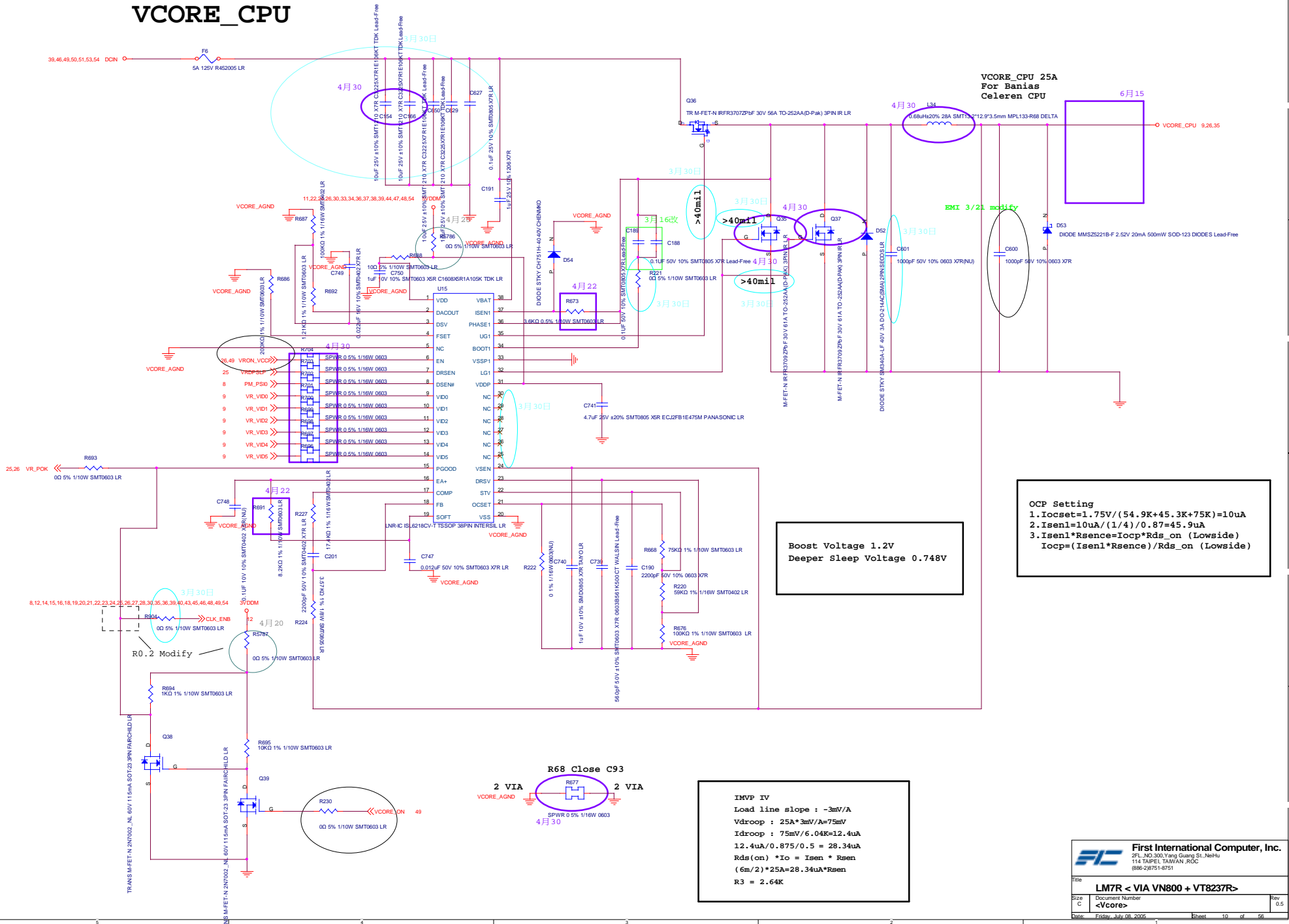


One Ground One Via

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VCORE_CPU

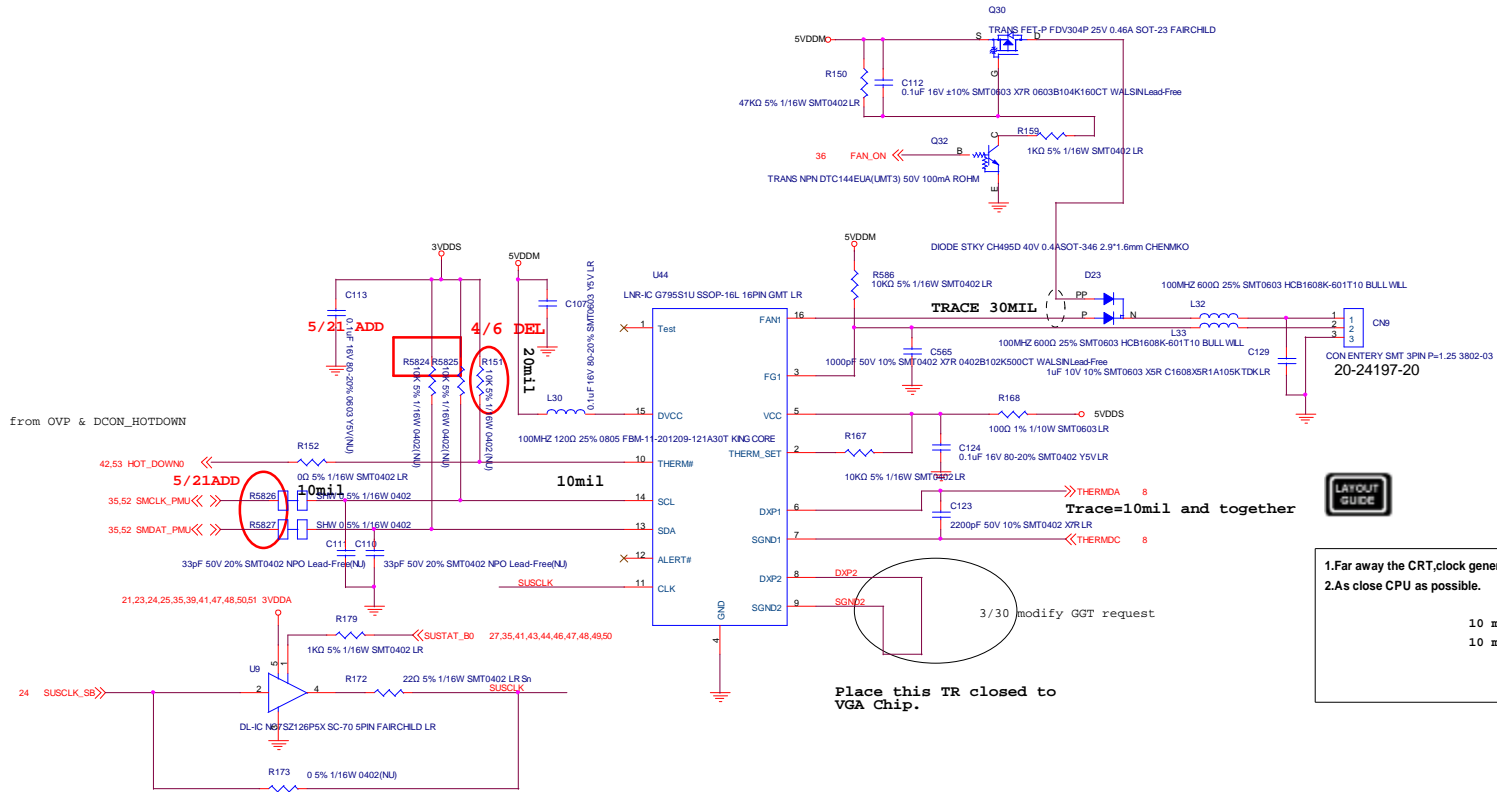


OCP Setting
 1. $I_{ocset} = 1.75V / (54.9K + 45.3K + 75K) = 10\mu A$
 2. $I_{sen1} = 10\mu A / (1/4) / 0.87 = 45.9\mu A$
 3. $I_{sen1} * R_{sense} = I_{ocp} * R_{ds_on}$ (Lowside)
 $I_{ocp} = (I_{sen1} * R_{sense}) / R_{ds_on}$ (Lowside)

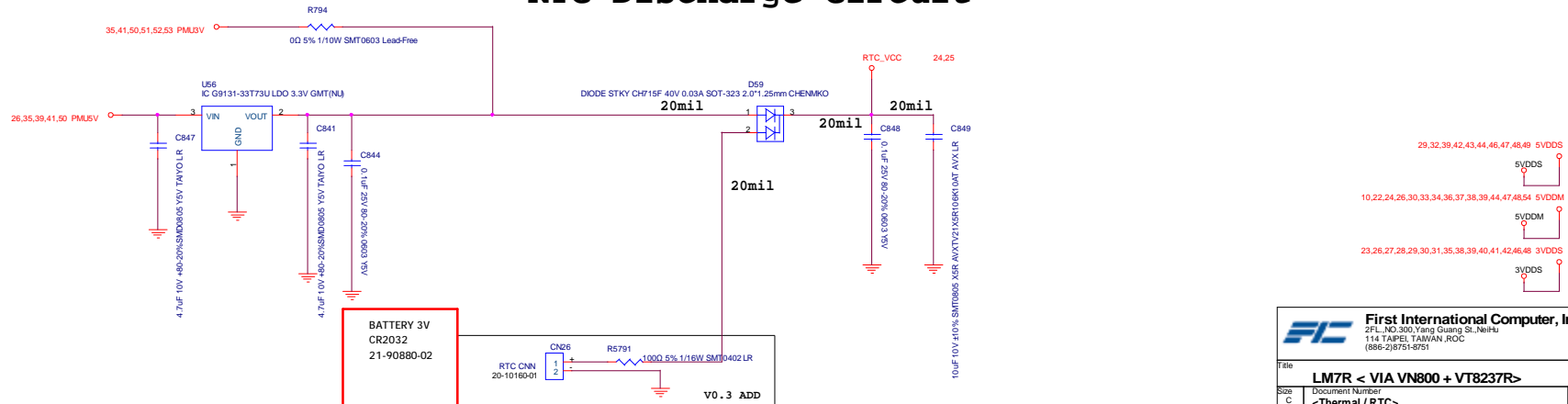
Boost Voltage 1.2V
Deeper Sleep Voltage 0.748V

IMVP IV
 Load line slope : $-3mV/A$
 $V_{droop} : 25A * 3mV/A = 75mV$
 $I_{droop} : 75mV / 6.04K = 12.4\mu A$
 $12.4\mu A / 0.875 / 0.5 = 28.34\mu A$
 $R_{ds(on)} * I_o = I_{sen} * R_{sen}$
 $(6m/2) * 25A = 28.34\mu A * R_{sen}$
 $R_3 = 2.64K$

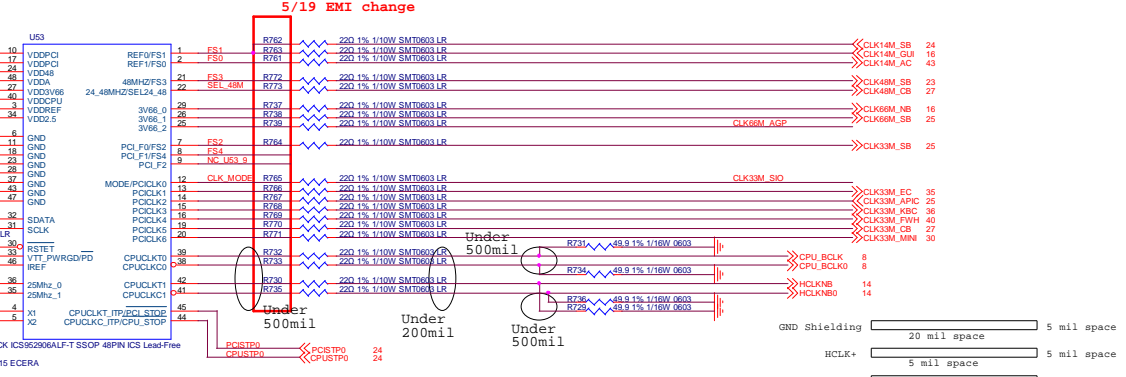
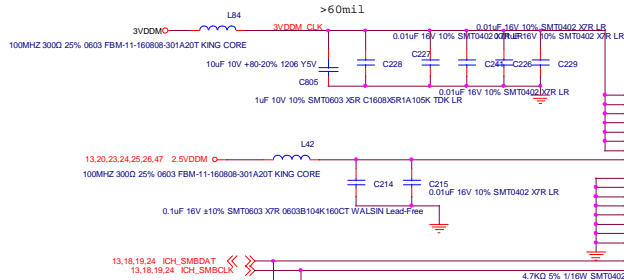
THERMAL SENSOR



RTC Discharge Circuit



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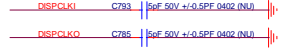
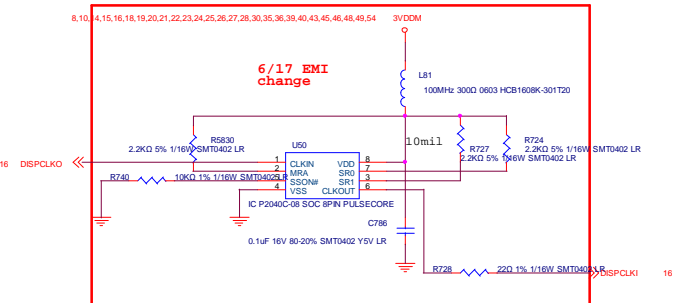
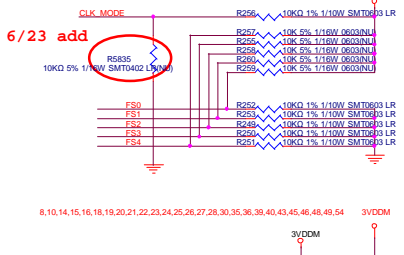
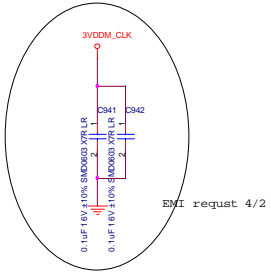
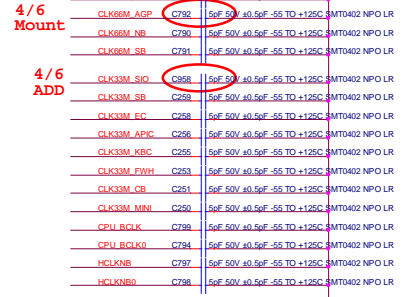
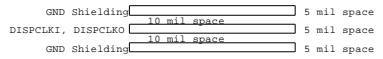


Clock Latout Guideline

CLOCKS	LENGTH	TRACE / SPACE	NOTES
HOST Clock CPU_BCLK[1..0] MCH_BCLK[1..0] ITP_BCLK[1..0]	2" - 8"	5 / 20 mils (5 mil space between 1 & 0)	1. Differentials pairs with the same length (within 20 mil) 2. CPU & NB trace mismatch within 20 mil
CLK66 Clock CLK_ICH66 CLK_MCH66 CLK_AGP	4.5" - 9.0"	5 / 20 mils MAX : 8.5"	Length mismatch within 100 mils
CLK33 Clock CLK_ICHPCI CLK_SIOPCI CLK_FWHPCI	4.5" - 9.0"	5 / 20 mils	Length same as CLK66 Clock Length mismatch within 100mils
PCI Clock CLK_MINPCI CLK_1394PCI CLK_PMU08PCI CLK_CBPCI	4.5"-9.0"	5 / 20 mils	1. Making PCI length with minimum various 2. Length Require CLK33-2.5" 3. Length mismatch +/- 2.0"
CLK14 Clock CLK_SIO14 CLK_ICH14 CLK_TV14	2.0"-9.0"	5 / 20 mils	1. Length mismatch +/- 500 mils
CLK_ICH48 CLK_MCH48	3.5" - 12.5"	5 / 20 mils	

- Clock Layout :**
1. Close to Clock generator
 2. Trace as short as possible and use 12 mil
 3. Place crystal within 500 mils of CLK Generator

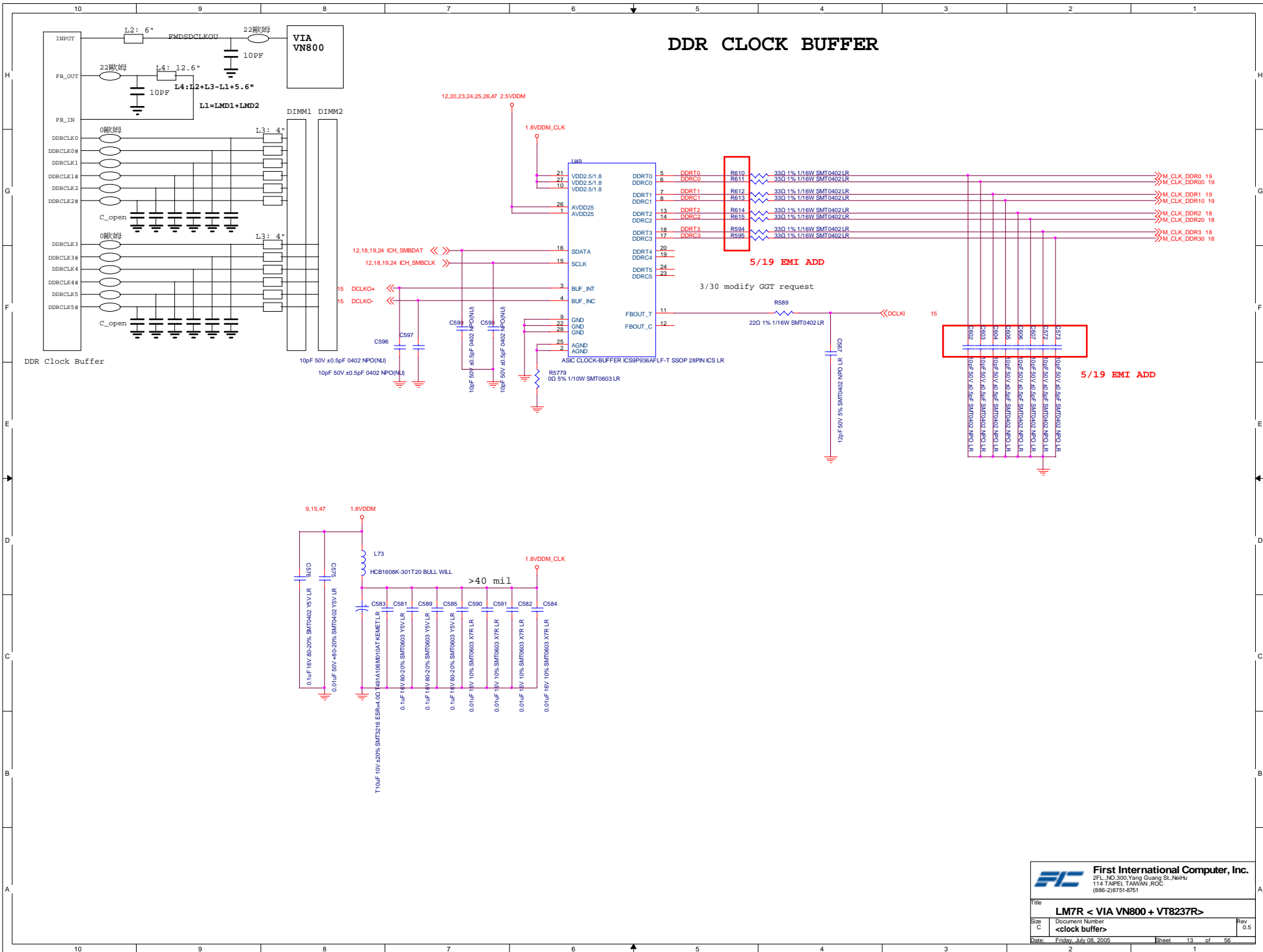
FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	REF
0	0	0	0	0	100.00M	66.67M	33.33M	14.318M
0	0	0	0	1	200.00M	66.67M	33.33M	14.318M
0	0	0	1	0	133.33M	66.67M	33.33M	14.318M
0	0	0	1	1	166.67M	66.67M	33.33M	14.318M
0	0	1	0	1	400.00M	66.67M	33.33M	14.318M



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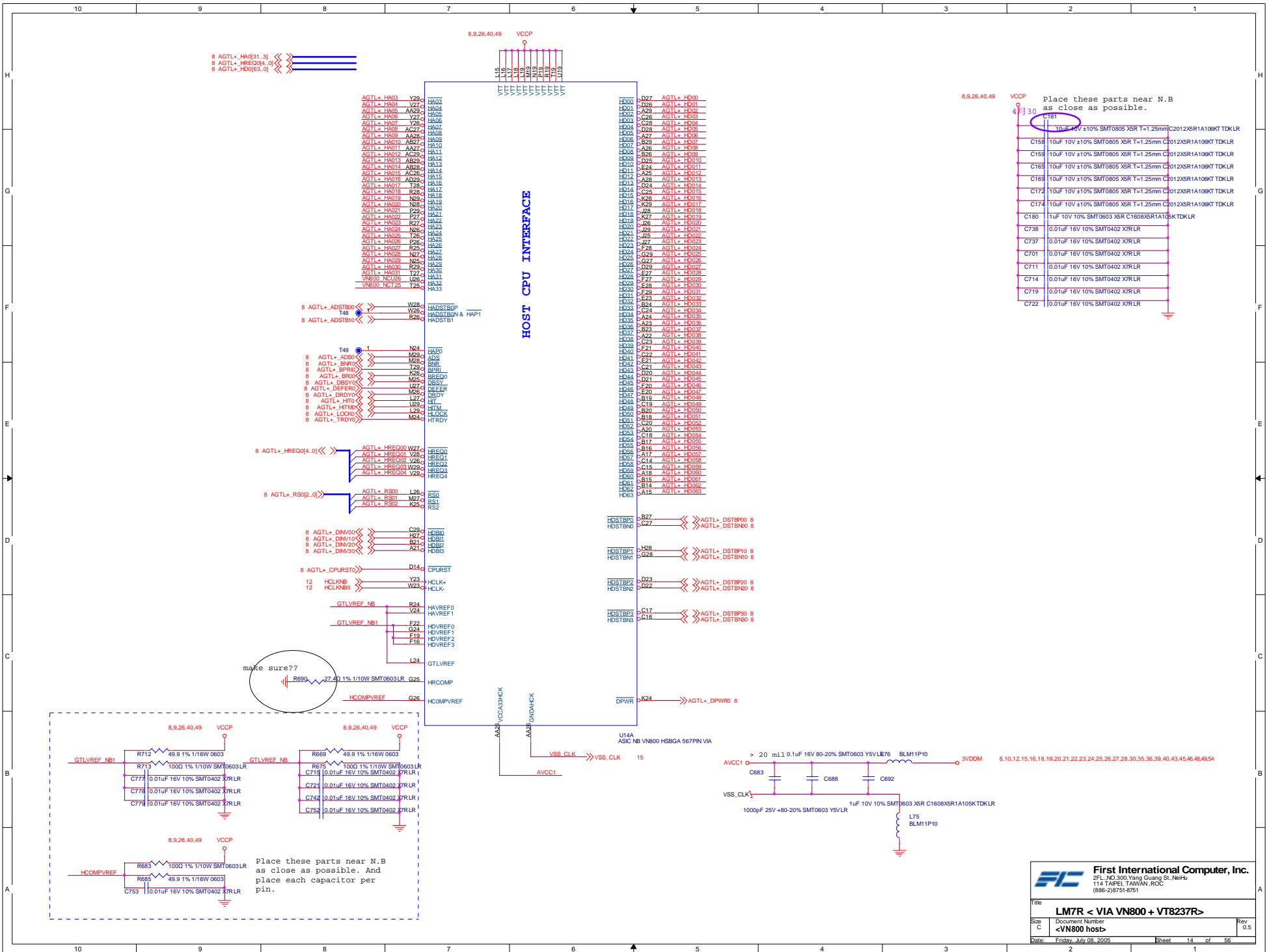
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DDR CLOCK BUFFER



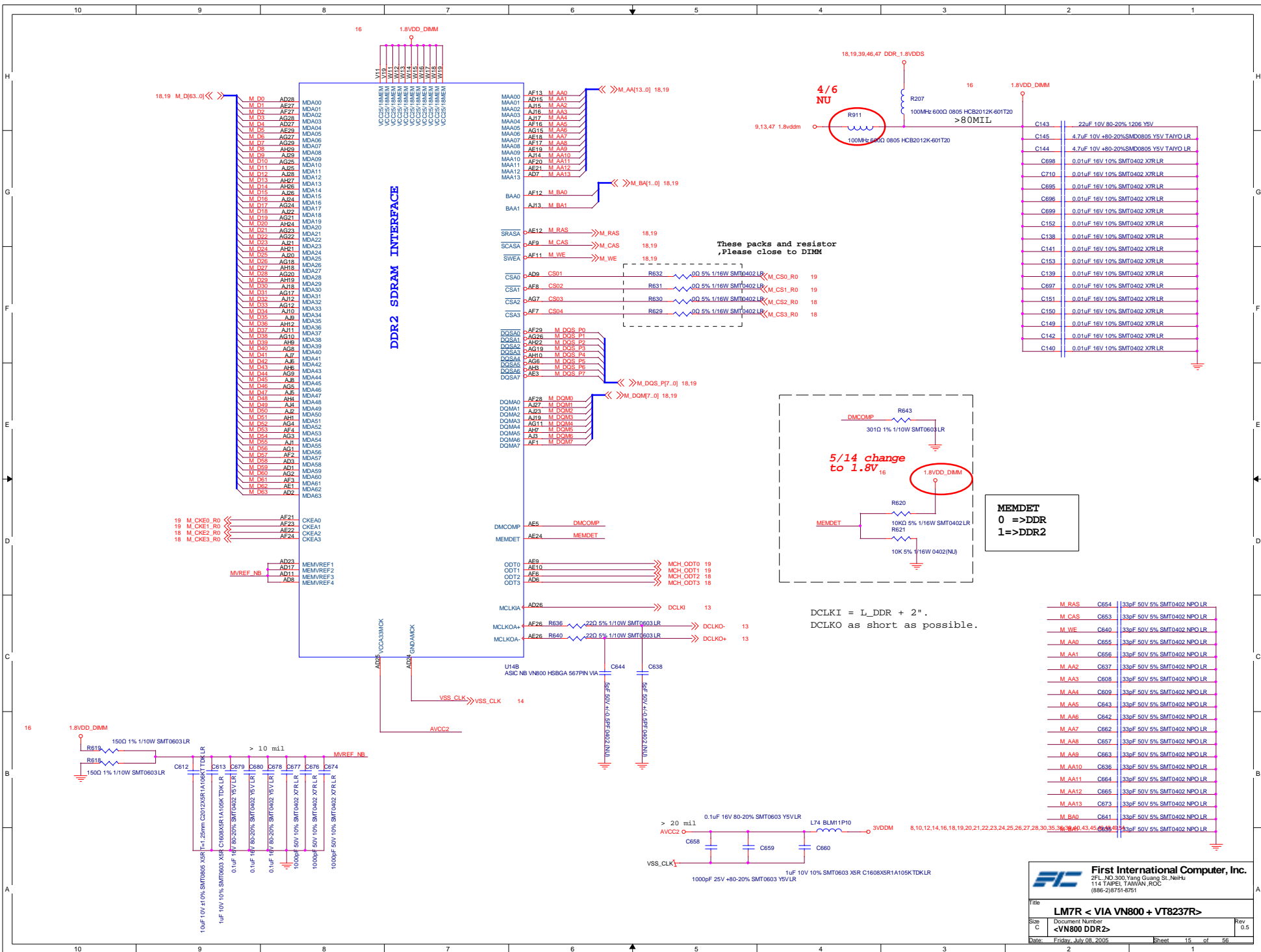
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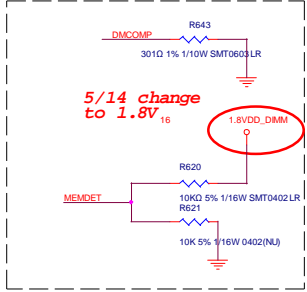


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Title: **LM7R < VIA VN800 + VT8237R >**
 Size: C Document Number
 <VN800 host>
 Date: Friday, July 08, 2005 Sheet 14 of 56 Rev 0.5



These packs and resistor, Please close to DIMM

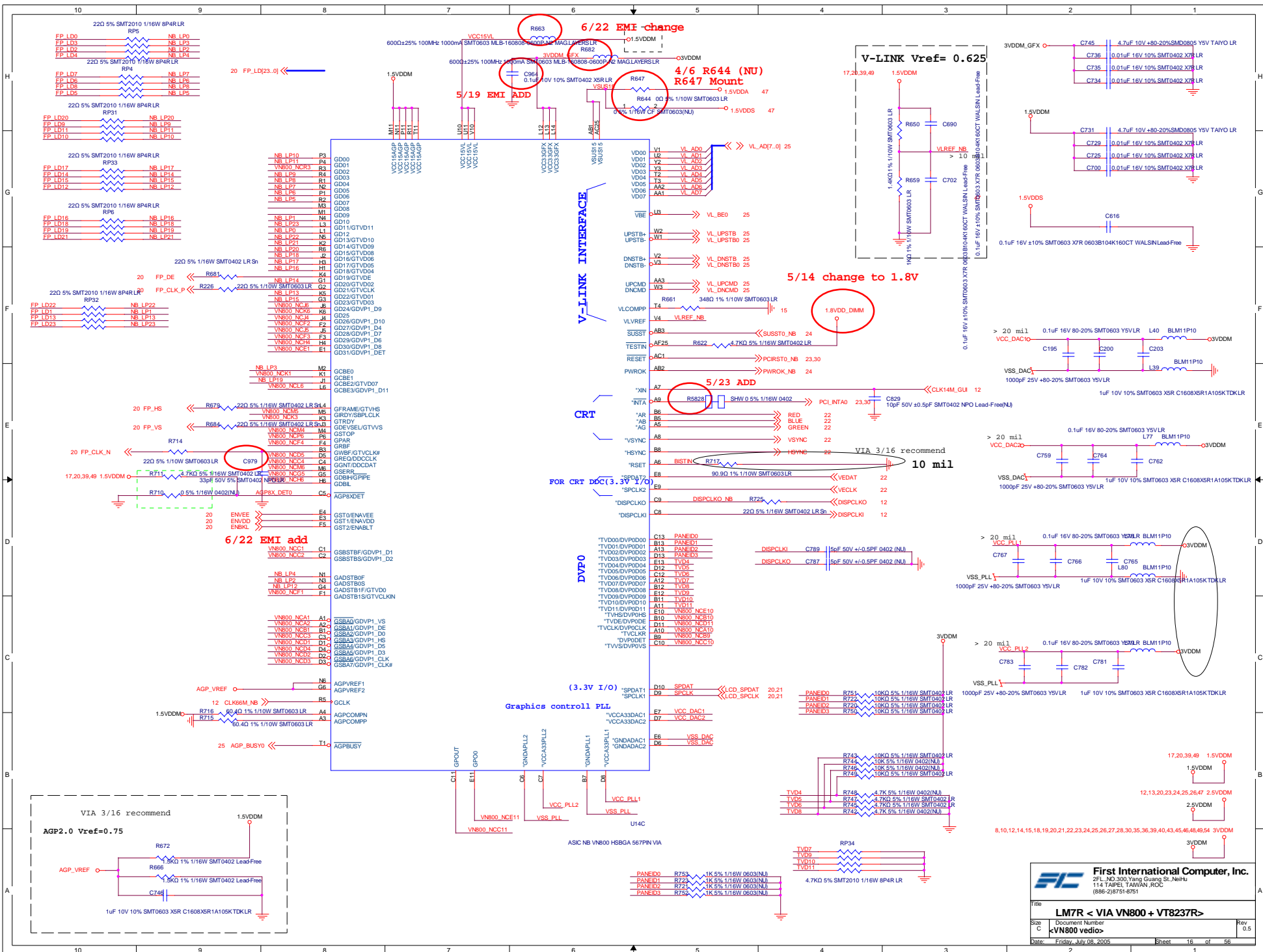


MEMDET
0 => DDR
1 => DDR2

DCLKI = L_DDR + 2".
DCLKO as short as possible.

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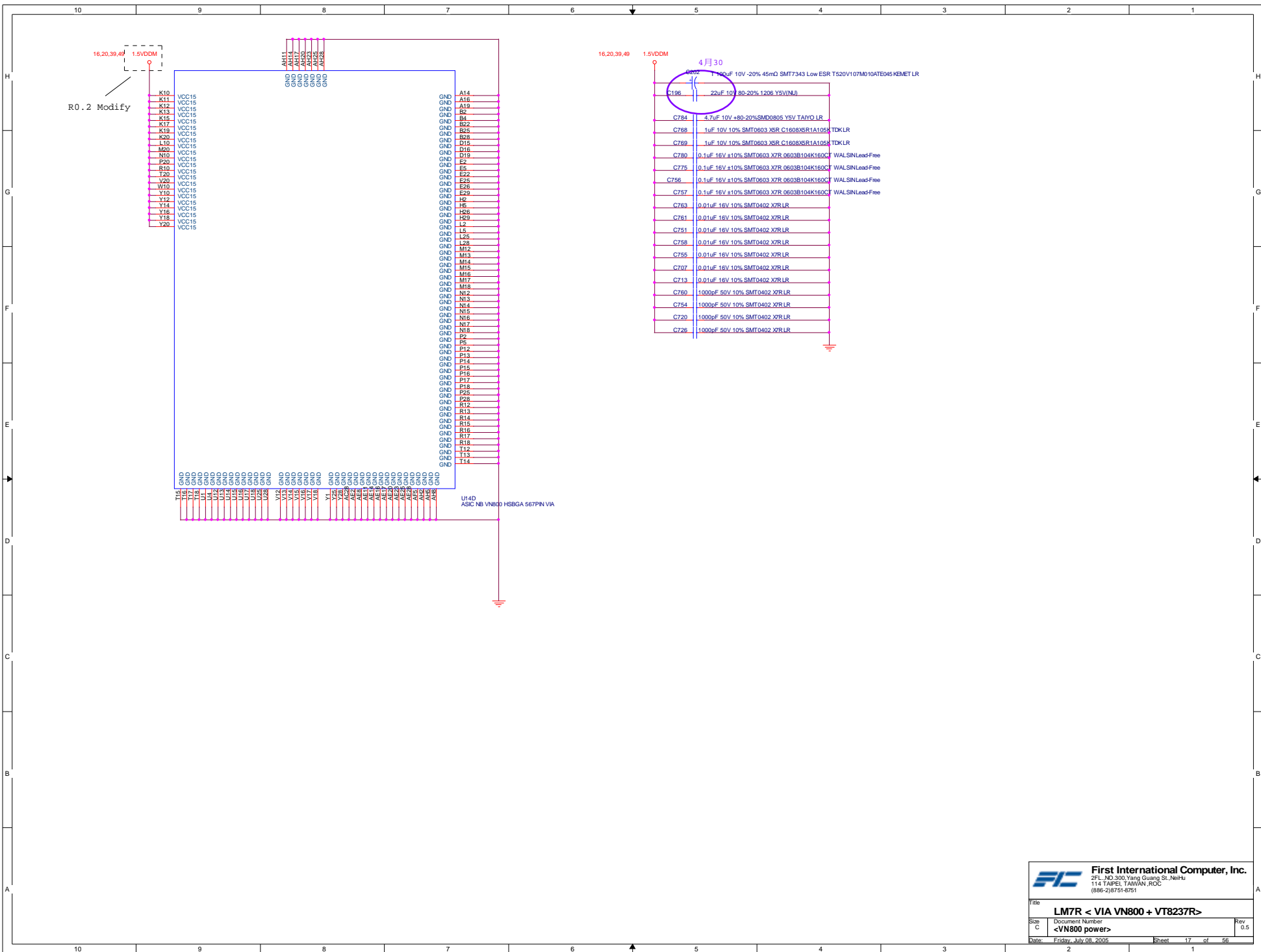
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Size: C Document Number: **<VN800 DDR2>** Rev: 0.5
Date: Friday, July 08, 2005 Sheet: 15 of 56



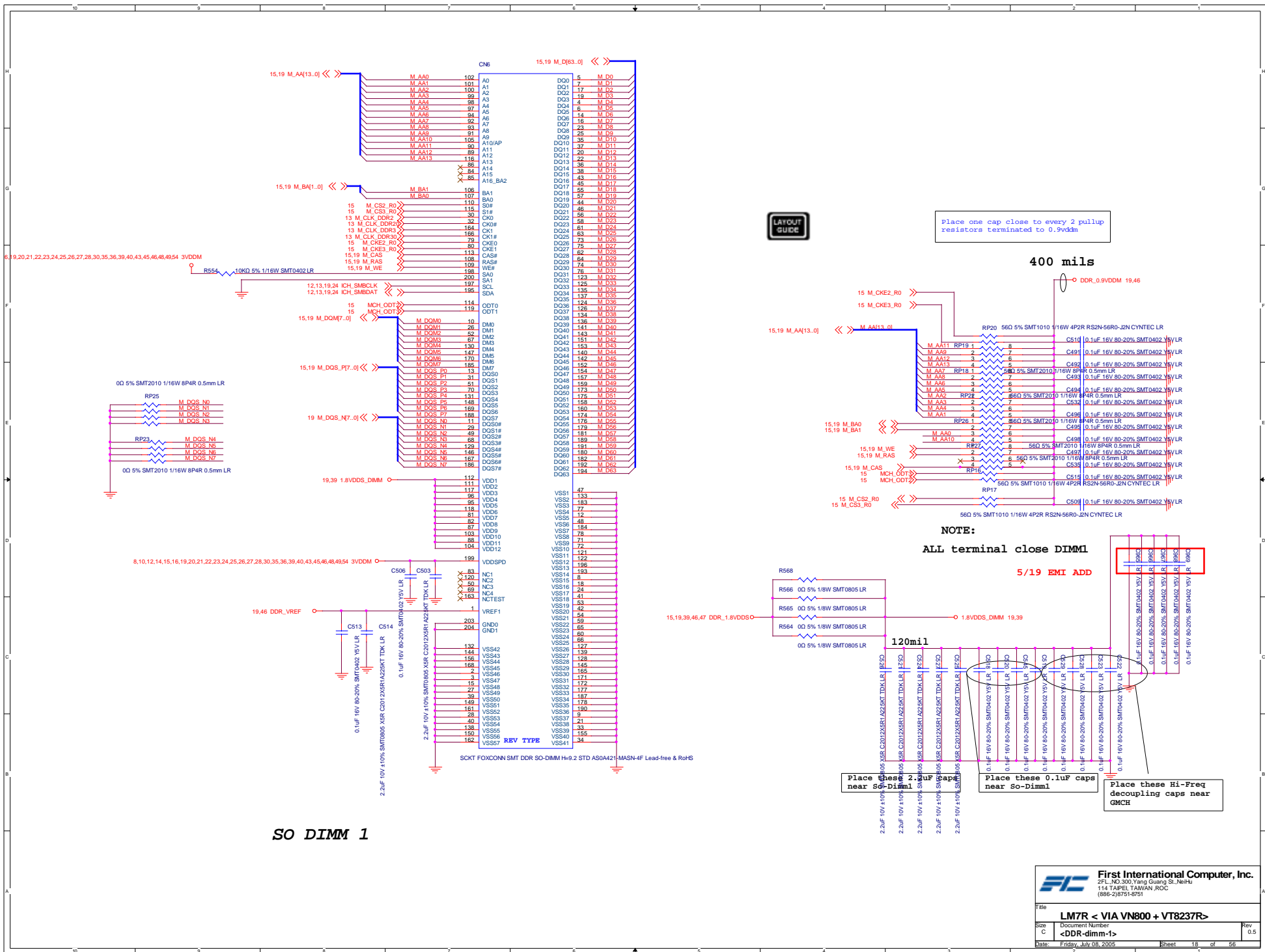
First International Computer, Inc.
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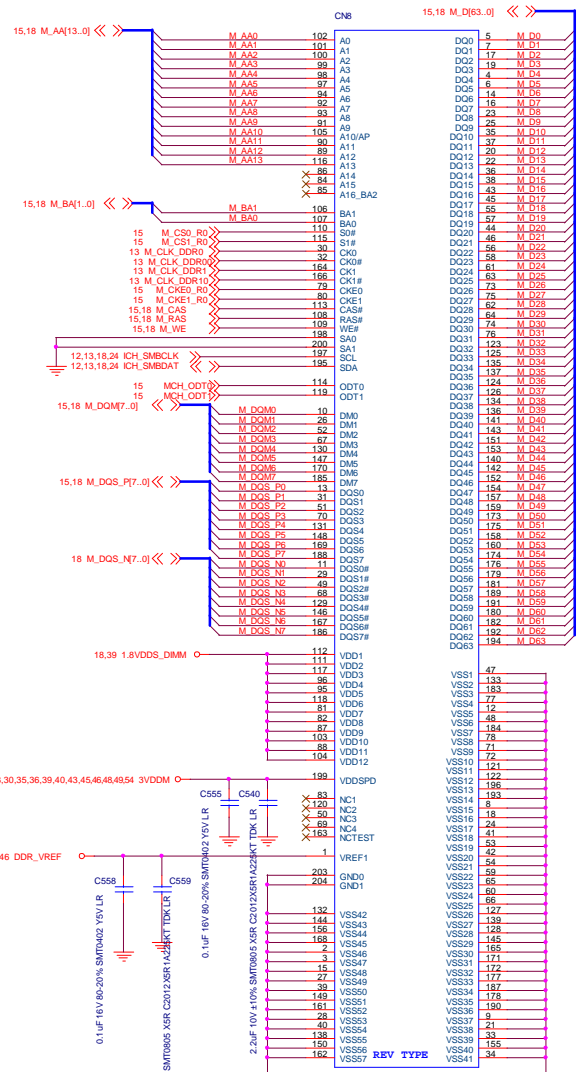
LM7R < VIA VN800 + VT8237R >

Title	Document Number	Rev
Size	<VN800 vedio>	0.5
Date	Friday, July 08, 2005	Sheet 16 of 56

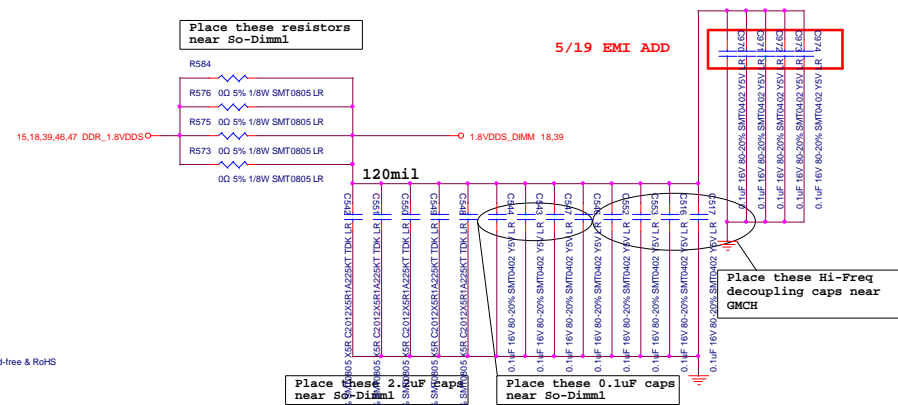
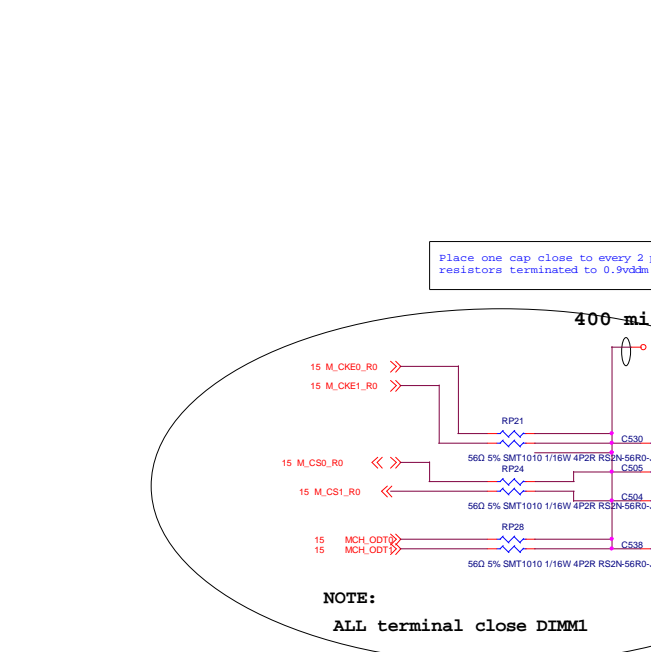


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Title	LM7R < VIA VN800 + VT8237R >
Size	Document Number
C	<VN800 power>
Date	Friday, July 08, 2005
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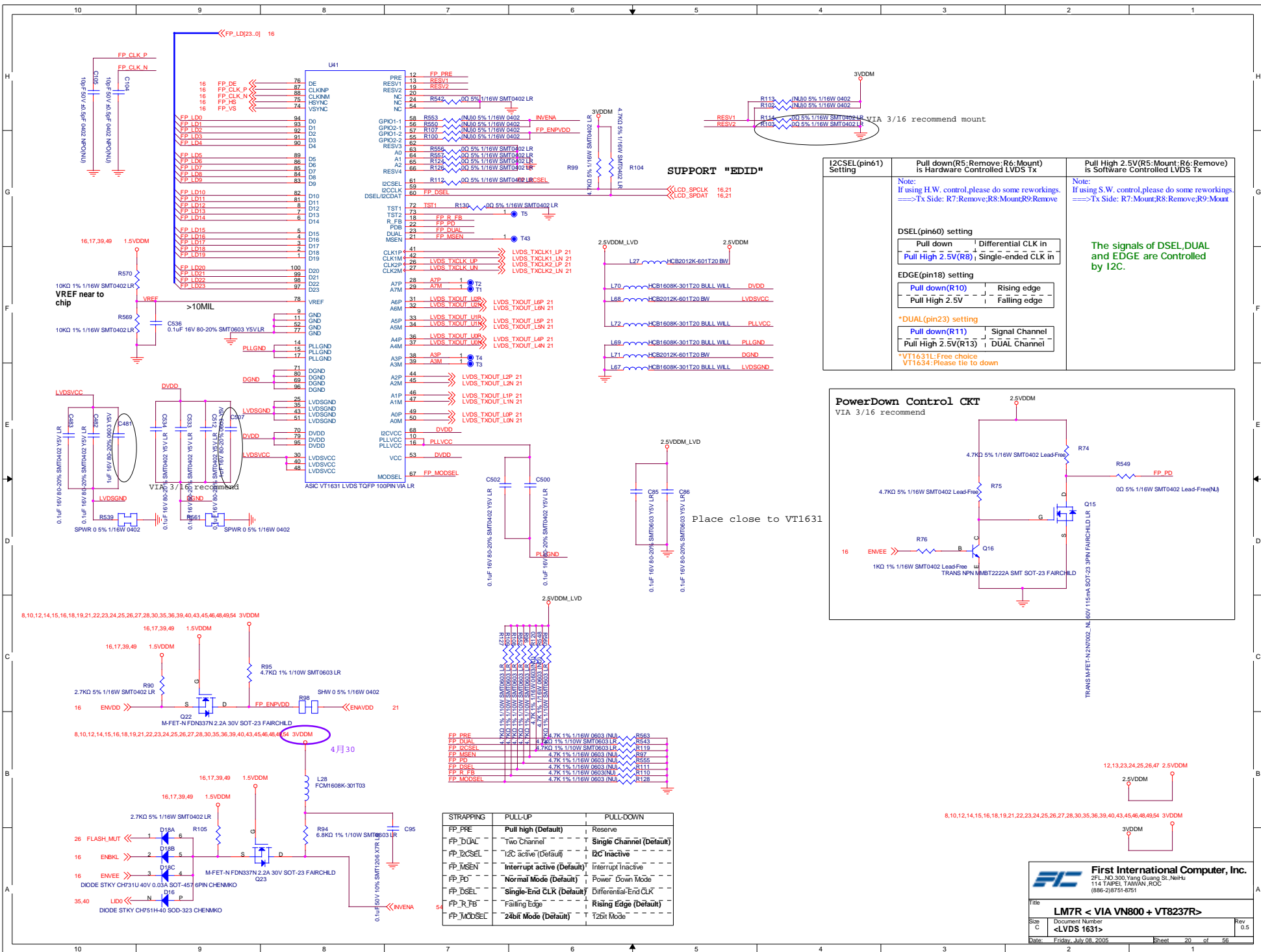


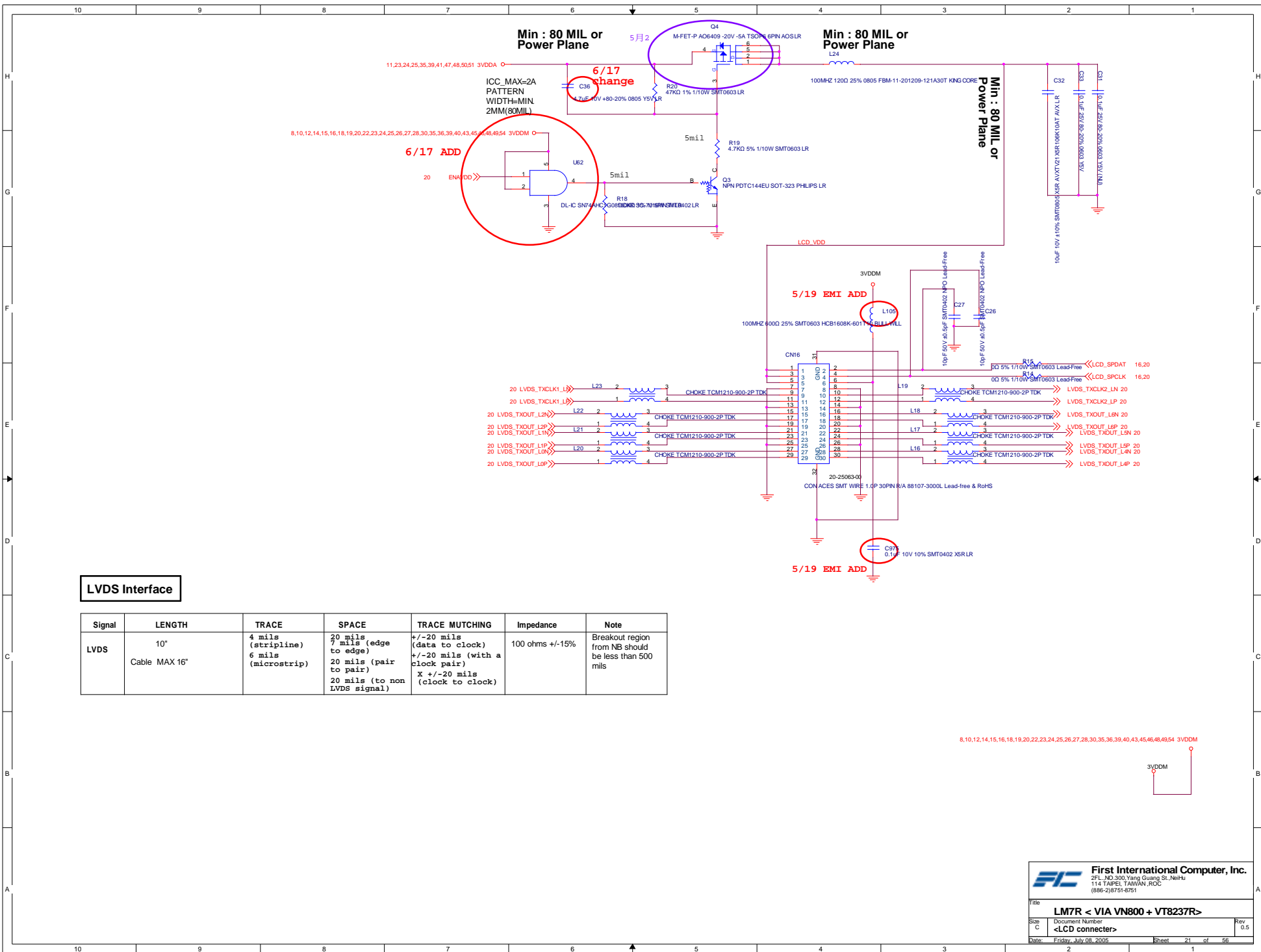
SO DIMM 0



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 Size: C Document Number: **< DDR-dimm-2 >** Rev: 0.5
 Date: Friday, July 08, 2005 Sheet: 19 of 56





LVDS Interface

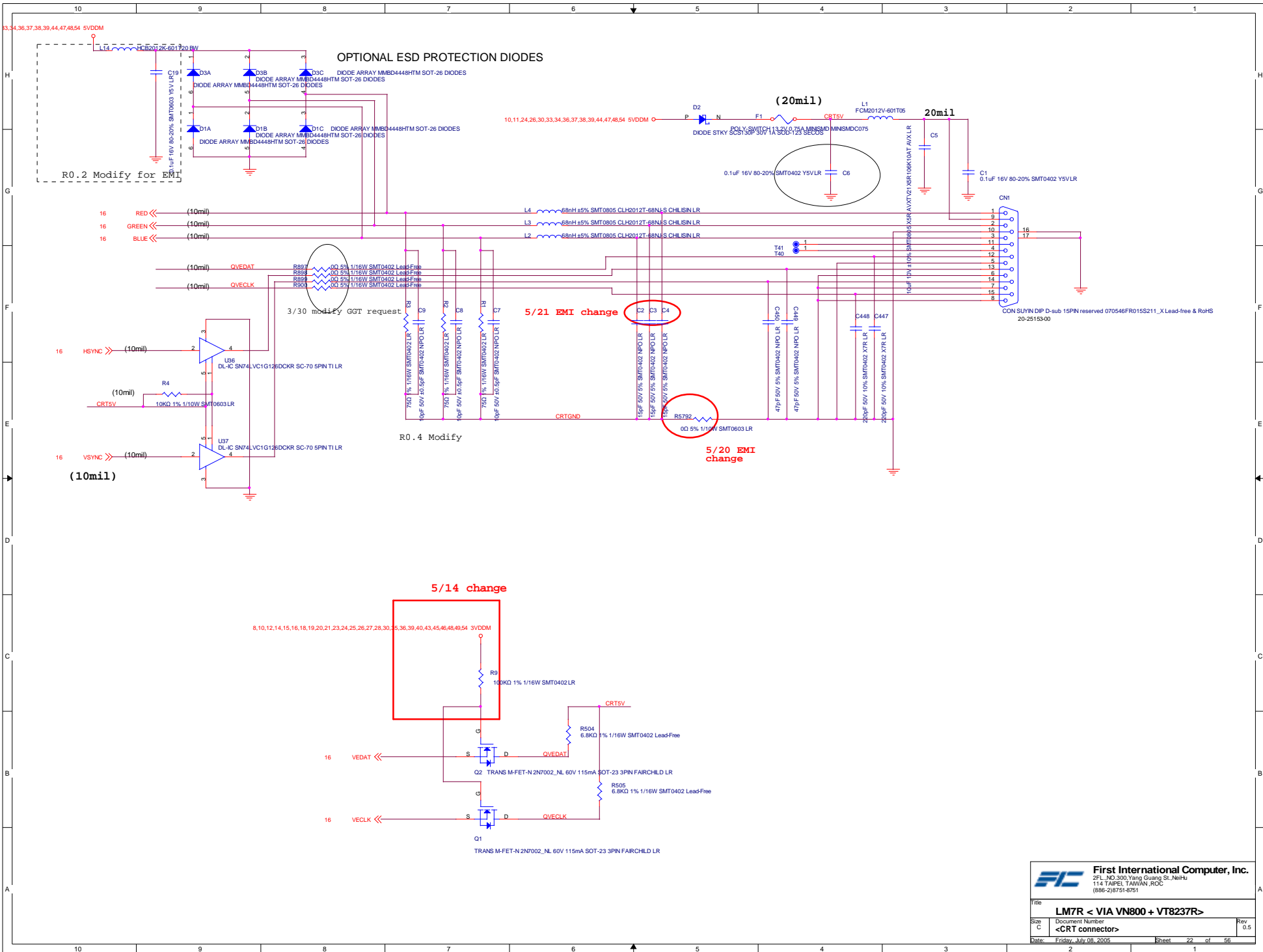
Signal	LENGTH	TRACE	SPACE	TRACE MUTCHING	Impedance	Note
LVDS	10"	4 mils (stripline) 6 mils (microstrip)	20 mils (edge to edge) 20 mils (pair to pair) 20 mils (to non LVDS signal)	+/-20 mils (data to clock) +/-20 mils (with a clock pair) X +/-20 mils (clock to clock)	100 ohms +/-15%	Breakout region from NB should be less than 500 mils

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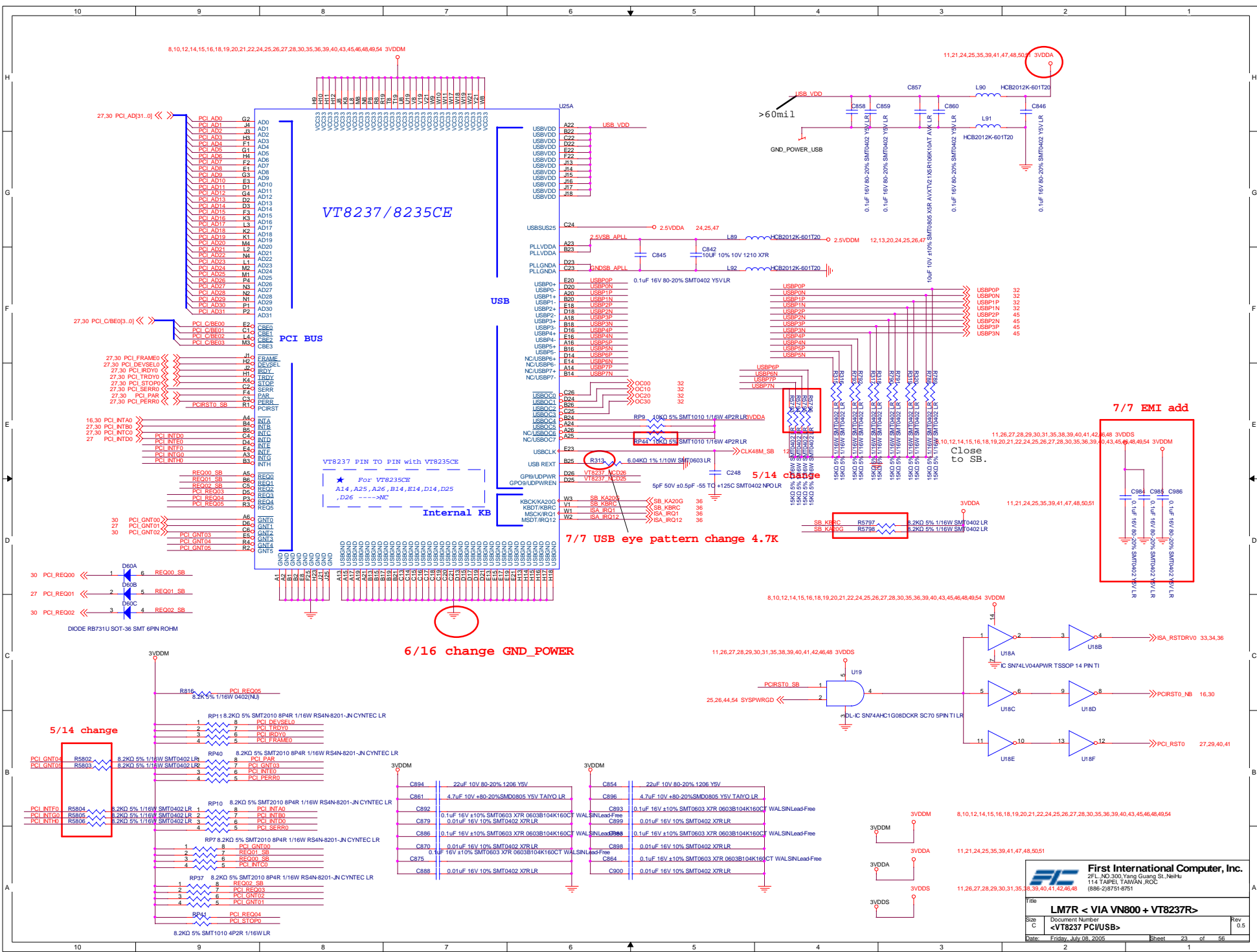
Title: **LM7R < VIA VN800 + VT8237R >**

Size C Document Number: **<LCD connector>** Rev 0.5

Date: Friday, July 08, 2005 Sheet 21 of 56



First International Computer, Inc. 2FL_NO.300,Yang Guang St.,Nehu 114 TAIPEI, TAIWAN, ROC (886-2)8751-8751	

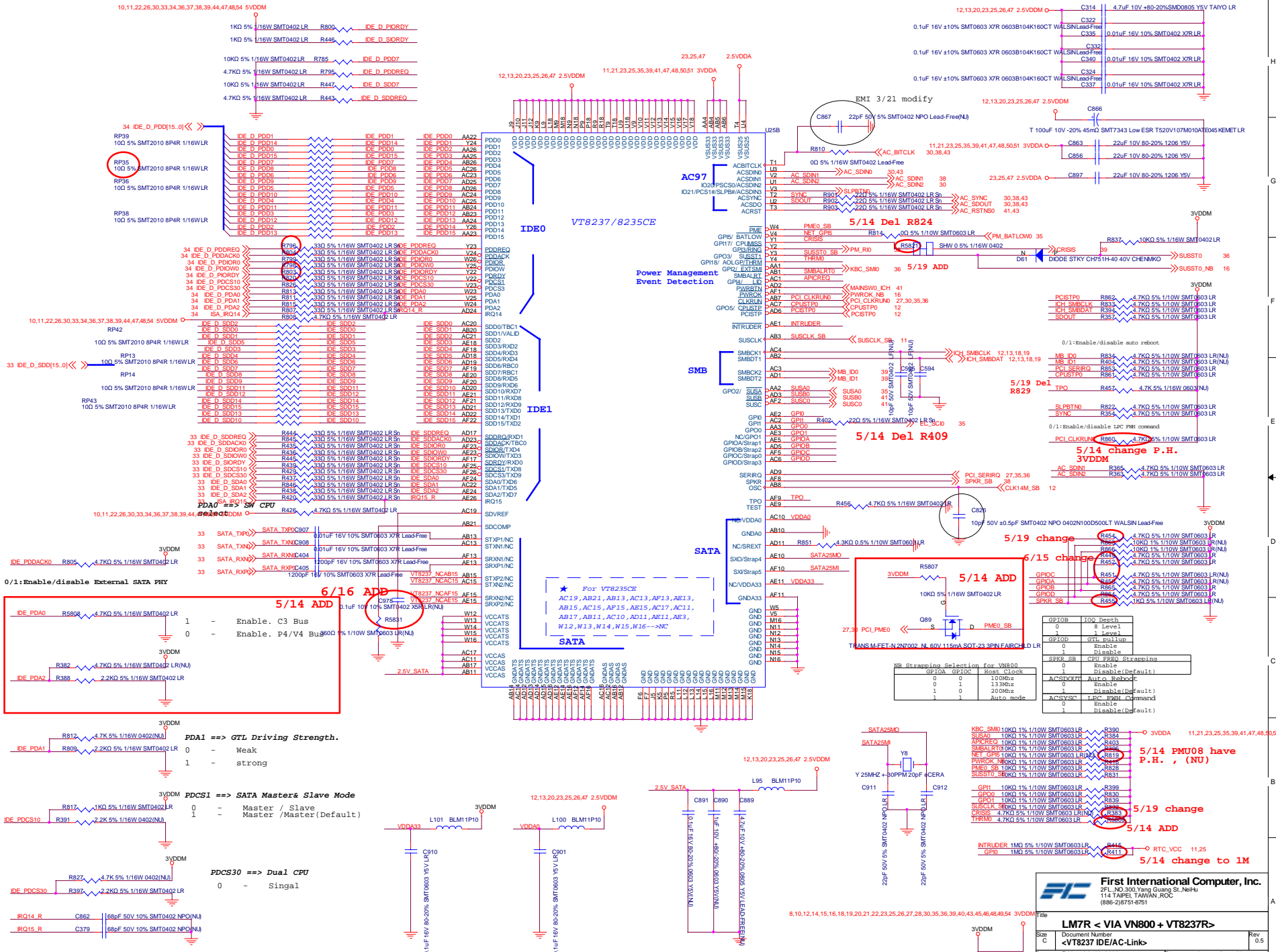


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LM7R < VIA VN800 + VT8237R >
 <VT8237 PCI/USB>

Rev 0.5

Date: Friday, July 08, 2005 Sheet 23 of 56



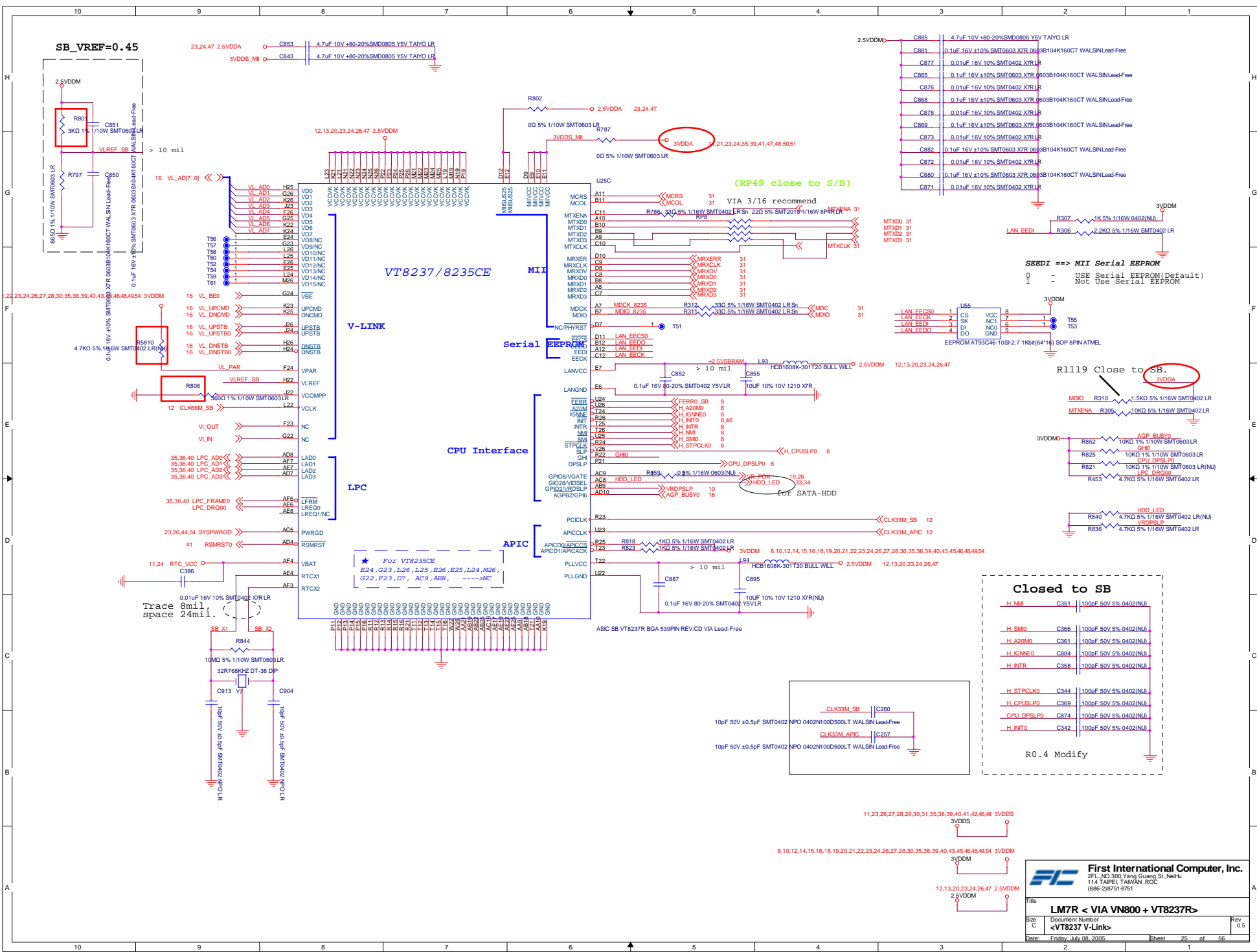
NB Strapping Selection for VN800		
GPIOA	GPIOC	Non-Vol. Clear
0	0	100ms
0	1	133ms
1	0	200ms
1	1	Auto. mode

ACSDPWRT	
ACSDPWRT	Auto. Reboot
0	Enable
1	Disable(Default)

ACSVSVC	
ACSVSVC	IRC. SWH Command
0	Enable
1	Disable(Default)

TRANS.MFEET.N27002.NL.6V.115mA.SOT-23.3PN.FAIRC.D.LR

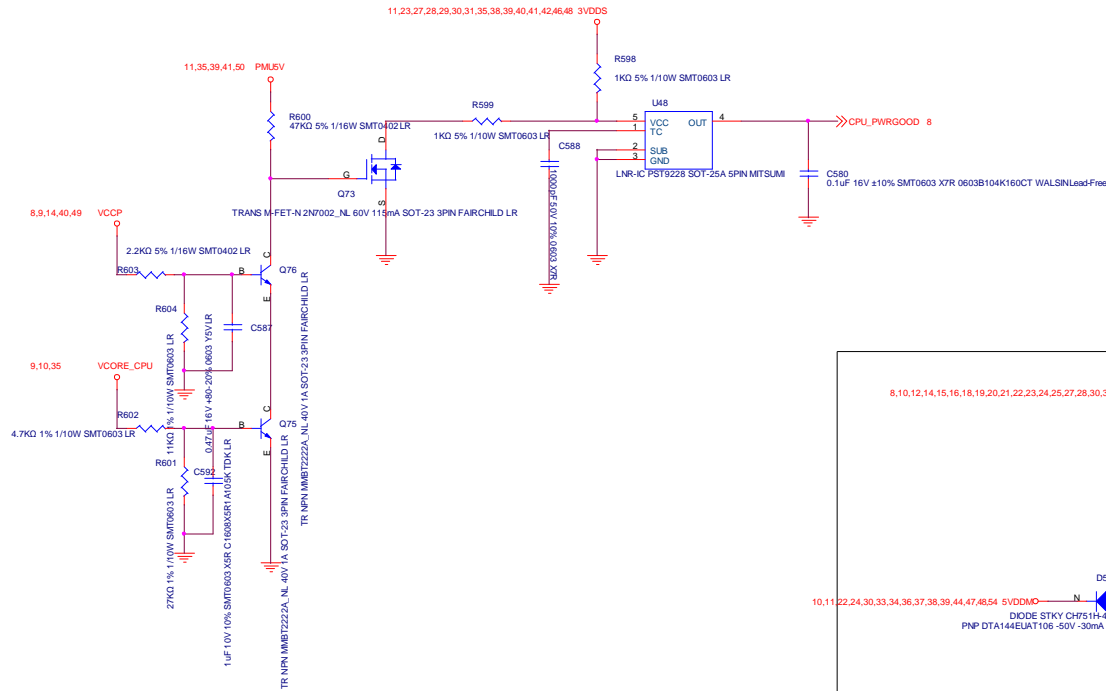
First International Computer, Inc.
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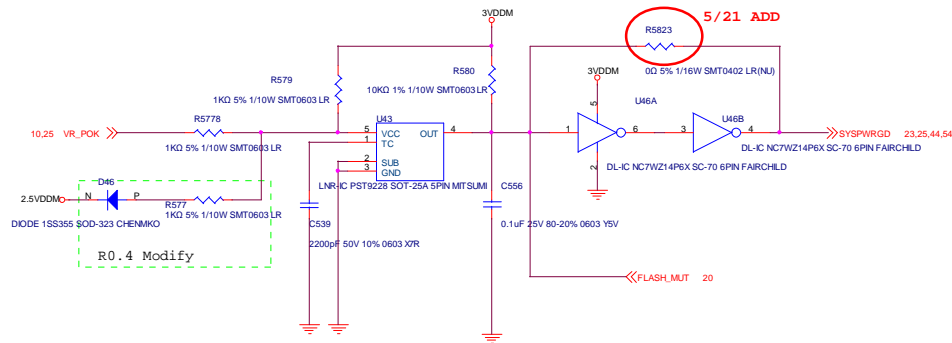
First International Computer, Inc.
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Title: **LM7R < VIA VN800 + VT8237R >**
 Document Number: **<VT8237 V-Link>** Rev 0.5
 Date: Friday, July 08, 2005 Sheet 25 of 56

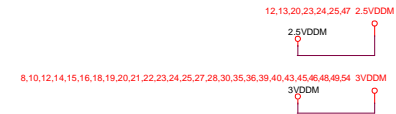
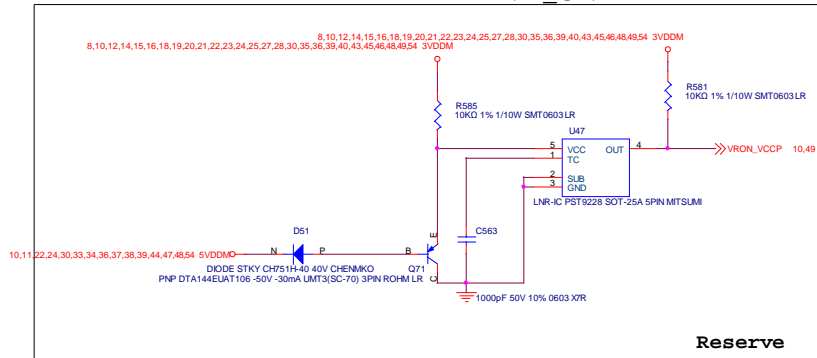
CPU POWER OK CIRCUIT



SYSTEM POWER OK CIRCUIT

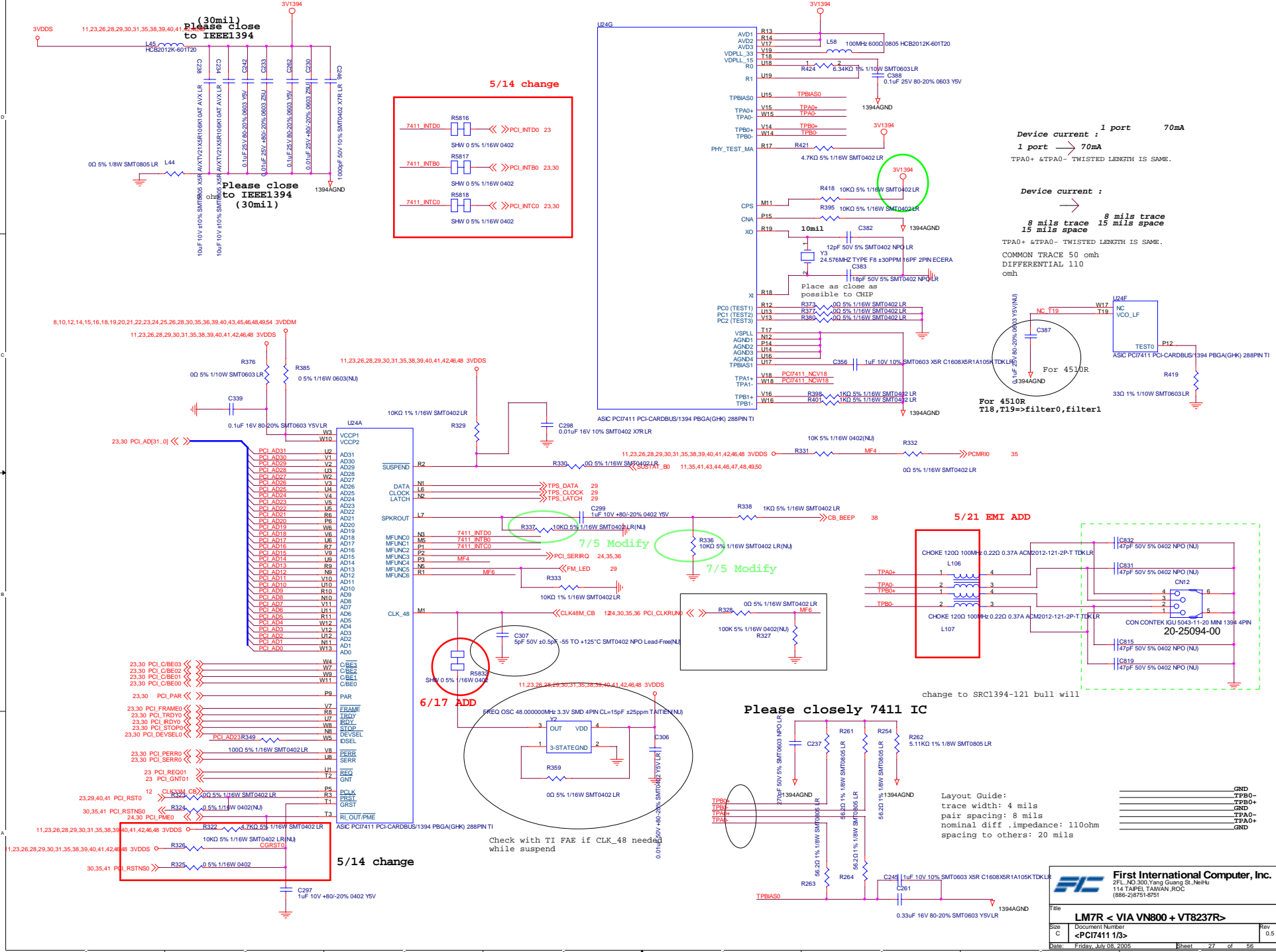


VR_ON



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Title: LM7R < VIA VN800 + VT8237R >		
Size: C	Document Number: POWER GOOD	Rev: 0.5
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Please close to 7411 IC

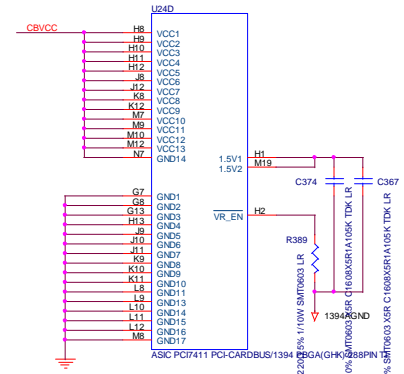
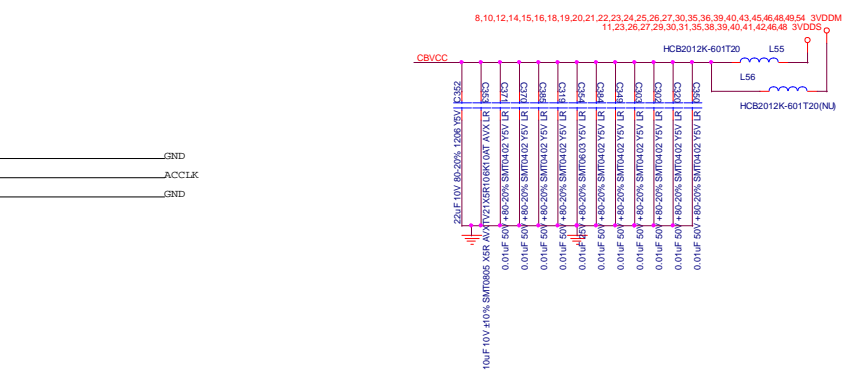
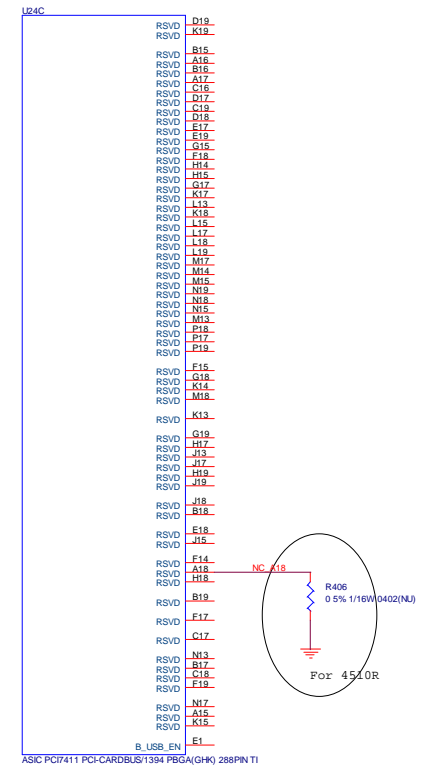
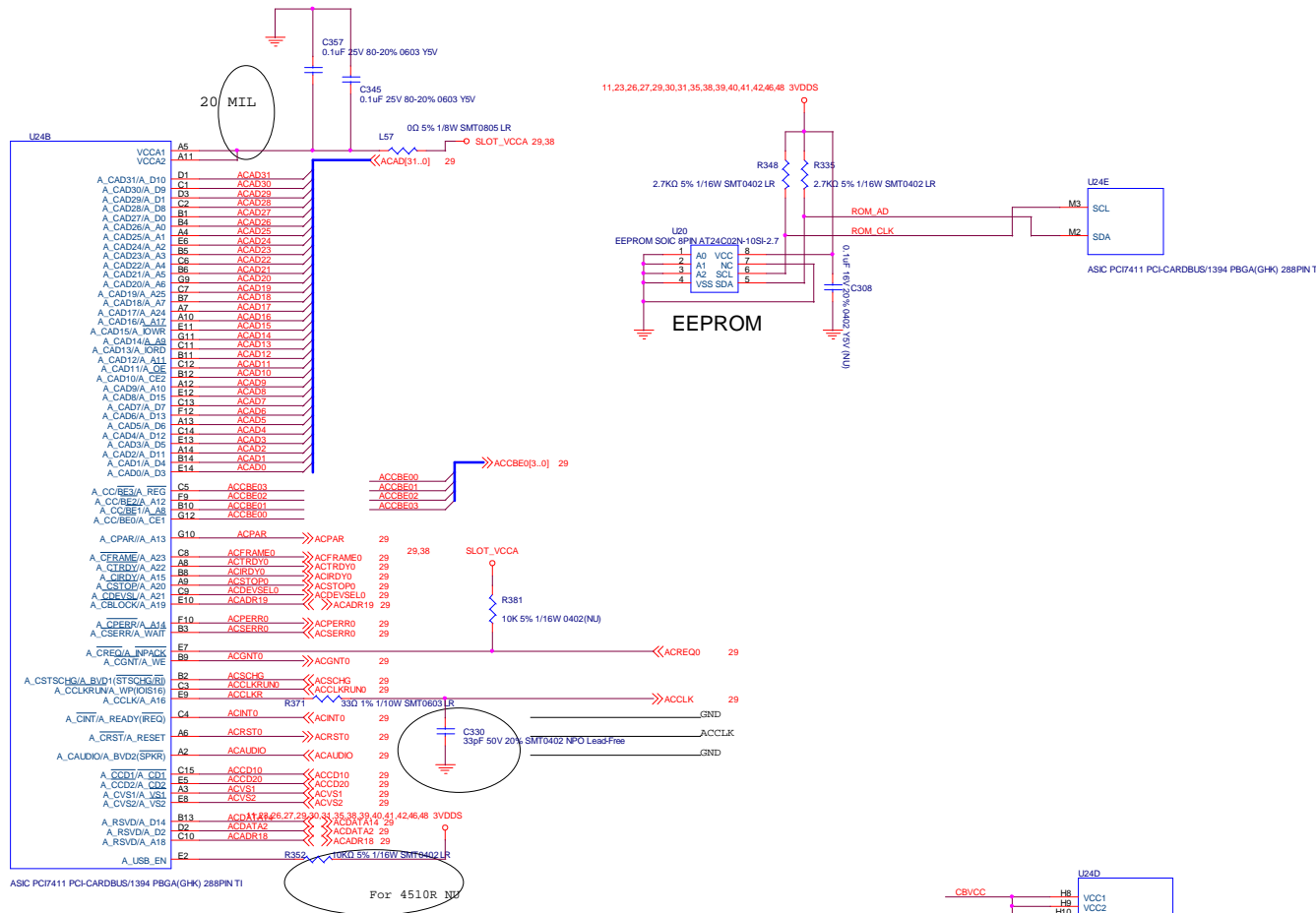


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Title: **LM7R < VIA VN800 + VT8237R >**

Size	Document Number	Rev
C	<PCI7411 I/S>	0.5

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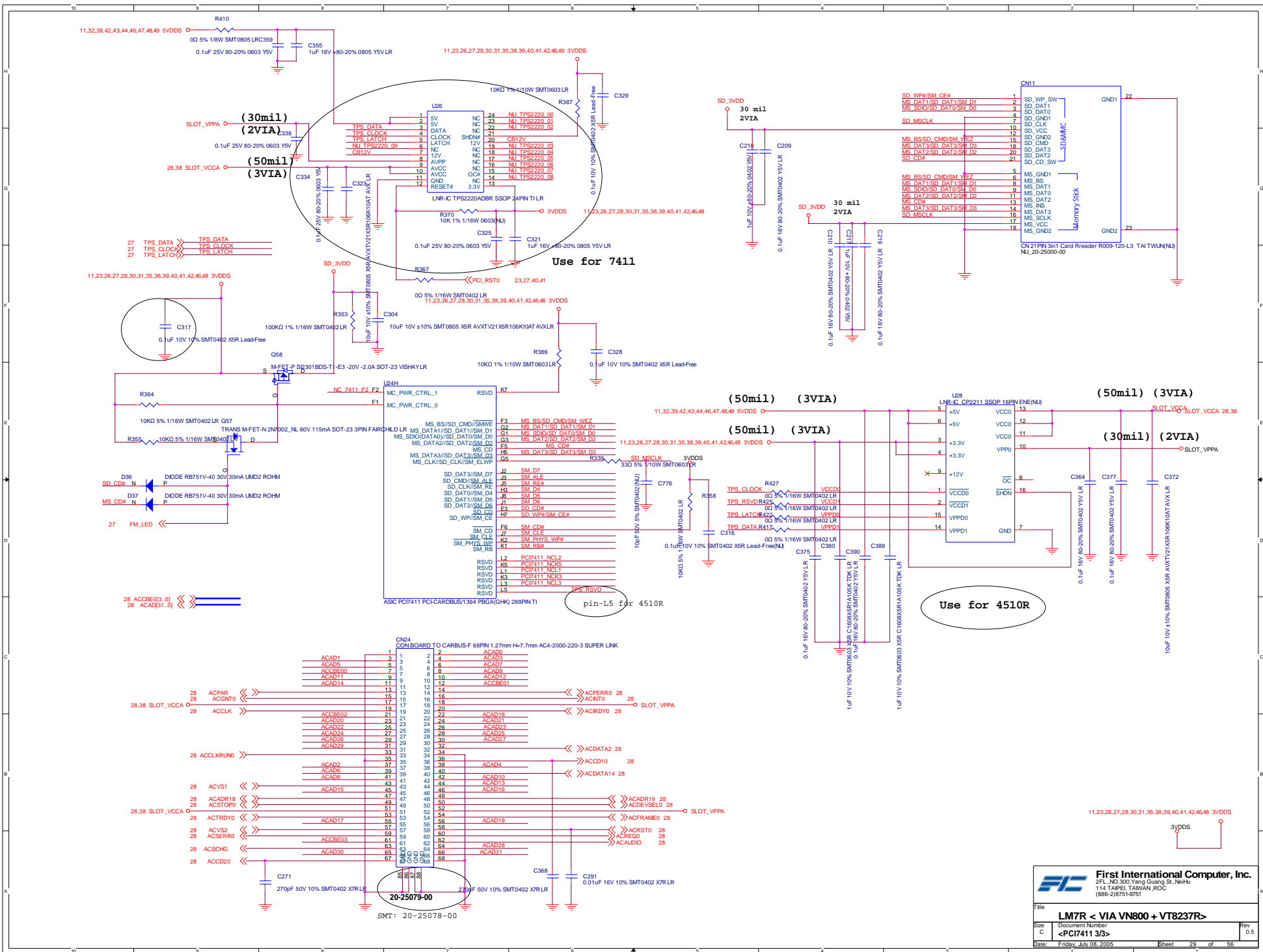
VR_EN= HIGH (for 451.0R)
H1,M19 =>to 1.8V
VR_EN= LOW (for 451.0R)
H1,M19 =>to GND

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Title: **LM7R < VIA VN800 + VT8237R >**

Size: C Document Number: <PC17411 2/3> Rev: 0.5

Date: Friday, July 08, 2005 Sheet: 28 of 56



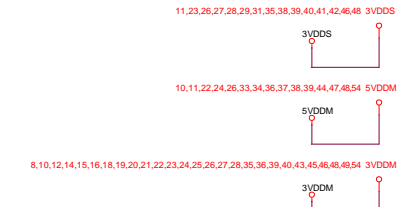
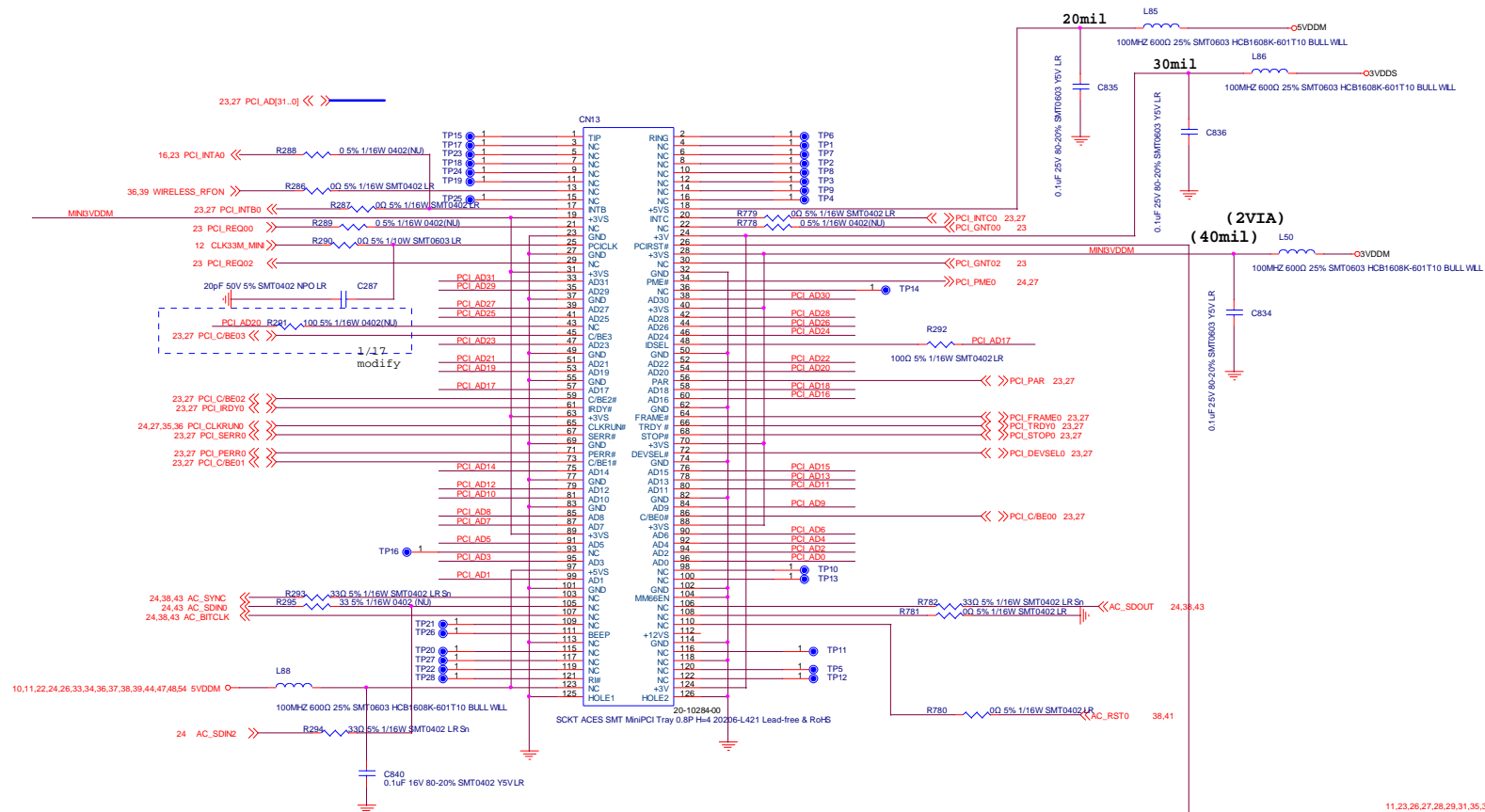
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Title: **LM7R < VIA VN800 + VT8237R >**

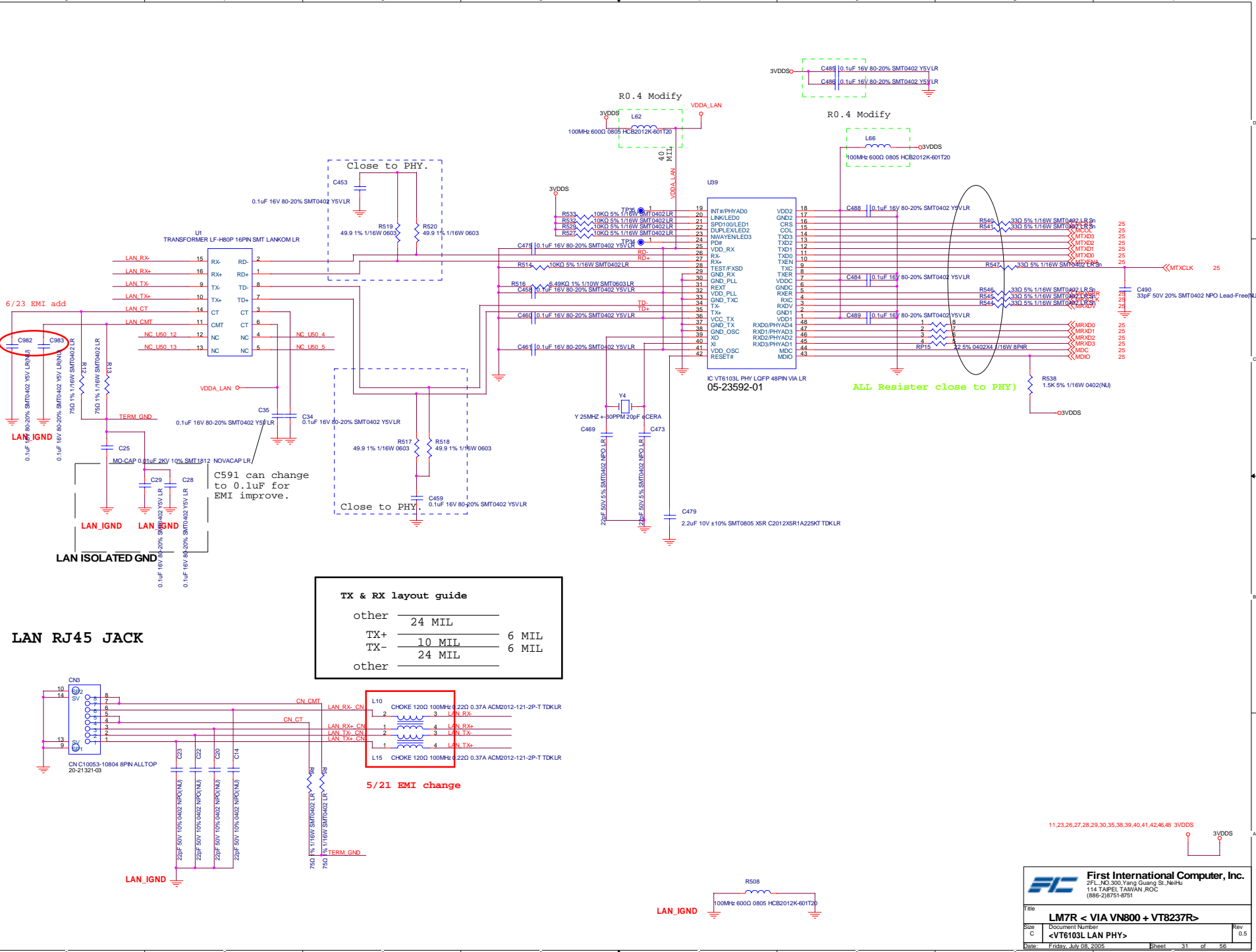
Size: C Document Number: **<PC17411 3/3>** Rev: 0.5

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TYPE III MODEM / LAN CONNECTOR



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Title	
LM7R < VIA VN800 + VT8237R >	
Size	Document Number
C	<Mini-PCI>
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LAN RJ45 JACK

TX & RX layout guide

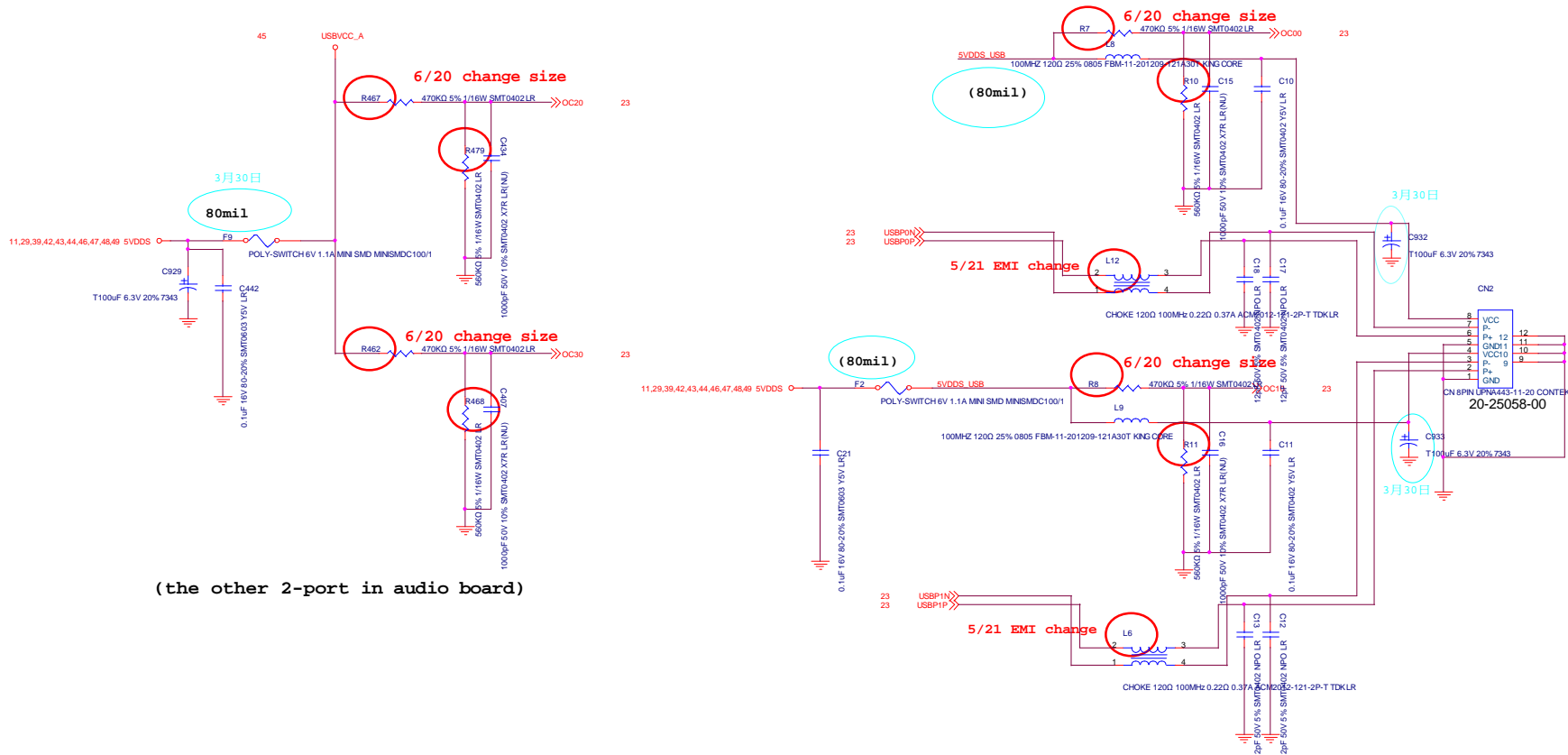
other	24 MIL	
TX+	10 MIL	6 MIL
TX-	24 MIL	6 MIL

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Title: **LM7R < VIA VN800 + VT8237R >**

Size: C Document Number: **<VT8103L LAN PHY>** Rev: 0.5

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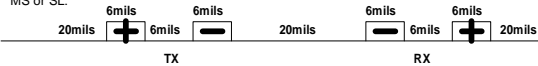
(the other 2-port in audio board)

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Title		
LM7R < VIA VN800 + VT8237R >		
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SATA Layout Note:

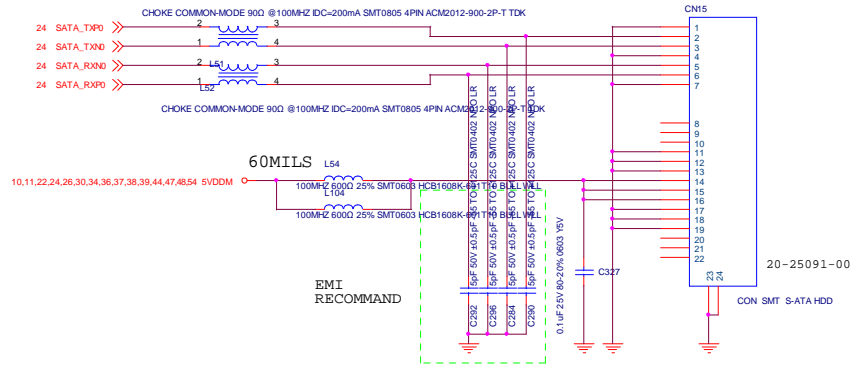
MS or SL:



- * Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs. The Best layer is Top.
- * TX/RX trace length < 2 inchs.
- * TX+/- need matching trace ±10 mils length.
- * RX+/- need matching trace ±10 mils length.
- * SATA Pair to Pair Trace matching trace ±10 mils length.

NOTE

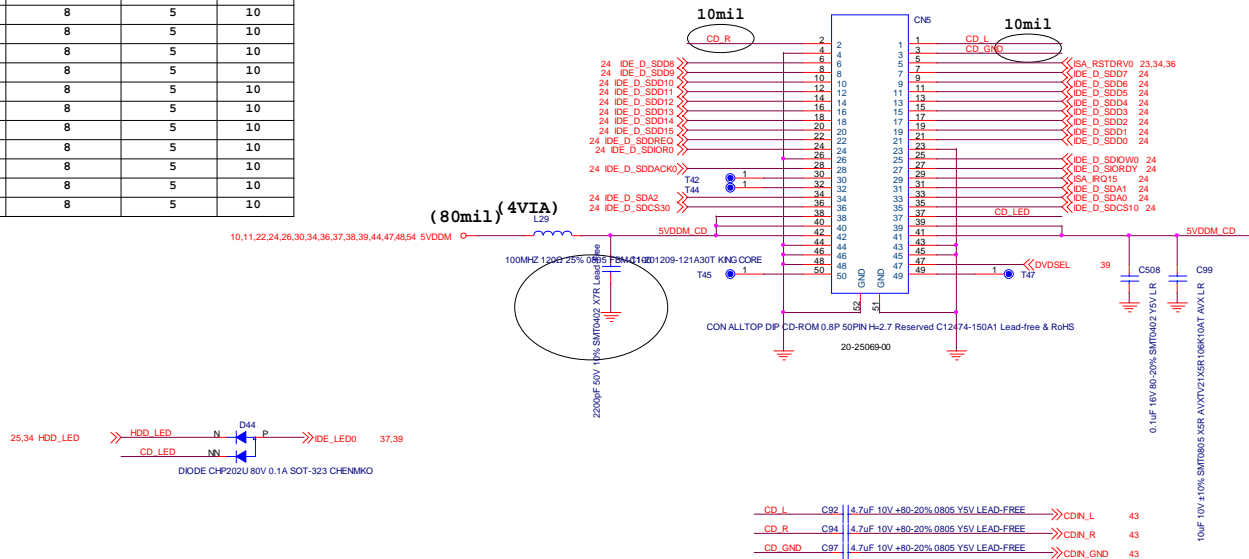
SATA differential stripline 20:5:6:5:20
 SATA differential microstripline 20:6:6:6:20
 請包GROUND



IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN



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Title: **LM7R < VIA VN800 + VT8237R >**

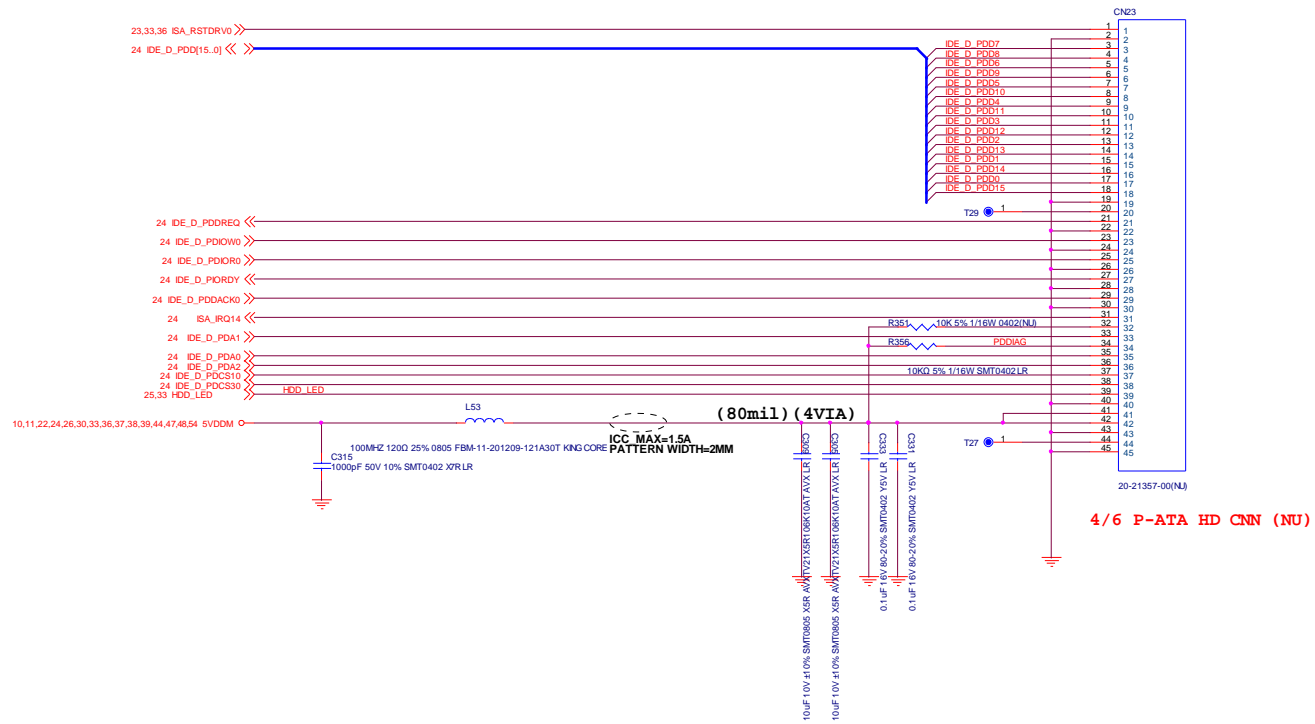
Size: C | Document Number: IDE connectors | Rev: 0.5

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PATA-HDD SWITCH CNN(option)

IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIO#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10



FIC First International Computer, Inc.
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Title: **LM7R < VIA VN800 + VT8237R >**

Size: C Document Number: <PATA-FPC-CNN> Rev: 0.5

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PMU08

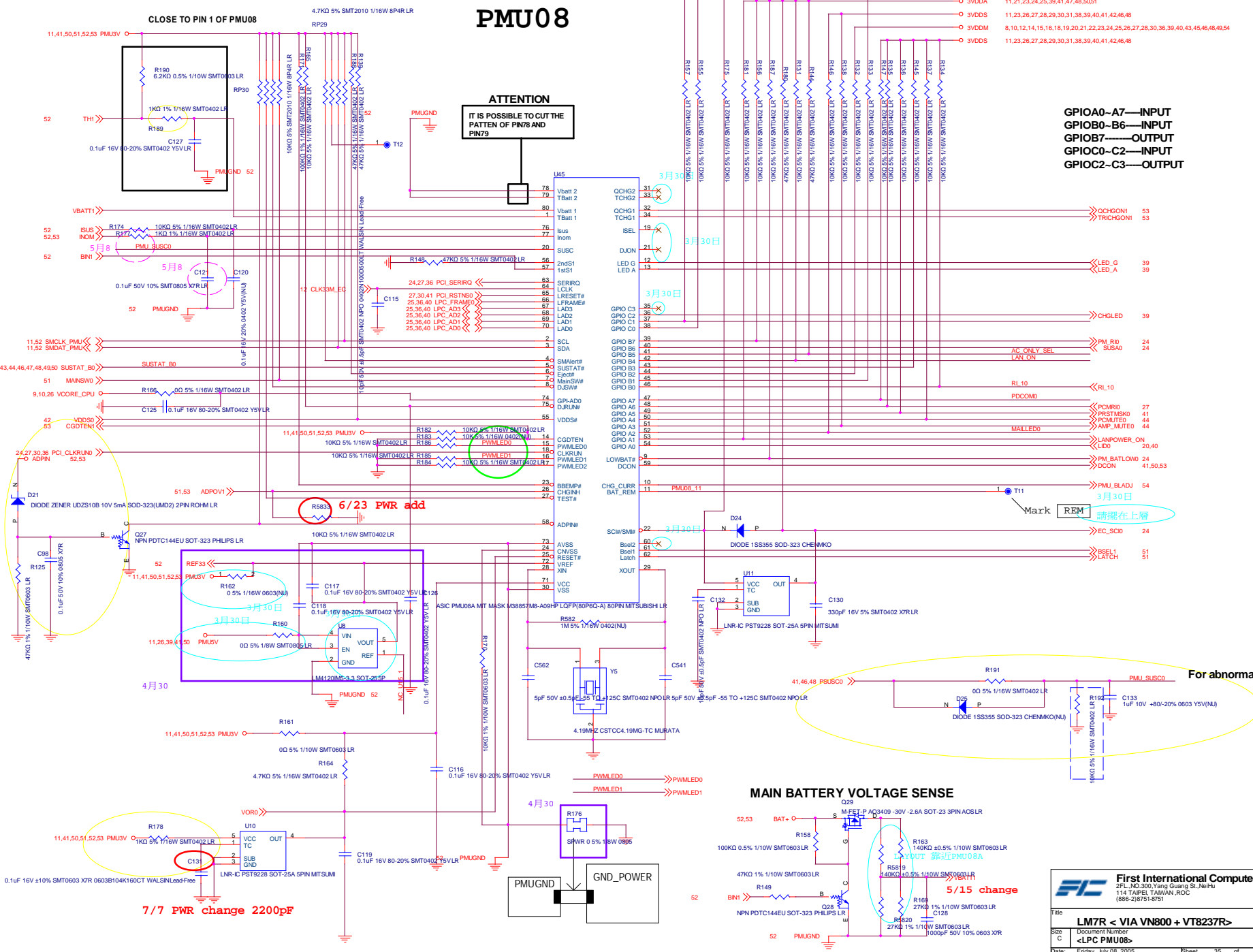
CLOSE TO PIN 1 OF PMU08

ATTENTION

IT IS POSSIBLE TO CUT THE PATTERN OF PIN78 AND PIN79

- PMU0V 11.41,50.51,52,53
- 3VDDA 11.21,23,24,25,39,41,47,48,50,51
- 3VDDS 11.23,26,27,28,29,30,31,38,39,40,41,42,46,48
- 3VDDM 8.10,12,14,15,16,18,19,20,21,22,23,24,25,26,27,28,30,36,39,40,43,45,46,48,49,54
- 3VDDS 11.23,26,27,28,29,30,31,38,39,40,41,42,46,48

GPIOA0-A7—INPUT
GPIOB0-B6—INPUT
GPIOB7—OUTPUT
GPIOC0-C2—INPUT
GPIOC2-C3—OUTPUT

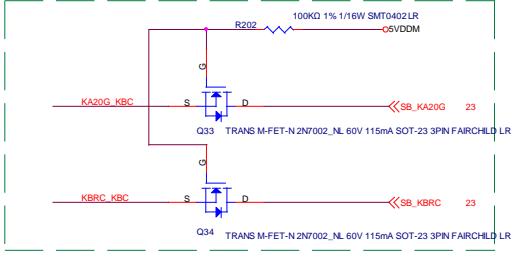
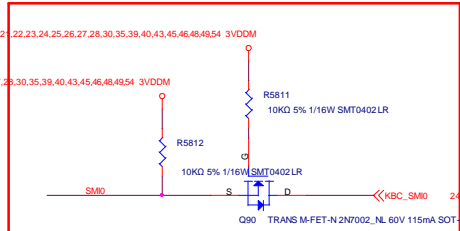
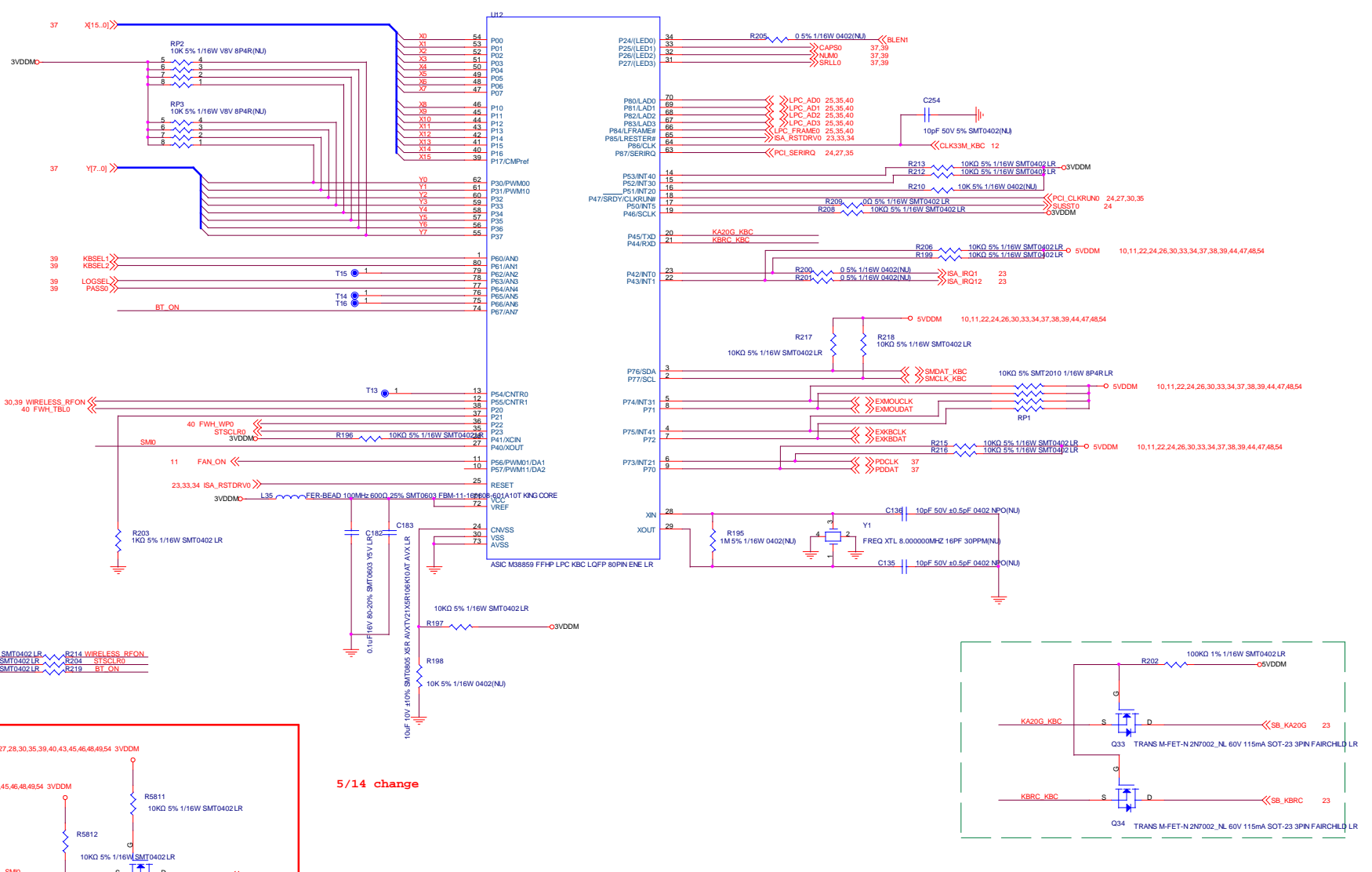


7/7 PWR change 2200pF

MAIN BATTERY VOLTAGE SENSE

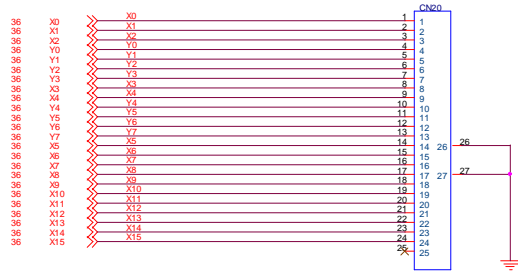
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Title: **LM7R < VIA VN800 + VT8237R >**
Size: C Documents Number: **<LPC PMU08>** Rev: 0.5
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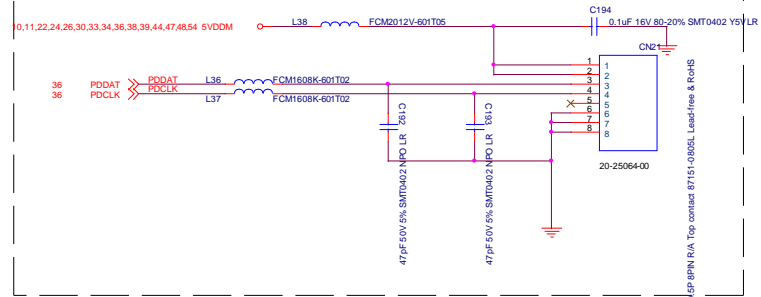
LM7R < VIA VN800 + VT8237R >		
Size	Document Number	Rev
C	<KBC M38869>	0.5
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INT KB CNN

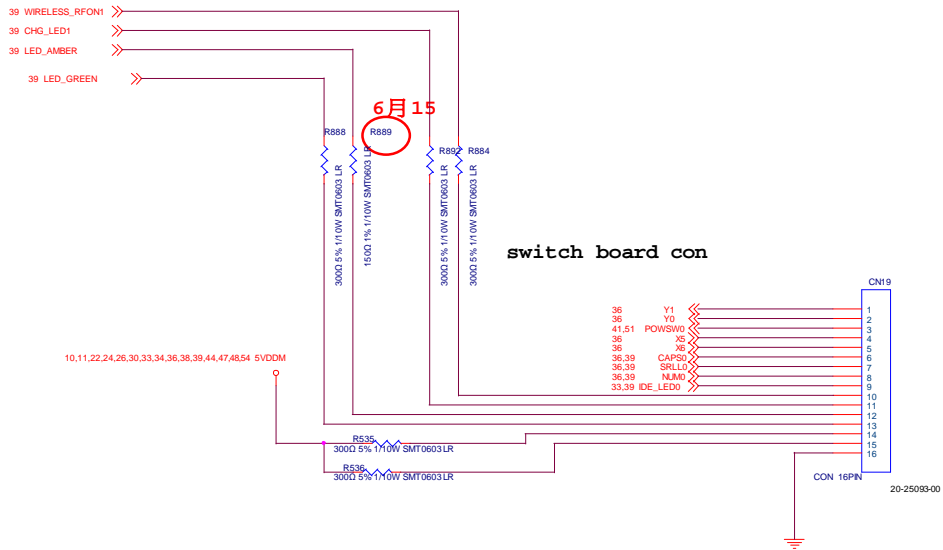


CON ACES SMT FFC 85202-2502L Lead Free & RoHS
20-25088-00

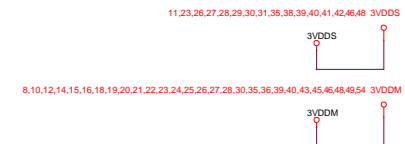
GLIDE PAD CONNECTOR



CON ACES SMT FFC 8P-8P/R/A, Top, connsd, 87151-0365L Lead-free & RoHS

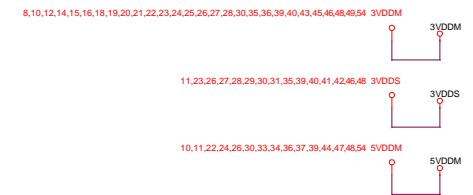
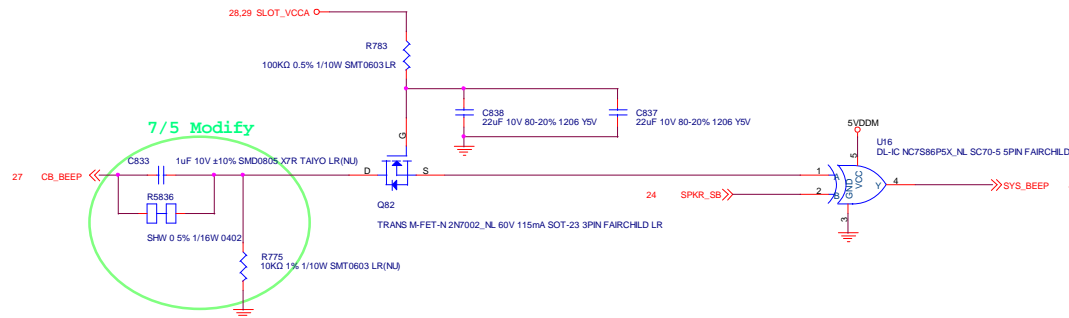
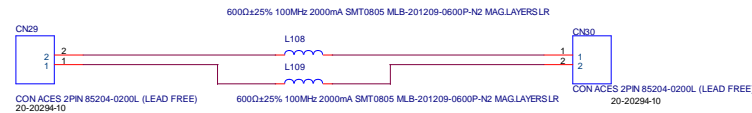
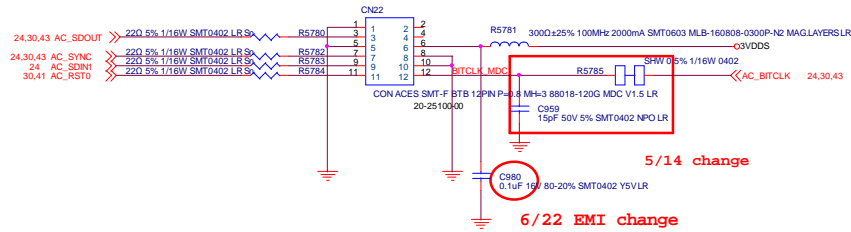


CON 16PN
20-25098-00



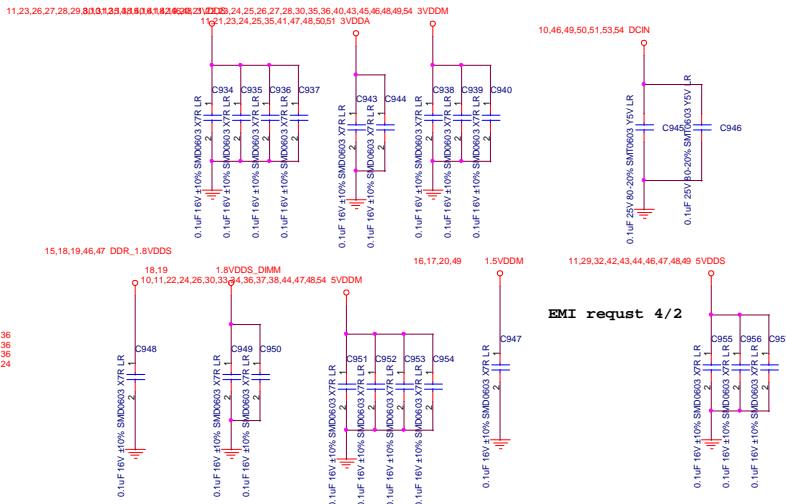
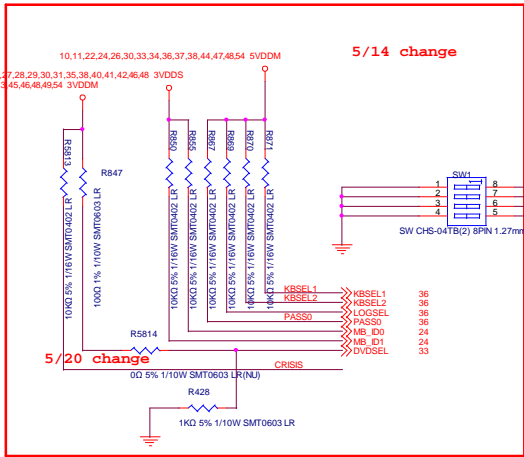
<p>First International Computer, Inc. 2/F, No.300, Yang Guang St., Neihu 114 TAIPEI, TAIWAN, R.O.C. (886-2)8751-8751</p>		
Title		
LM7R < VIA VN800 + VT8237R >		
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C	<INT KB / GP/SW CNN>	0.5
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MDC 1.5 CNN

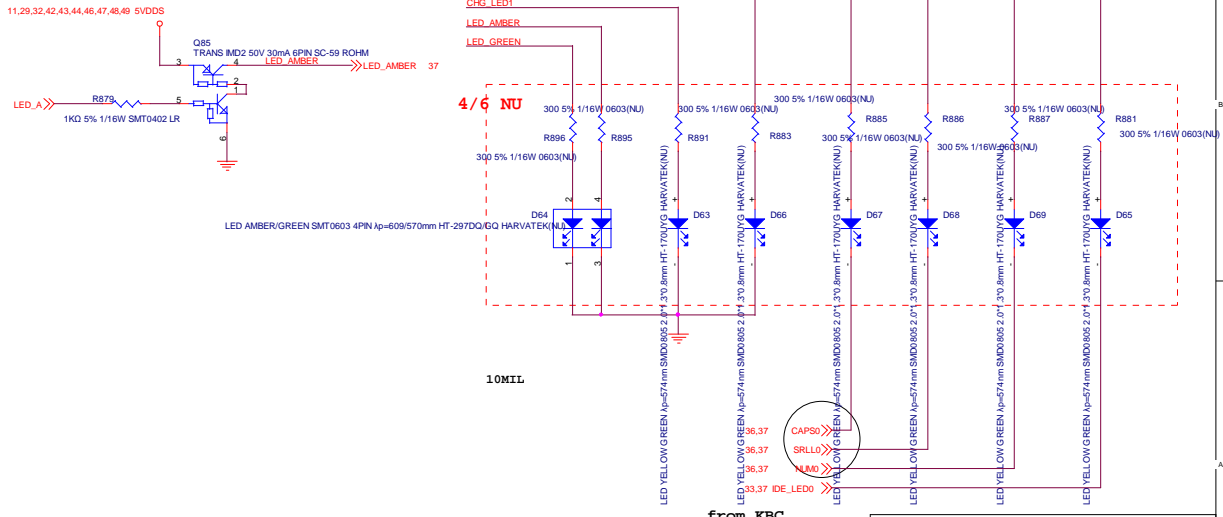
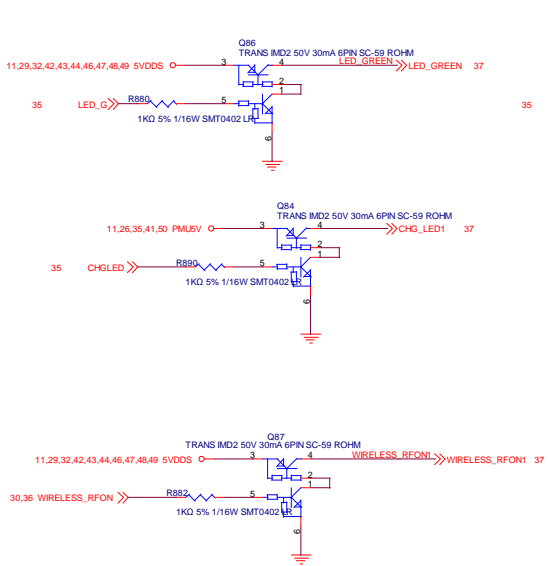


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Title		
LM7R < VIA VN800 + VT8237R >		
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C	<MDC CNN>	0.5
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DIP SWITCH



LED indicator control logic



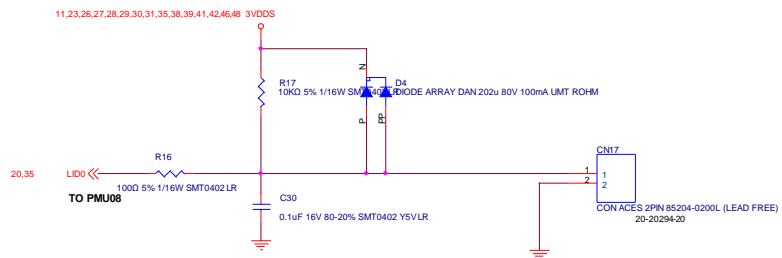
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Title: **LM7R < VIA VN800 + VT8237R >**

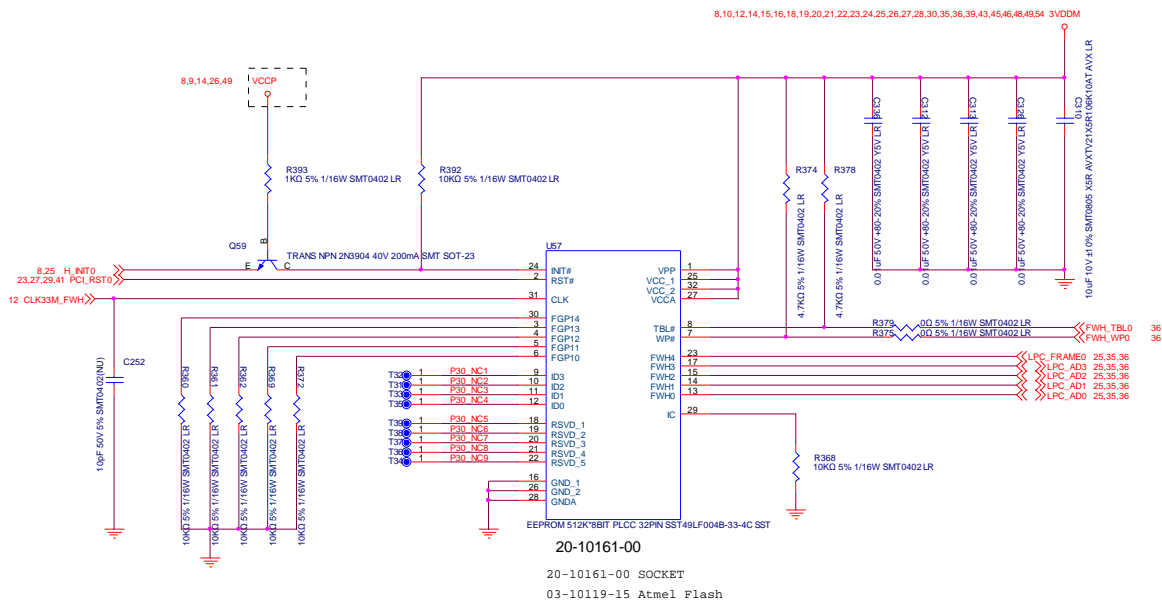
Size: C Document Number: **< DIP SW/LED >** Rev: 0.5


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LID Switch

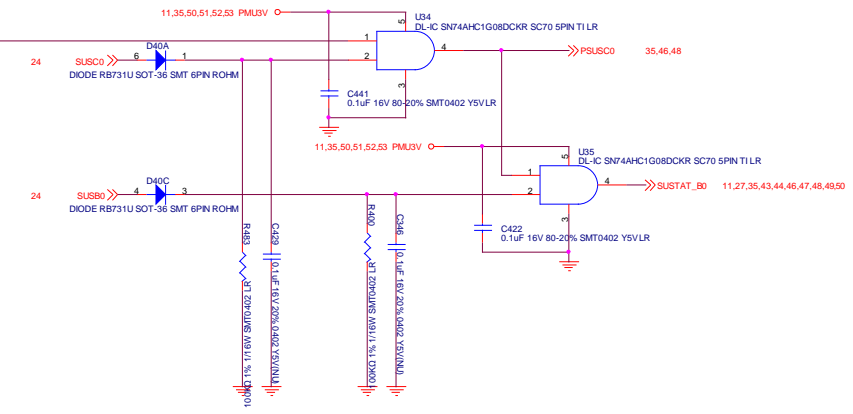
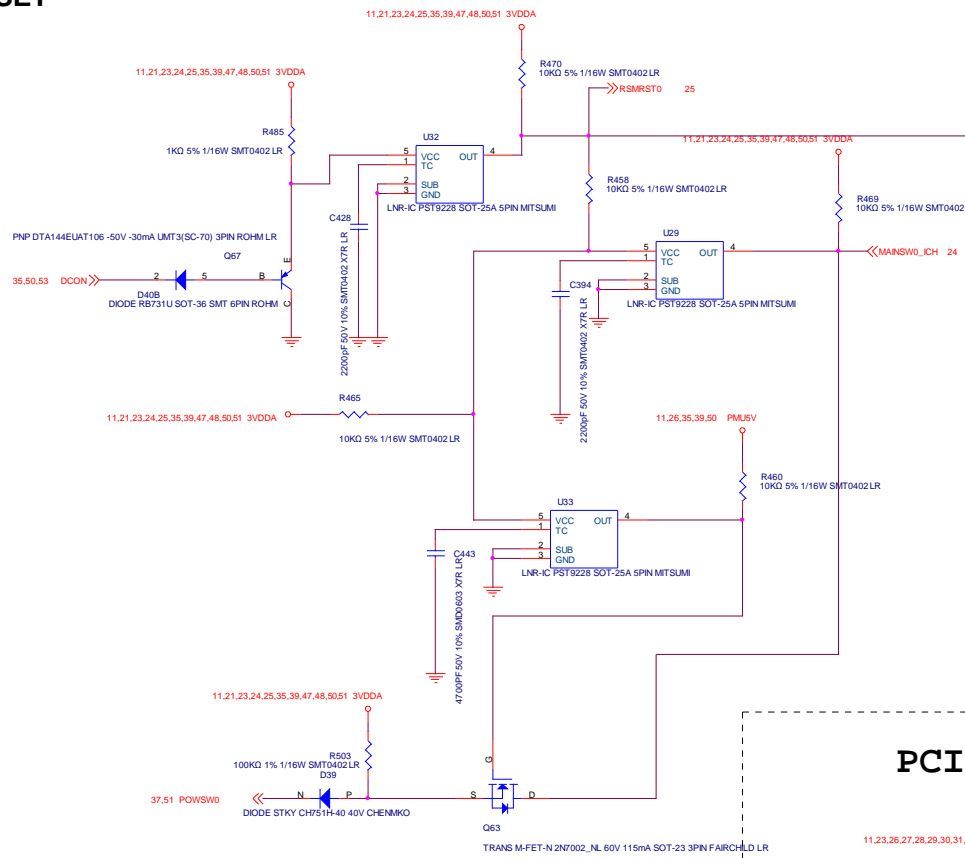


4M FLASH ROM

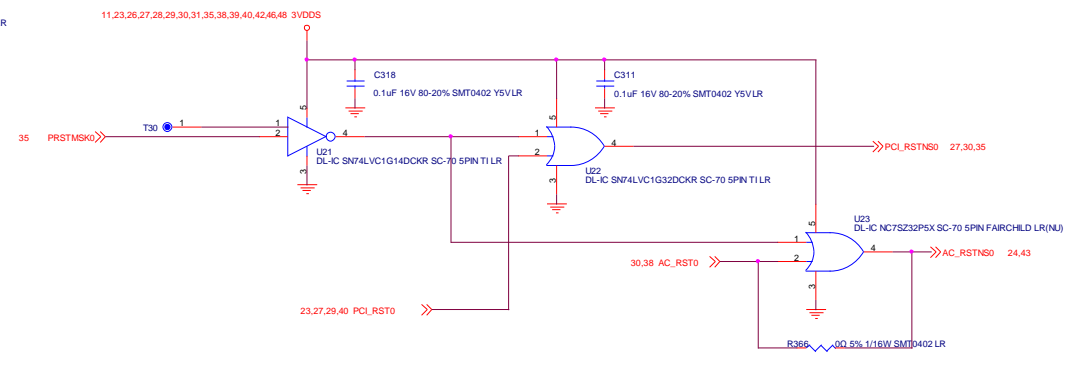


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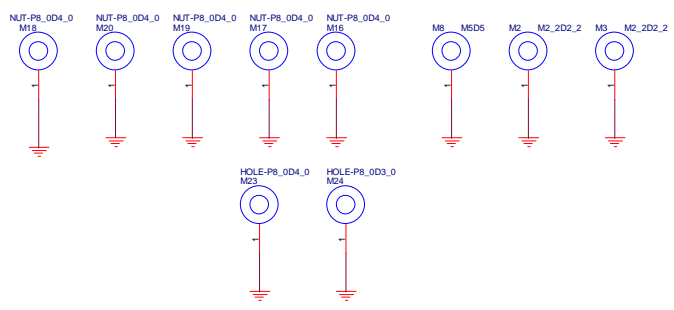
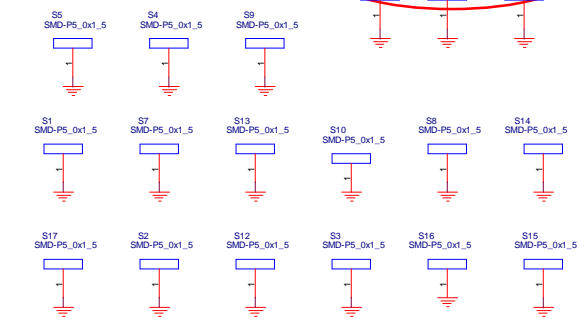
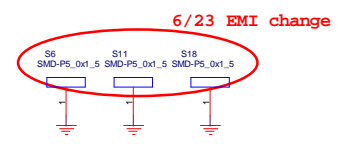
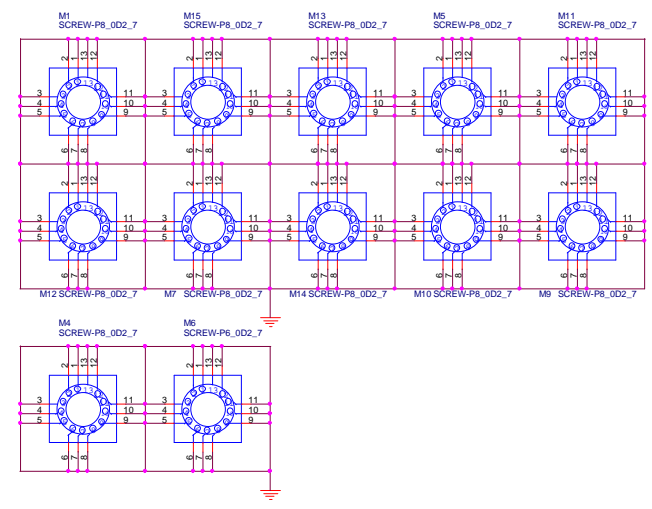
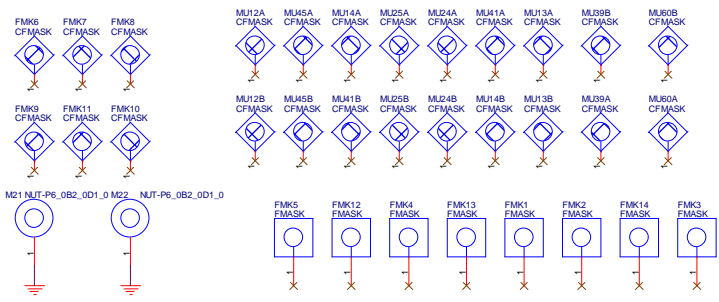
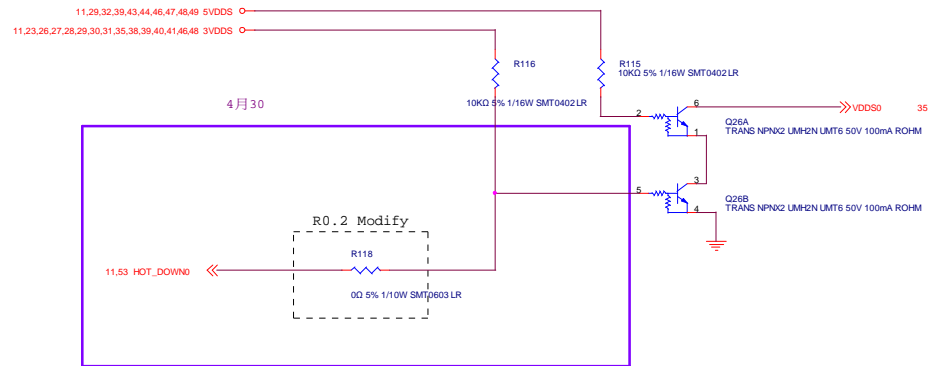
RESUME RESET



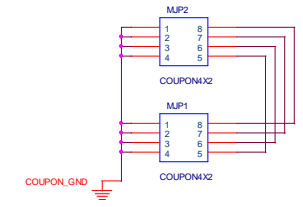
PCI RESET & PCI NON RESET



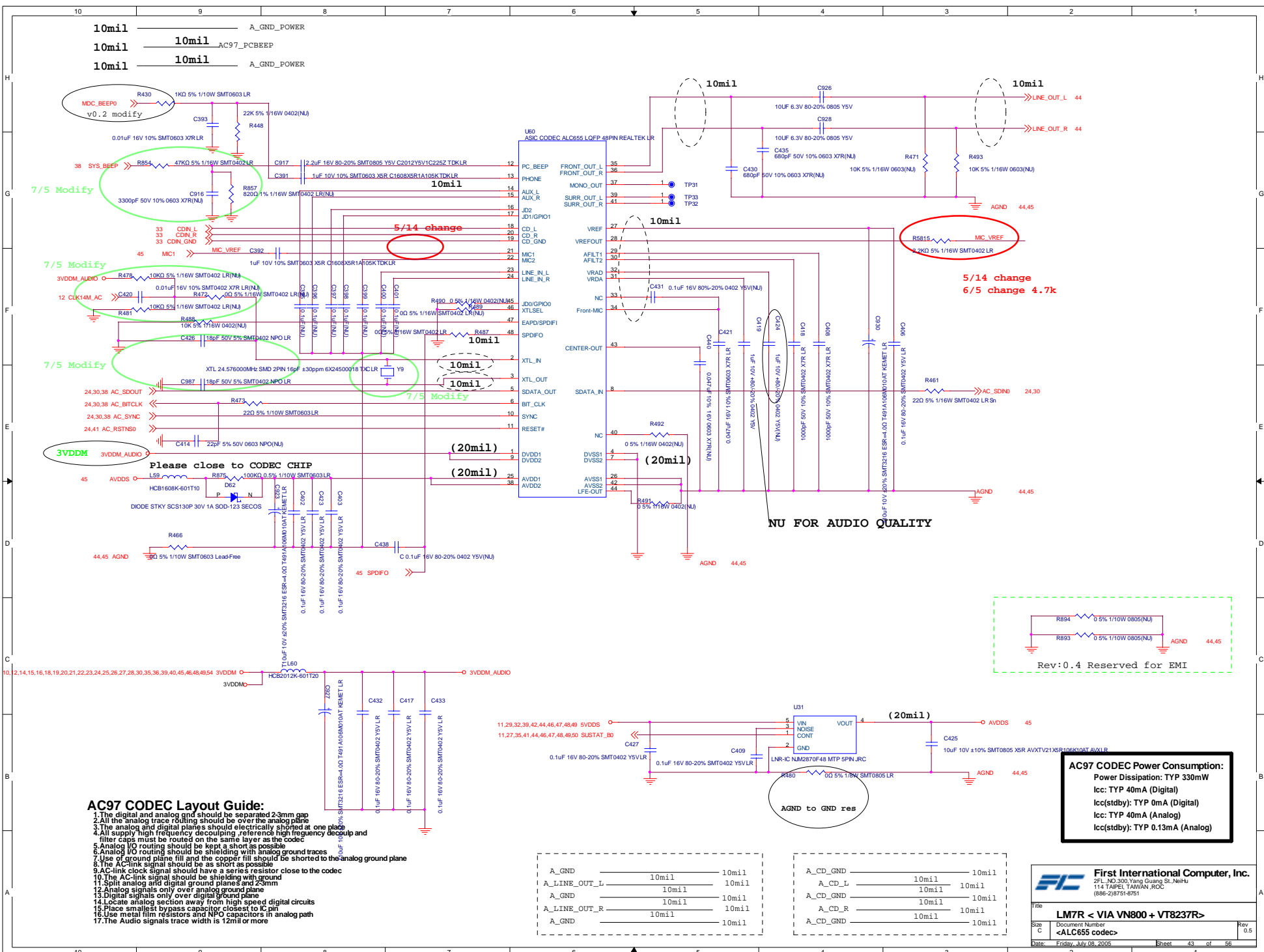
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Title		
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COUPON4X2



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AC97 CODEC Layout Guide:

- The digital and analog should be separated 2-3mm gap
- All the analog trace routing should be over the analog plane
- The analog and digital planes should be electrically shorted at one place
- All supply high frequency decoupling reference high frequency decoupling and filter caps must be routed on the same layer as the codec
- Analog I/O routing should be kept as short as possible
- Analog I/O routing should be shielding with analog ground traces
- Use of ground plane fill and the copper fill should be shorted to the analog ground plane as short as possible
- The AC-link signal should have a series resistor close to the codec
- The AC-link clock signal should have a series resistor close to the codec
- The AC-link signal should be shielding with ground
- Split analog and digital ground planes and 23mm
- Analog signals only over analog ground plane
- Digital signals only over digital ground plane
- Locate analog section away from high speed digital circuits
- Place smallest bypass capacitor closest to IC pin
- Use metal film resistors and NPO capacitors in analog path
- The Audio signals trace width is 12mil or more

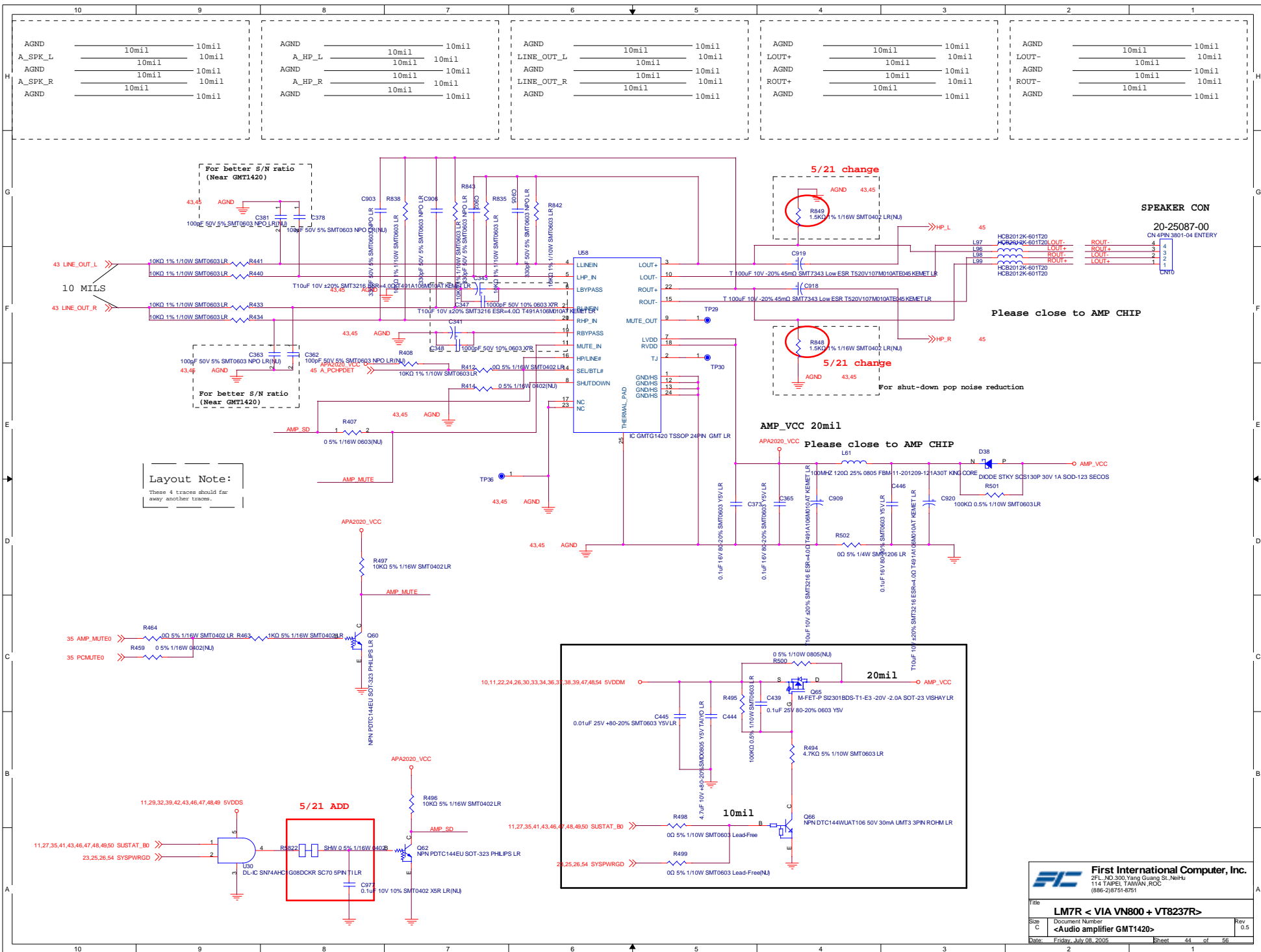
AC97 CODEC Power Consumption:
 Power Dissipation: TYP 330mW
 Icc: TYP 40mA (Digital)
 Icc(stby): TYP 0mA (Digital)
 Icc: TYP 40mA (Analog)
 Icc(stby): TYP 0.13mA (Analog)

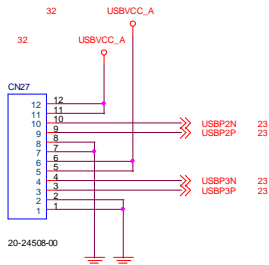
A_GND	10mil	10mil	A_CD_GND	10mil	10mil
A_LINE_OUT_L	10mil	10mil	A_CD_L	10mil	10mil
A_GND	10mil	10mil	A_CD_GND	10mil	10mil
A_GND	10mil	10mil	A_CD_R	10mil	10mil
A_LINE_OUT_R	10mil	10mil	A_CD_GND	10mil	10mil
A_GND	10mil	10mil	A_CD_GND	10mil	10mil

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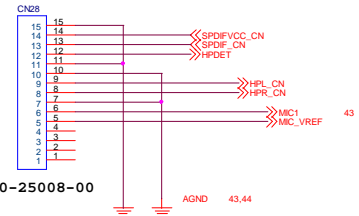
LM7R < VIA VN800 + VT8237R >
 <ALC655 codec>

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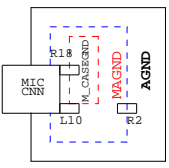




5/19 ME change, 20-24508-10 LF



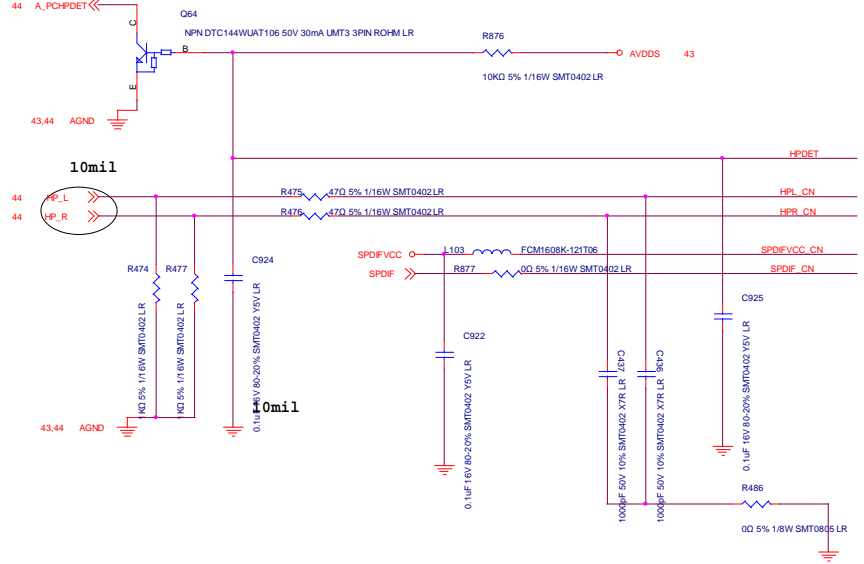
5/19 ME change, 20-25008-10 LF



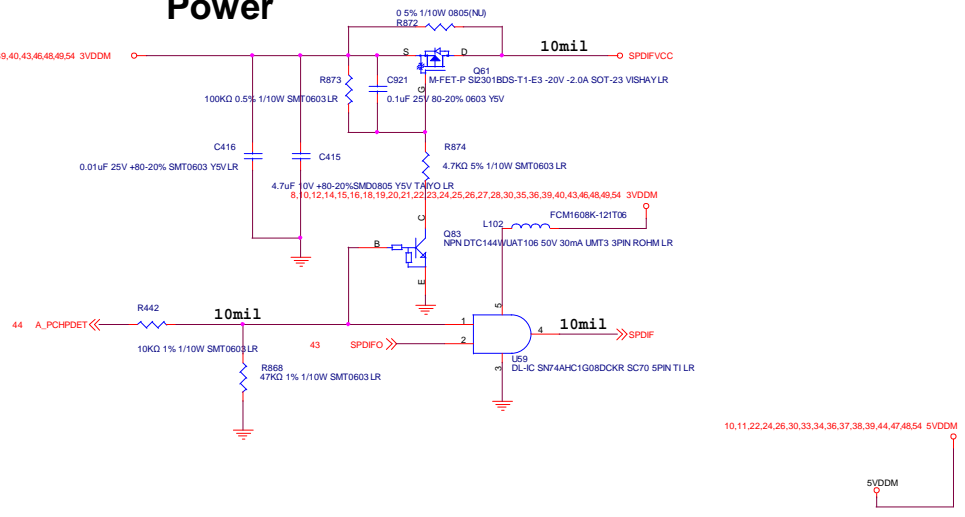
7/7 EMI change baed



Normal=LOW
Headphone insert=High

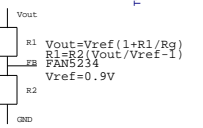
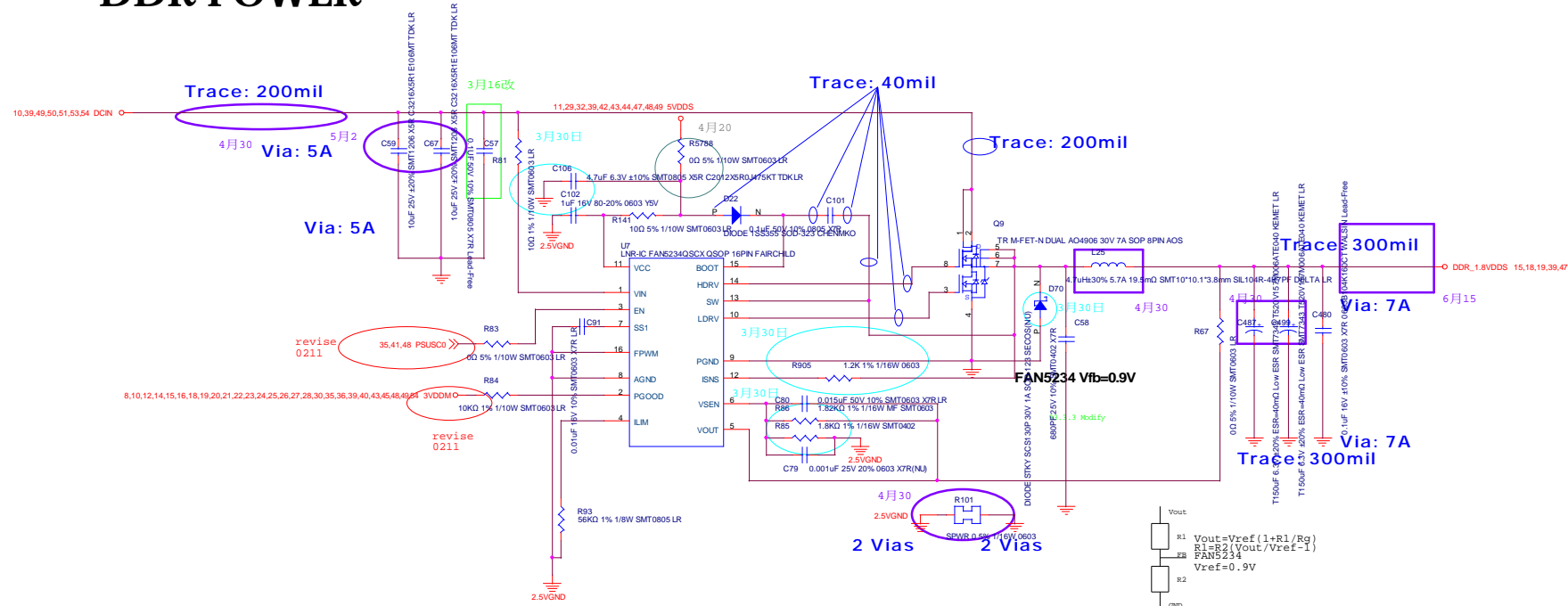


S/PDIF Power

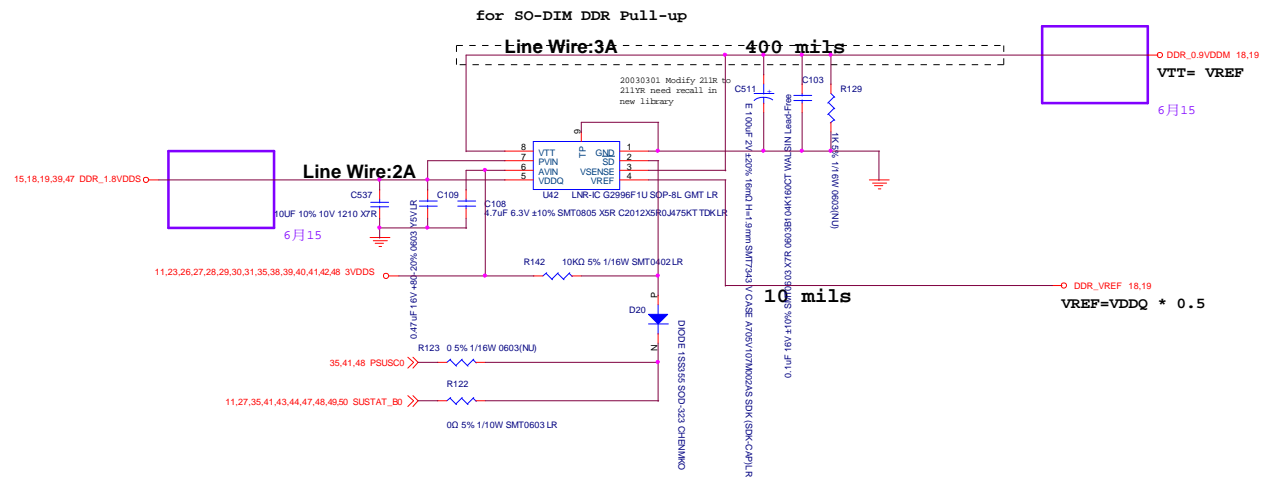


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DDR POWER



All Trace > 12mil



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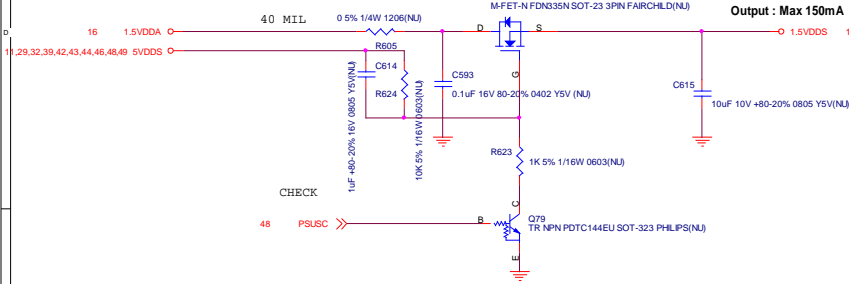
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Size: C Document Number: **<DDR2 POWER>** Rev: 0.5

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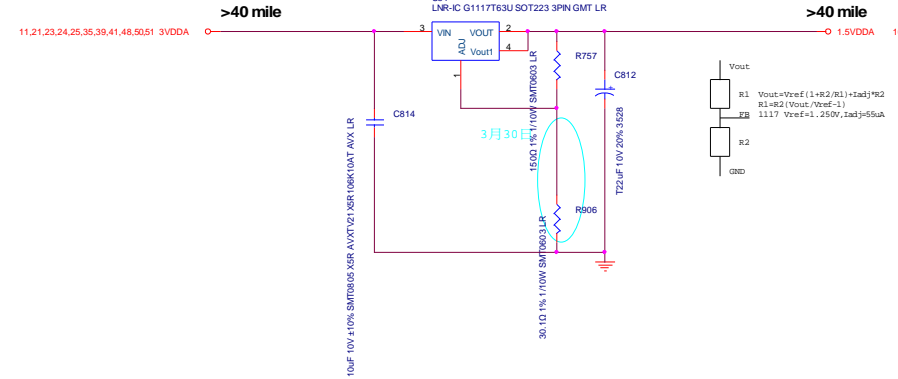
1.5VDDS 0.2A

Output : Max 150mA



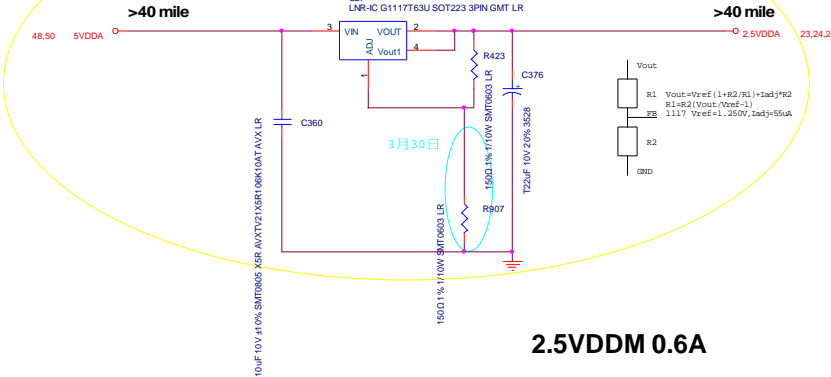
1.5VDDA 0.7A

>40 mile



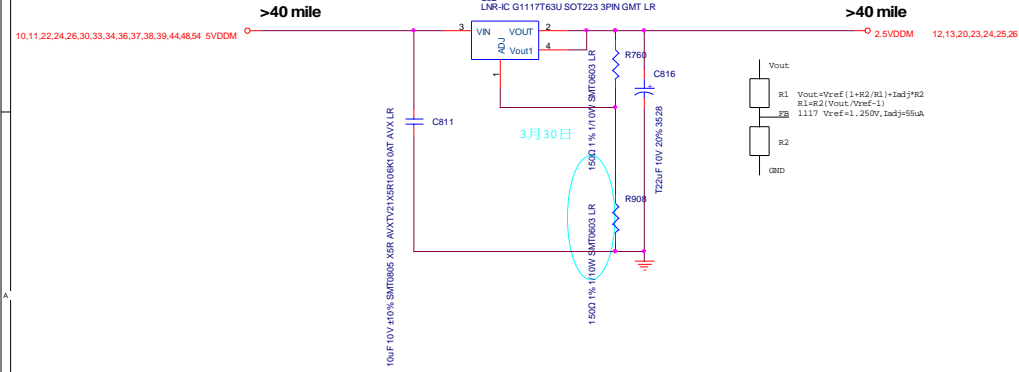
2.5VDDA 0.6A

>40 mile

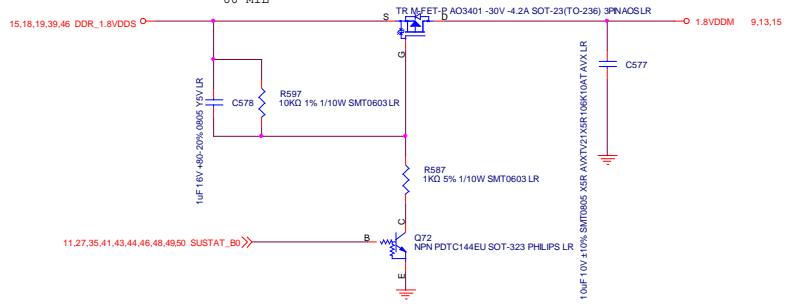


2.5VDDM 0.6A

>40 mile



1.8VDDM 1.5A

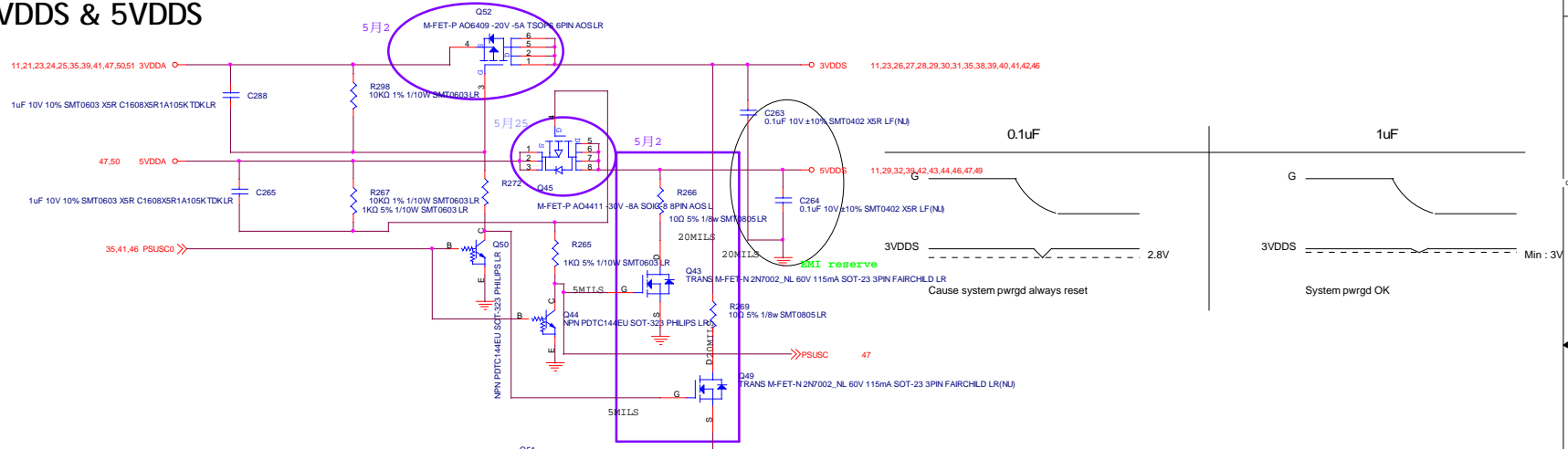


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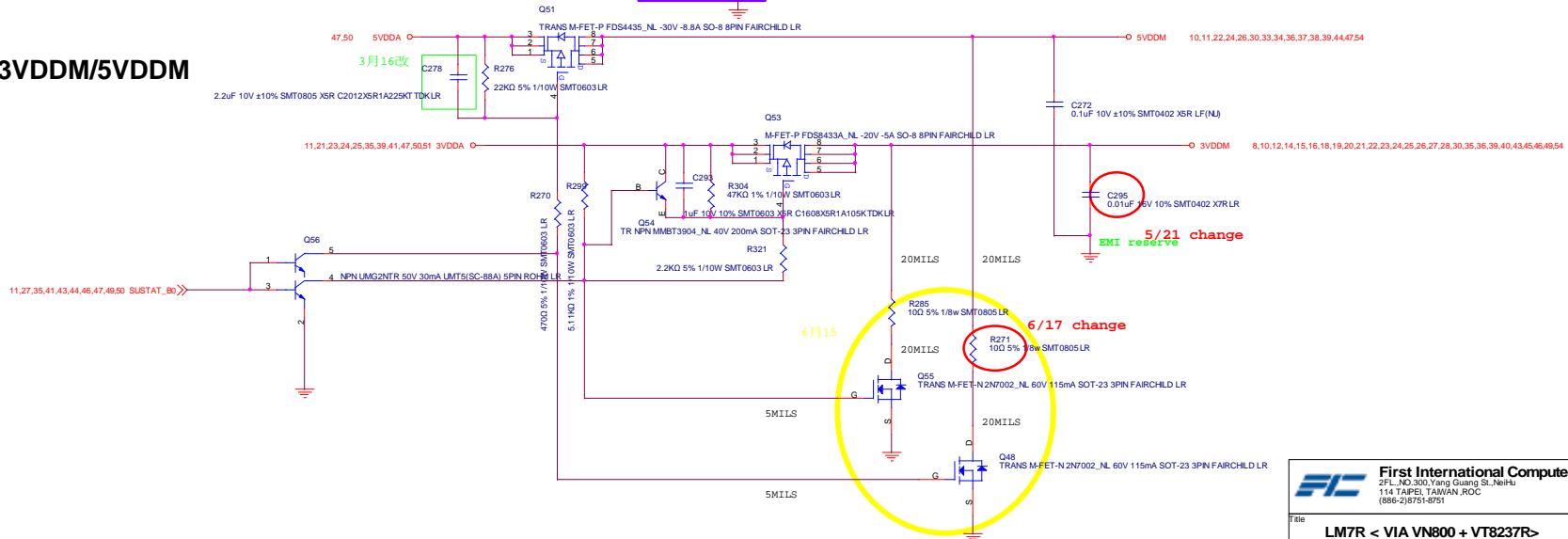
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3VDDS & 5VDDS

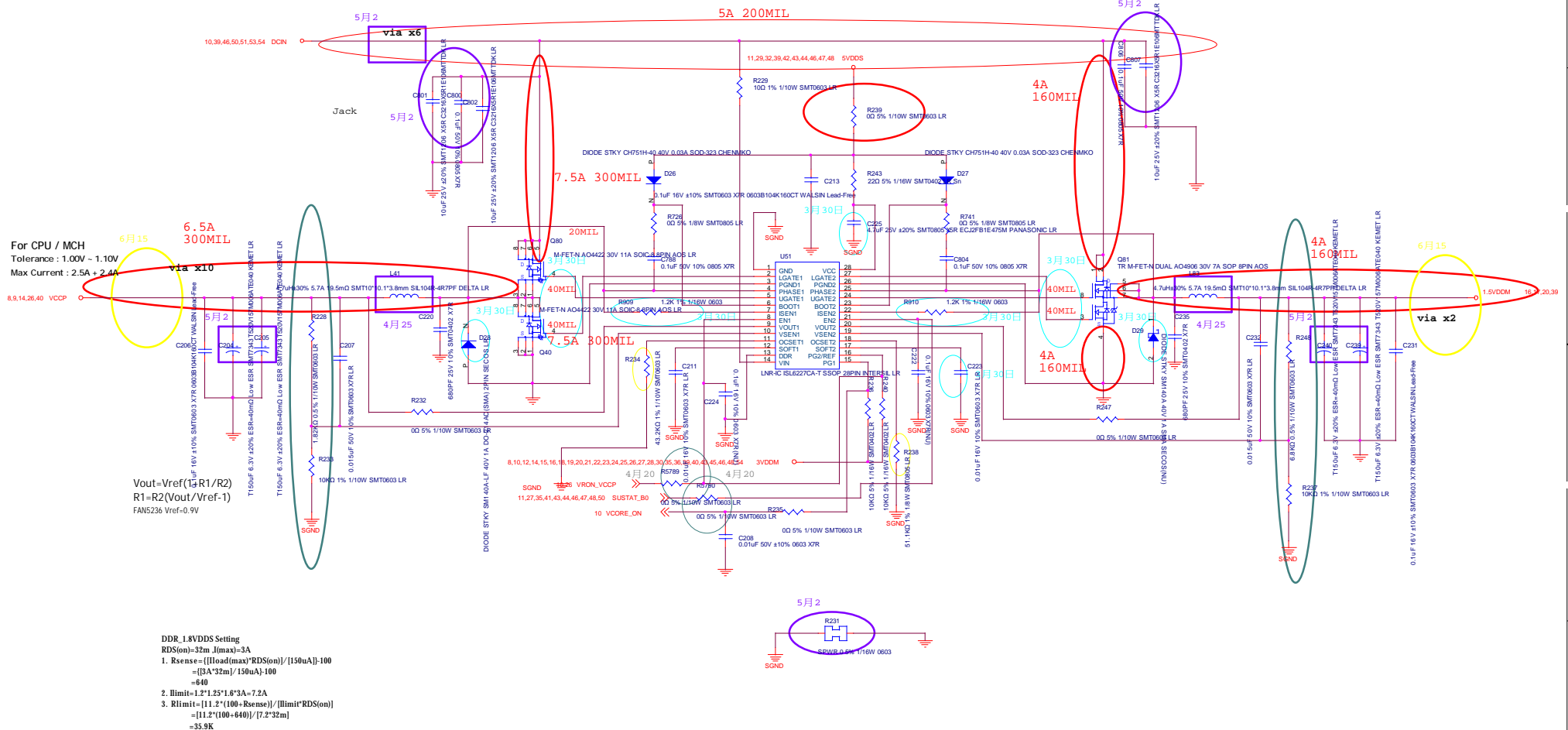


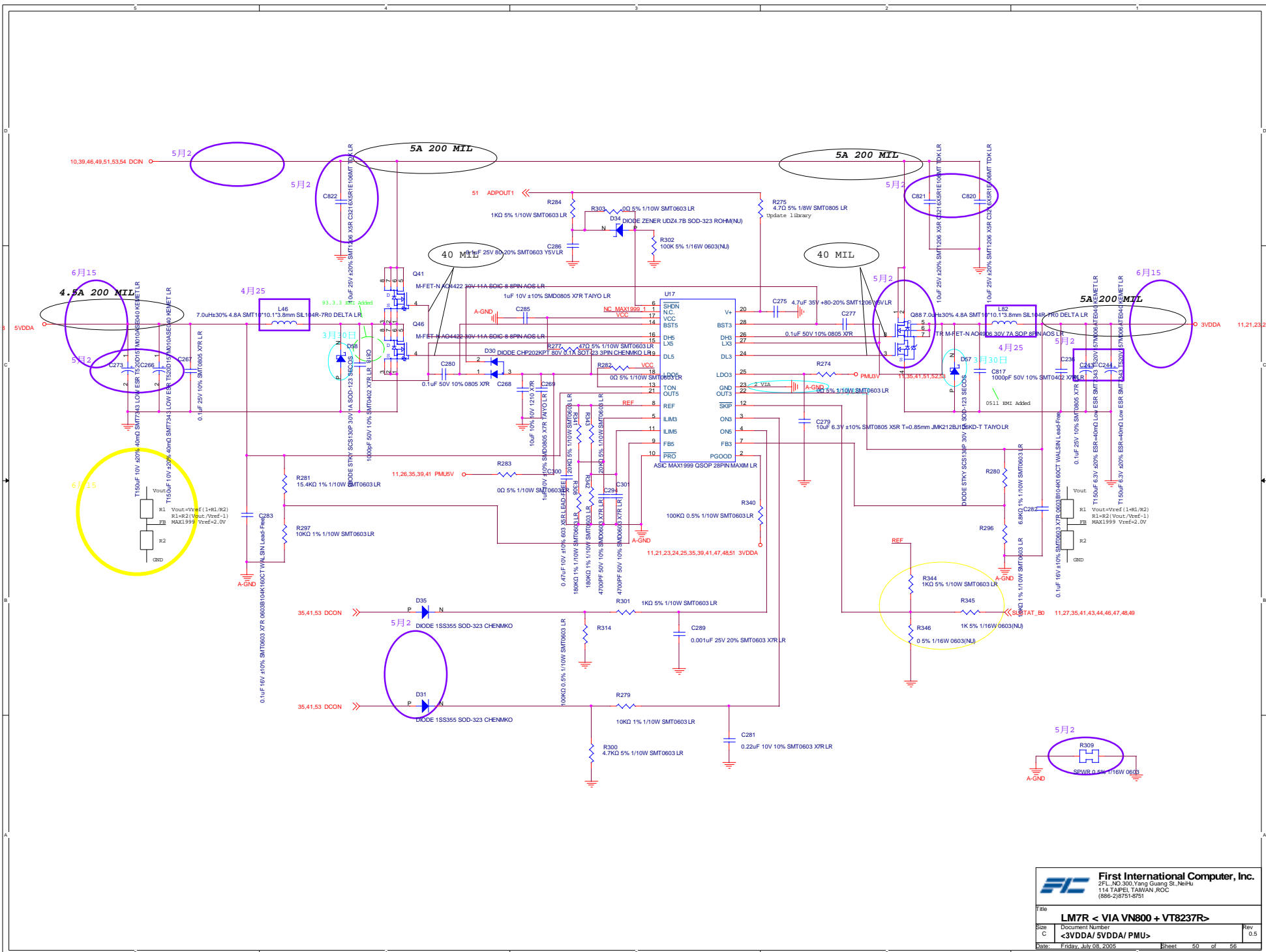
3VDDM/5VDDM



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VCCP, VORE_GMCH



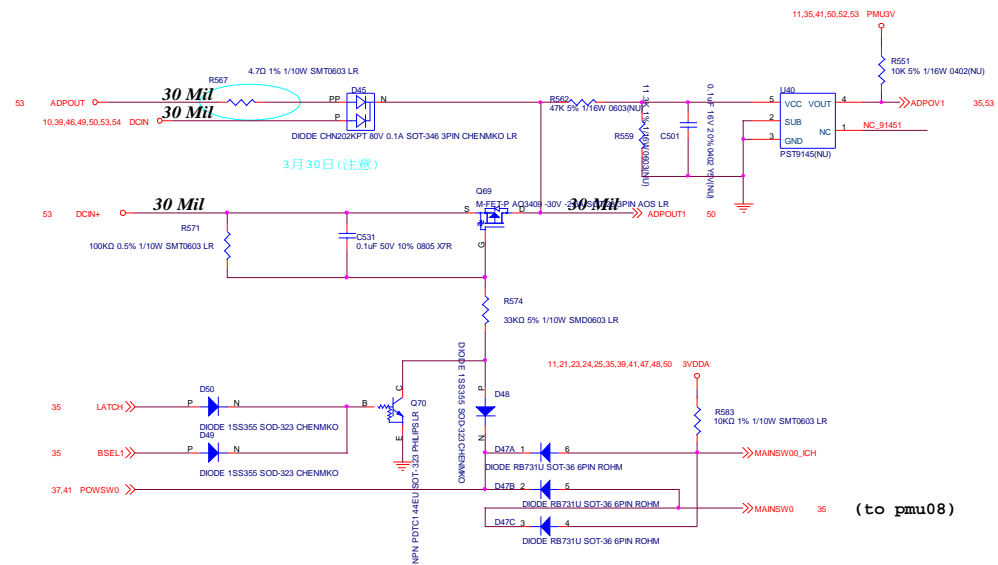


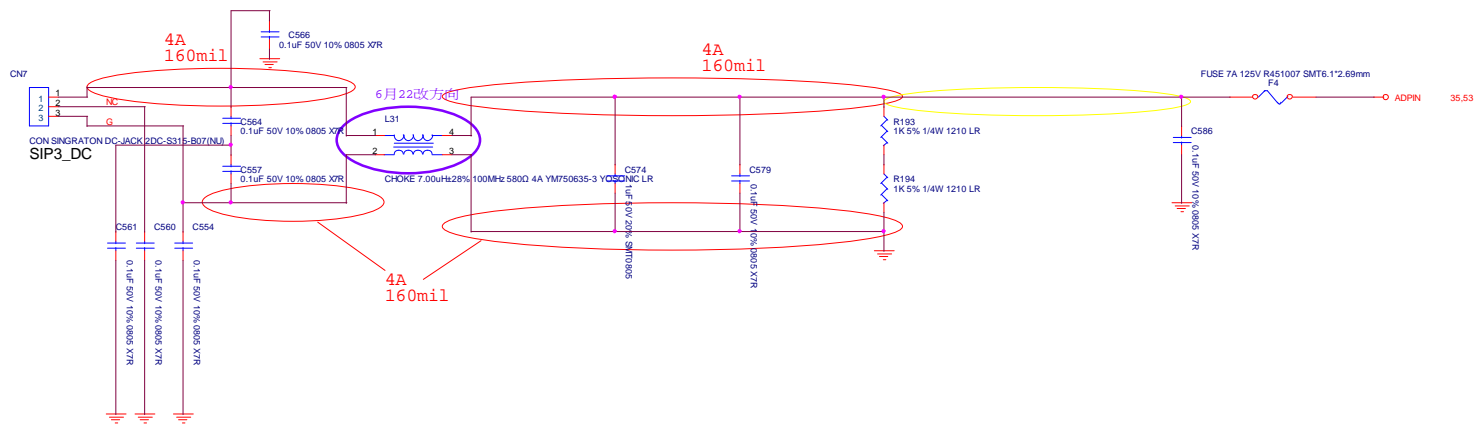
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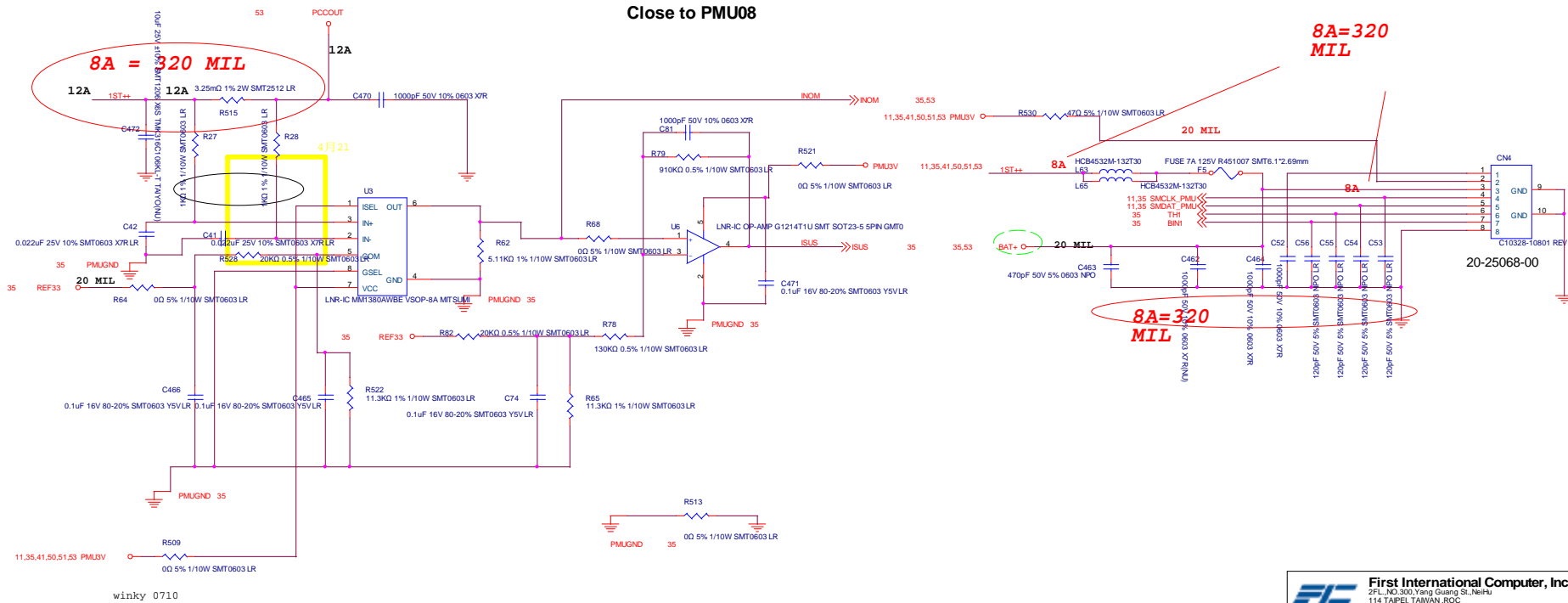
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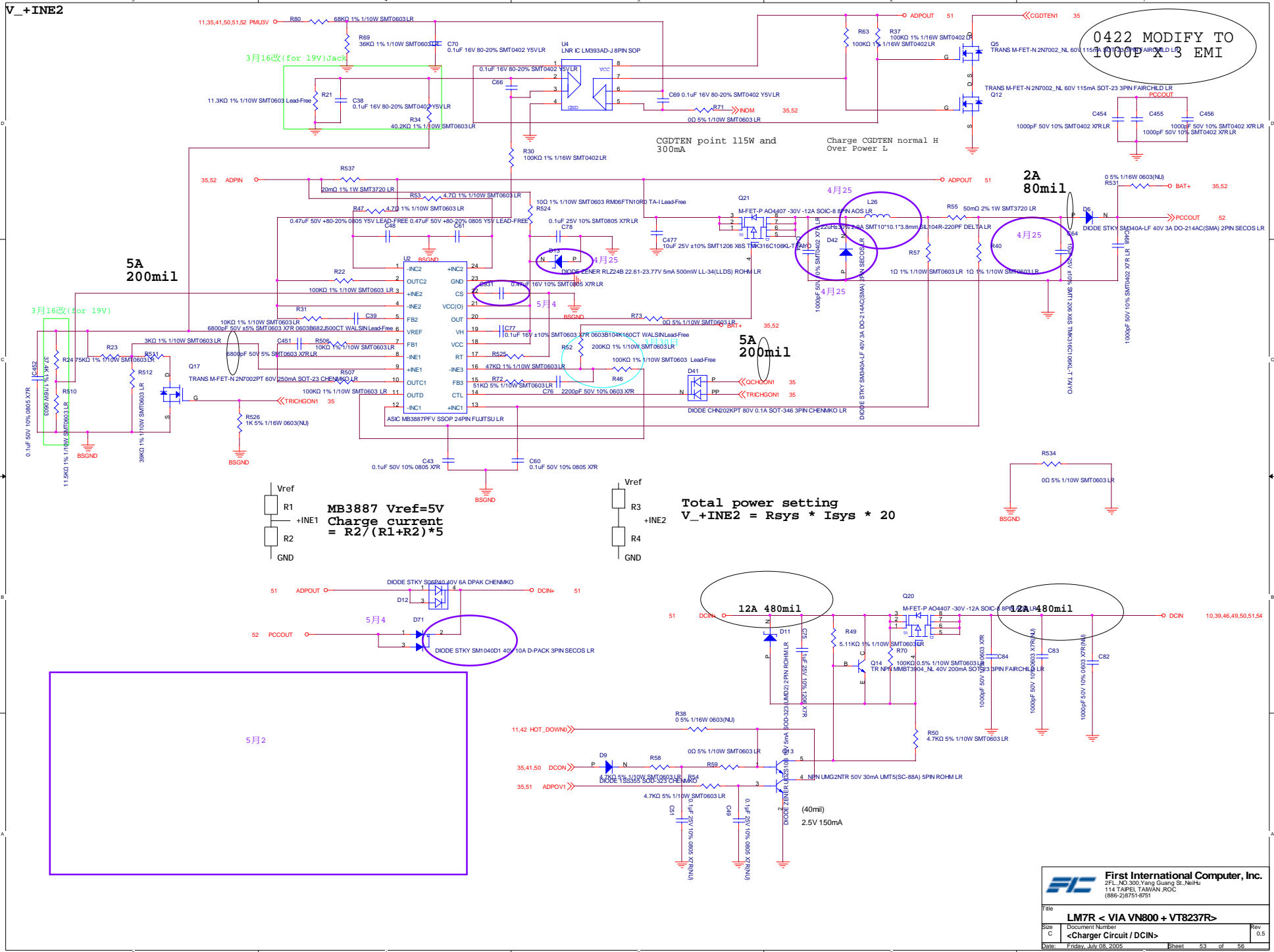


CHR BATTERY IN

Close to PMU08



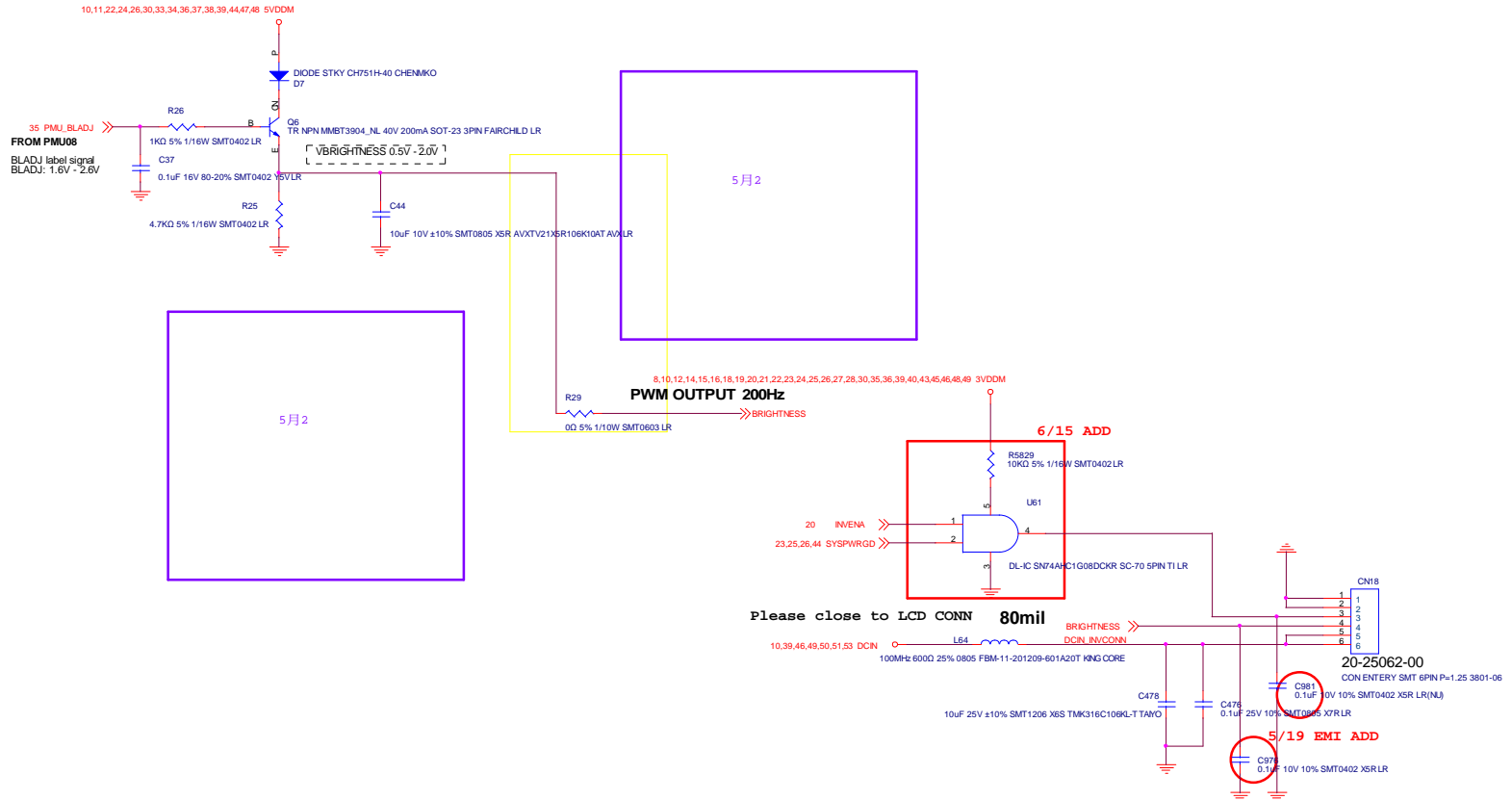
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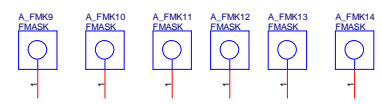
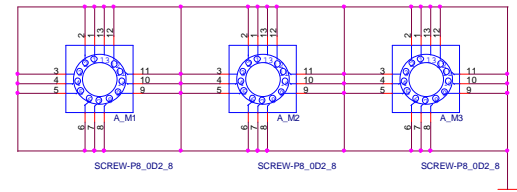
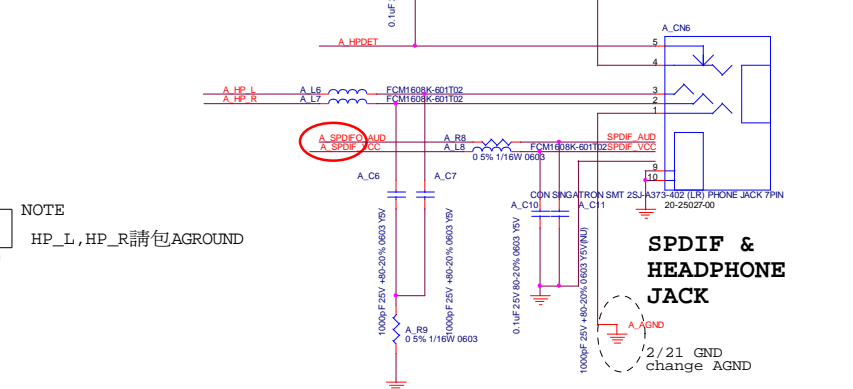
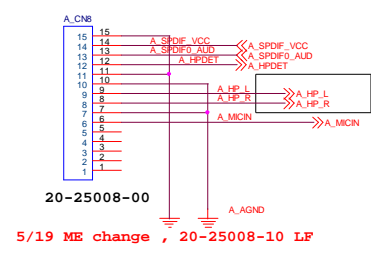
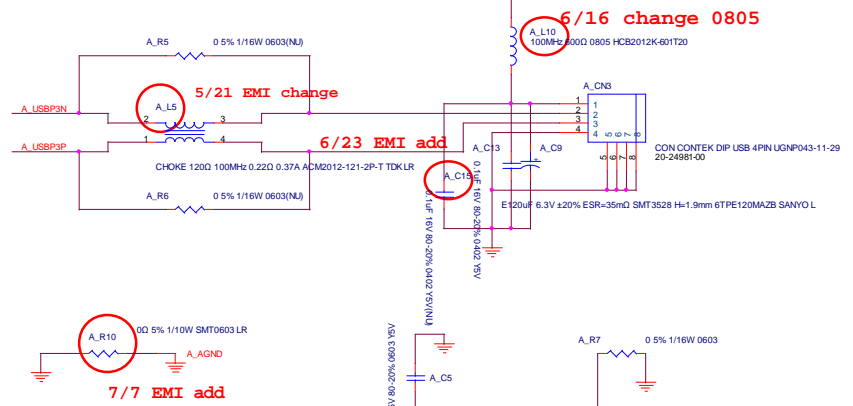
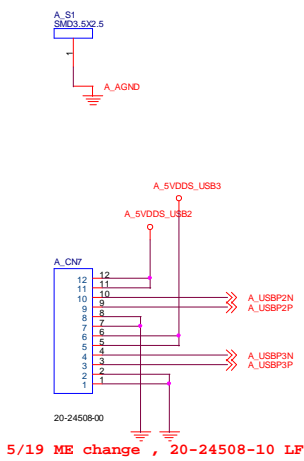
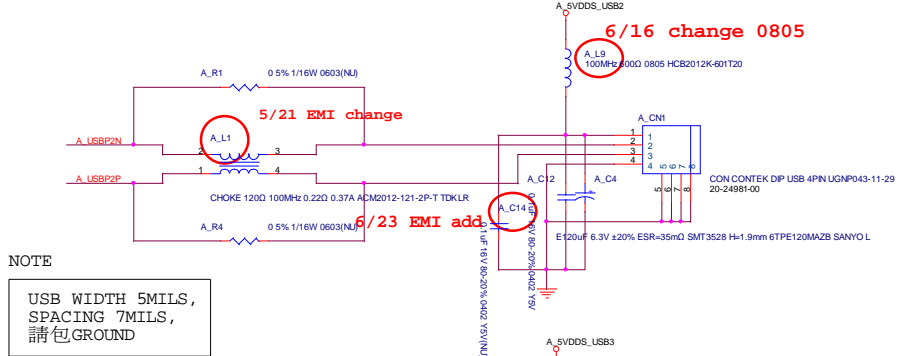
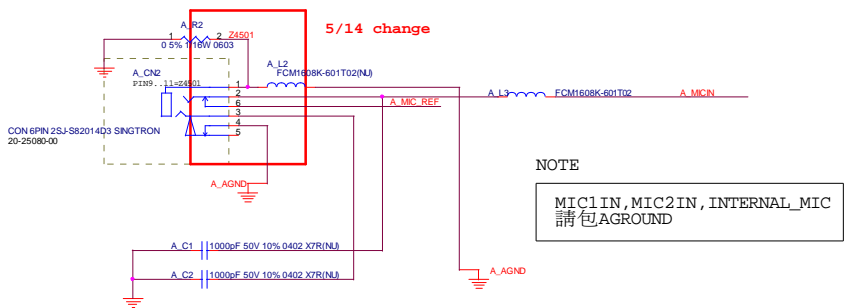
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Inverter Control

LCD brightness control



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