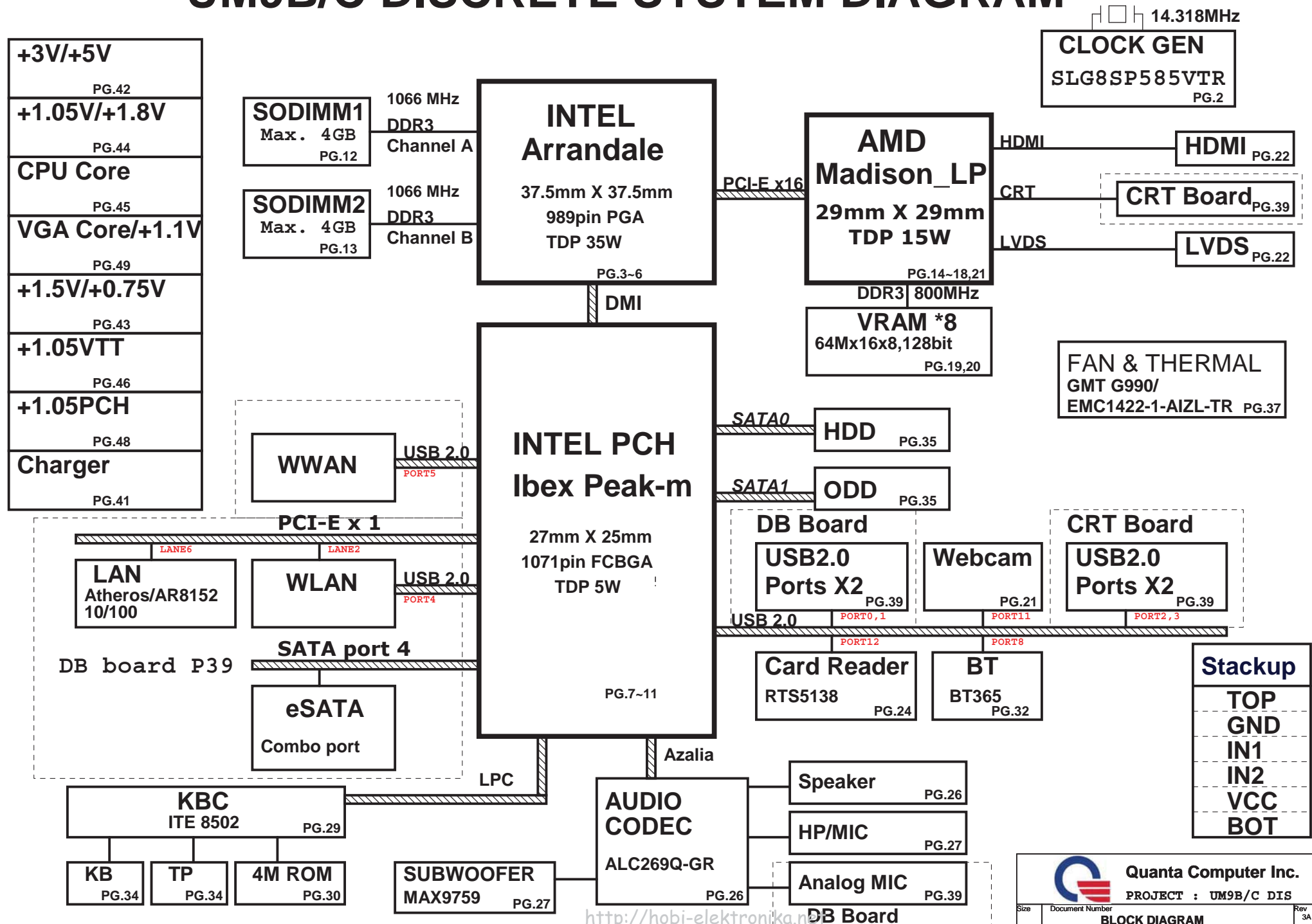



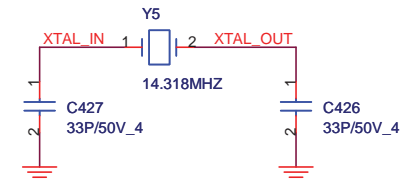
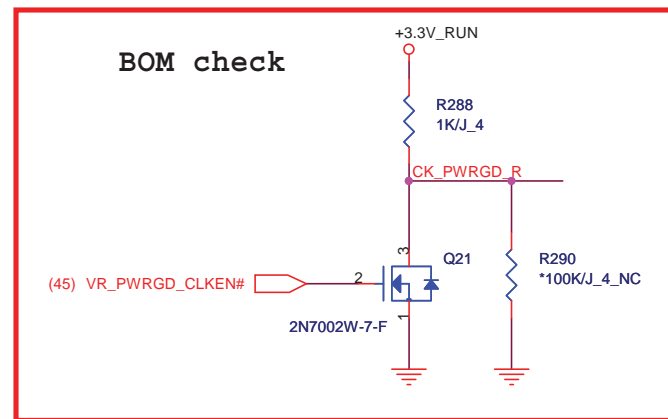
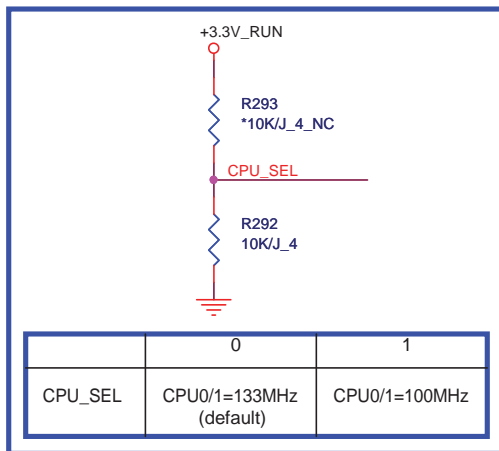
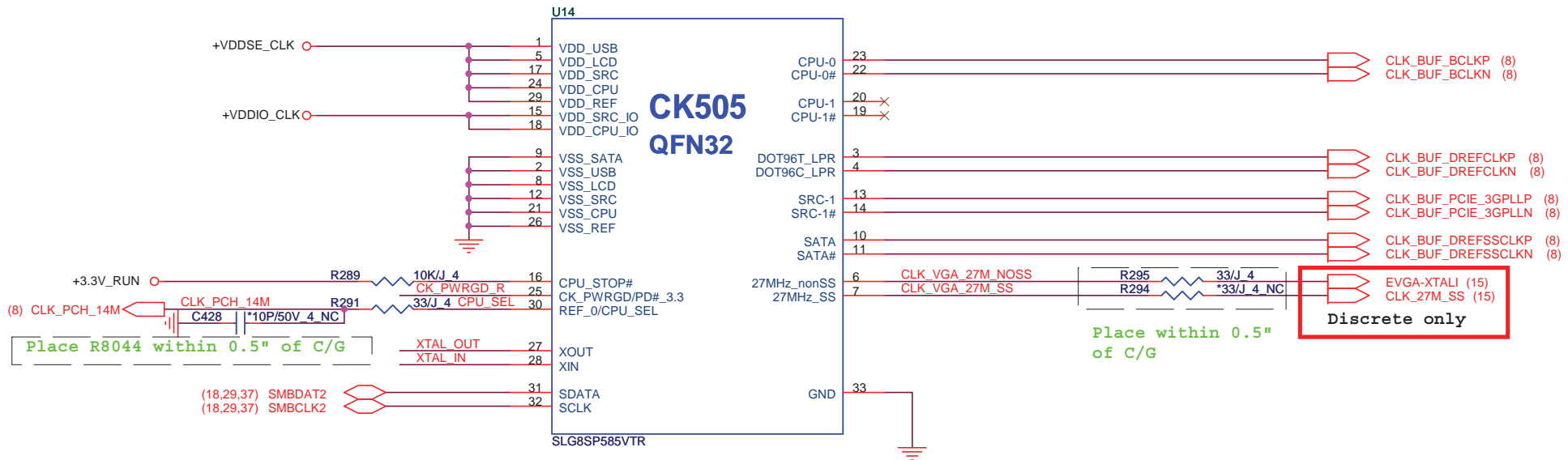
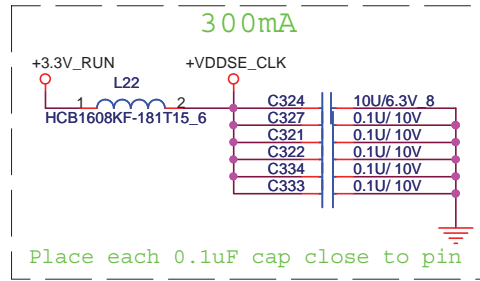
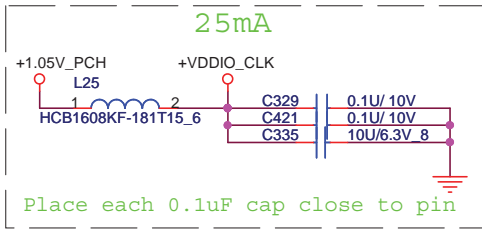
UM9B/C DISCRETE SYSTEM DIAGRAM



<http://hobi-elektronika.net>


Quanta Computer Inc.
 PROJECT : UM9B/C DIS
BLOCK DIAGRAM
 Date: Wednesday, January 27, 2010 Sheet 1 of 51 Rev 3A

PDC (Power Cap quantities follow UM3)

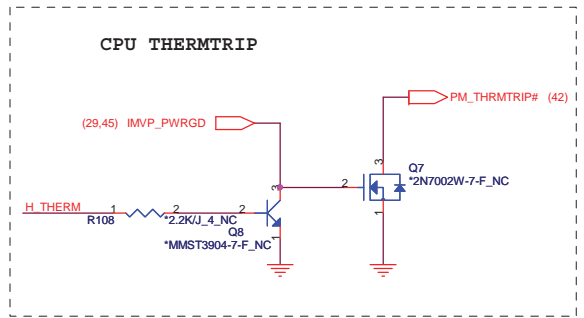
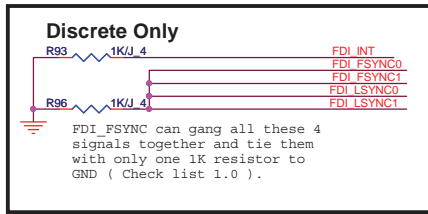
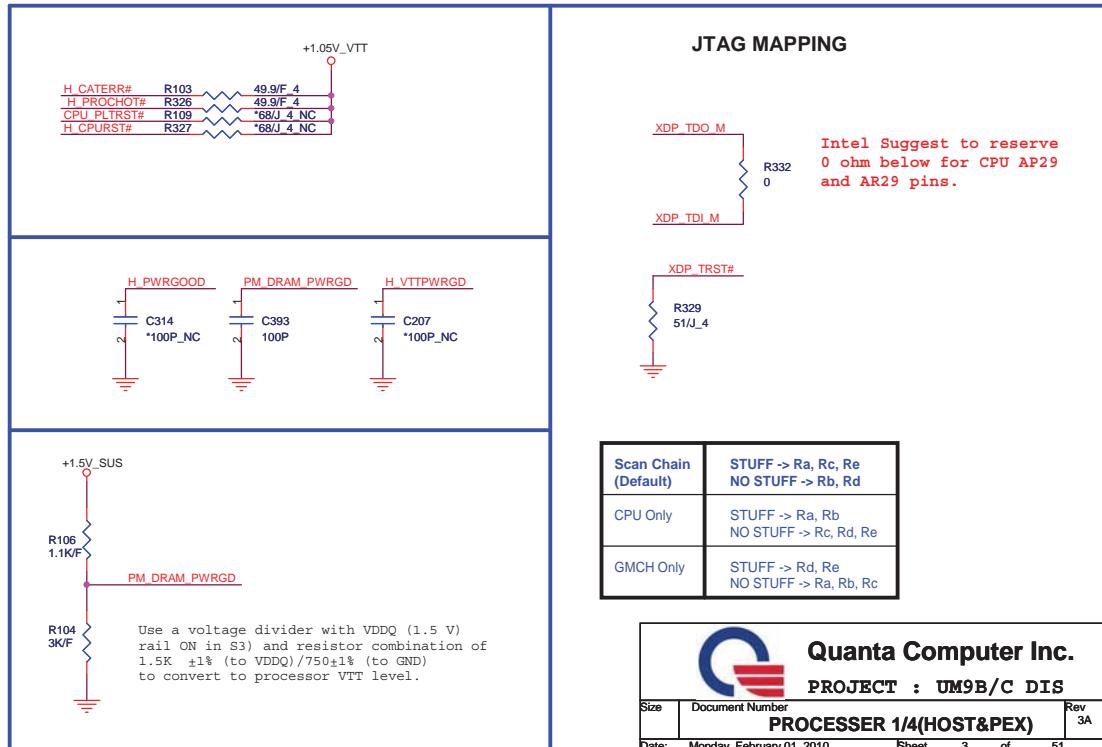
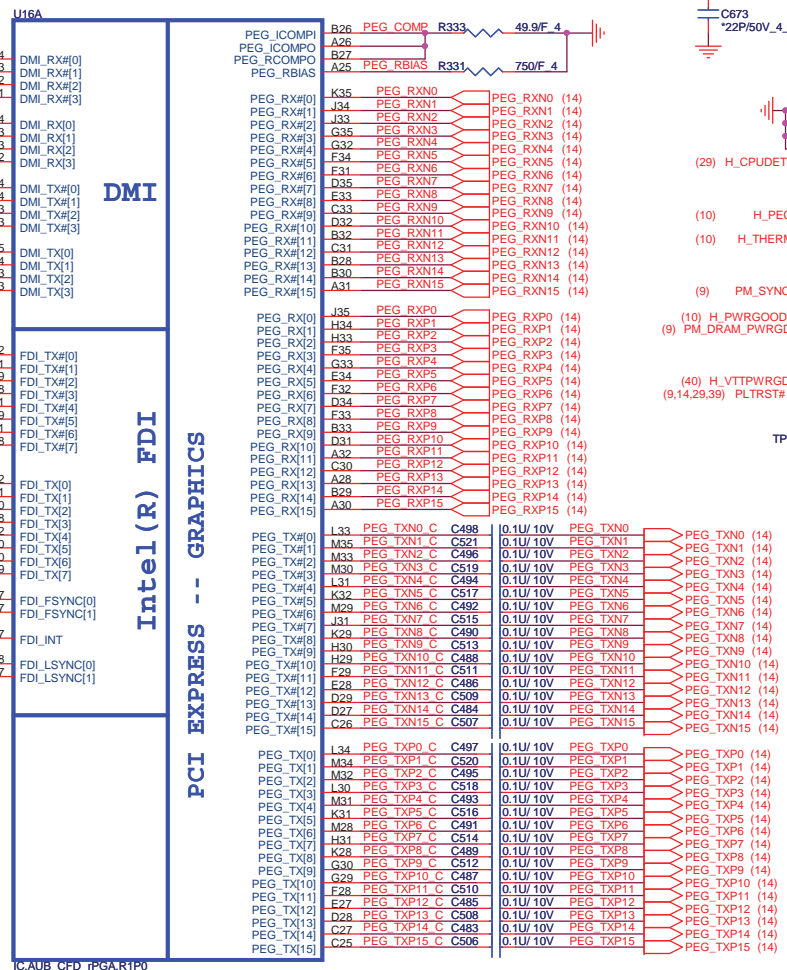


Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	Clock Gen(9LRS3197)/HOLES	3A
Date:	Monday, February 01, 2010	Sheet 2 of 51

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

DPLL_REF_SSCLK: Embedded Display Port PLL Differential Clock In. If no eDP, do we need implement these R?

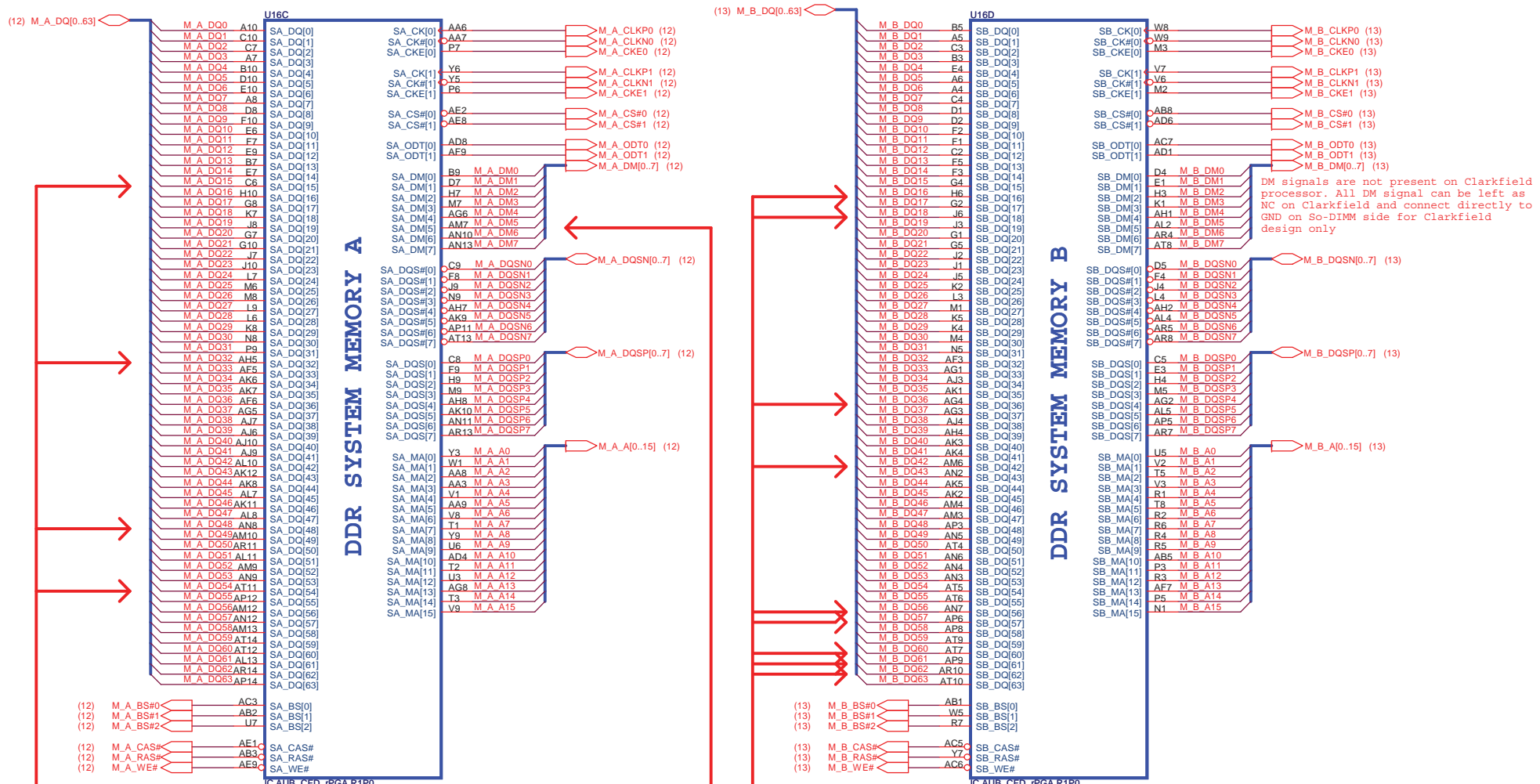


Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	PROCESSOR 1/4(HOST&PEX)	3A
Date:	Monday, February 01, 2010	Sheet 3 of 51

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

Quanta Computer Inc.
PROJECT : UM9B/C DIS

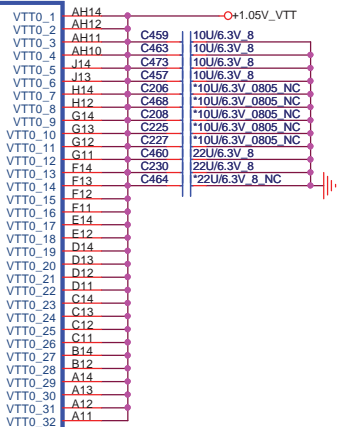
Size	Document Number	Rev
	PROCESSOR 2/4(DDR)	3A
Date:	Monday, February 01, 2010	Sheet 4 of 51

Name different with power

C477	*22U/6.3V 8 NC	AG35	VCC1
C479	*22U/6.3V 8 NC	AG34	VCC2
C501	*22U/6.3V 8 NC	AG32	VCC3
C472	*22U/6.3V 8 NC	AG31	VCC4
C203	*22U/6.3V 8 NC	AG30	VCC6
C202	22U/6.3V 8	AG29	VCC7
C470	22U/6.3V 8	AG27	VCC8
C469	22U/6.3V 8	AG26	VCC9
C499	22U/6.3V 8	AG26	VCC10
C214	22U/6.3V 8	AF35	VCC11
C204	22U/6.3V 8	AF34	VCC12
C504	22U/6.3V 8	AF32	VCC13
C500	*10U/6.3V 8 NC	AF33	VCC14
C200	*10U/6.3V 8 NC	AF31	VCC15
C205	*10U/6.3V 8 NC	AF30	VCC16
C476	*10U/6.3V 8 NC	AF29	VCC17
C213	10U/6.3V 8	AF28	VCC18
C201	10U/6.3V 8	AF27	VCC19
C478	10U/6.3V 8	AF26	VCC119
C217	10U/6.3V 8	AD35	VCC20
C219	10U/6.3V 8	AD34	VCC21
C471	10U/6.3V 8	AD33	VCC22
C218	10U/6.3V 8	AD32	VCC23
C503	10U/6.3V 8	AD31	VCC24
C475	10U/6.3V 8	AD30	VCC25
C215	10U/6.3V 8	AD29	VCC26
C502	10U/6.3V 8	AD28	VCC28
C216	10U/6.3V 8	AD27	VCC29
C196	*470U NC	AD26	VCC30
C191	*470U NC	AC34	VCC31
		AC33	VCC32
		AC32	VCC33
		AC31	VCC35
		AC30	VCC36
		AC29	VCC37
		AC28	VCC38
		AC27	VCC39
		AC26	VCC40
		AA35	VCC41
		AA34	VCC42
		AA33	VCC43
		AA32	VCC44
		AA31	VCC45
		AA30	VCC46
		AA29	VCC47
		AA28	VCC48
		AA27	VCC49
		AA26	VCC50
		Y35	VCC51
		Y34	VCC52
		Y33	VCC53
		Y32	VCC54
		Y31	VCC55
		Y30	VCC56
		Y29	VCC57
		Y28	VCC58
		Y27	VCC59
		Y26	VCC60
		Y35	VCC61
		Y34	VCC62
		Y33	VCC63
		Y32	VCC64
		Y31	VCC65
		Y30	VCC66
		Y29	VCC67
		Y28	VCC68
		Y27	VCC69
		Y26	VCC70
		U34	VCC71
		U33	VCC72
		U32	VCC73
		U31	VCC74
		U30	VCC75
		U29	VCC76
		U28	VCC77
		U27	VCC78
		U26	VCC79
		U25	VCC80
		R35	VCC81
		R34	VCC82
		R33	VCC83
		R32	VCC84
		R31	VCC85
		R30	VCC86
		R29	VCC87
		R28	VCC88
		R27	VCC89
		R26	VCC90
		P35	VCC91
		P34	VCC92
		P33	VCC93
		P32	VCC94
		P31	VCC95
		P30	VCC96
		P29	VCC97
		P27	VCC98
		P26	VCC99
		P25	VCC100

IC:AUB_CFD_PGAR1P0

18A



VTT Rail Values are Auburndal VTT=1.05V Clarkfield VTT=1.1V

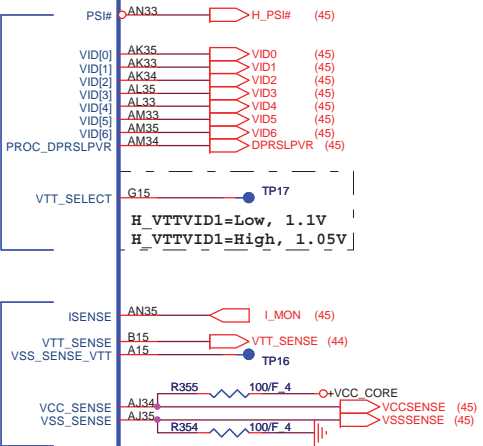
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

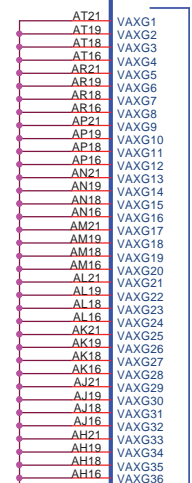
SENSE LINES



H_VTTVID1=Low, 1.1V H_VTTVID1=High, 1.05V

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

U16G



GRAPHICS

POWER

FDI

PEG & DMI

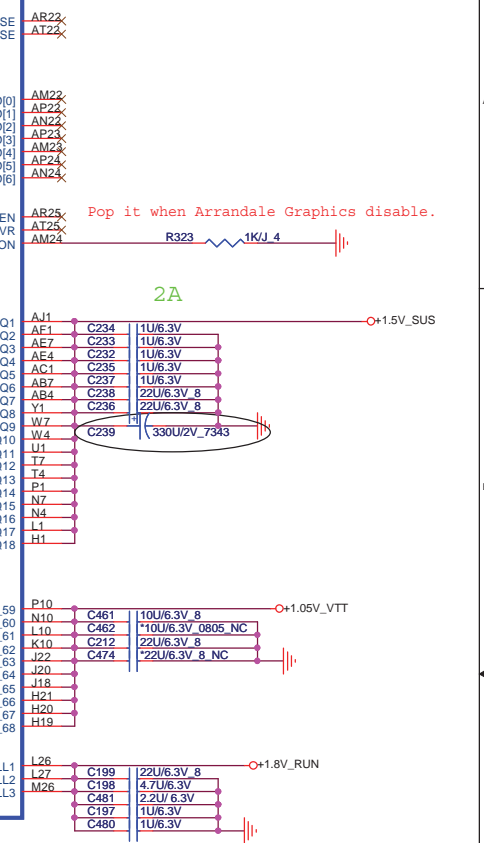
SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

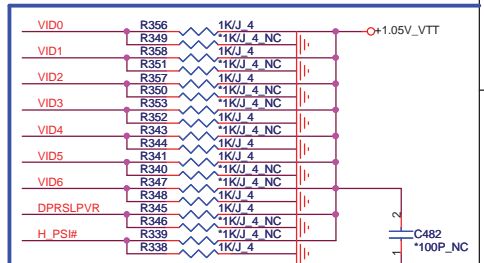
1.1V

1.8V



2A

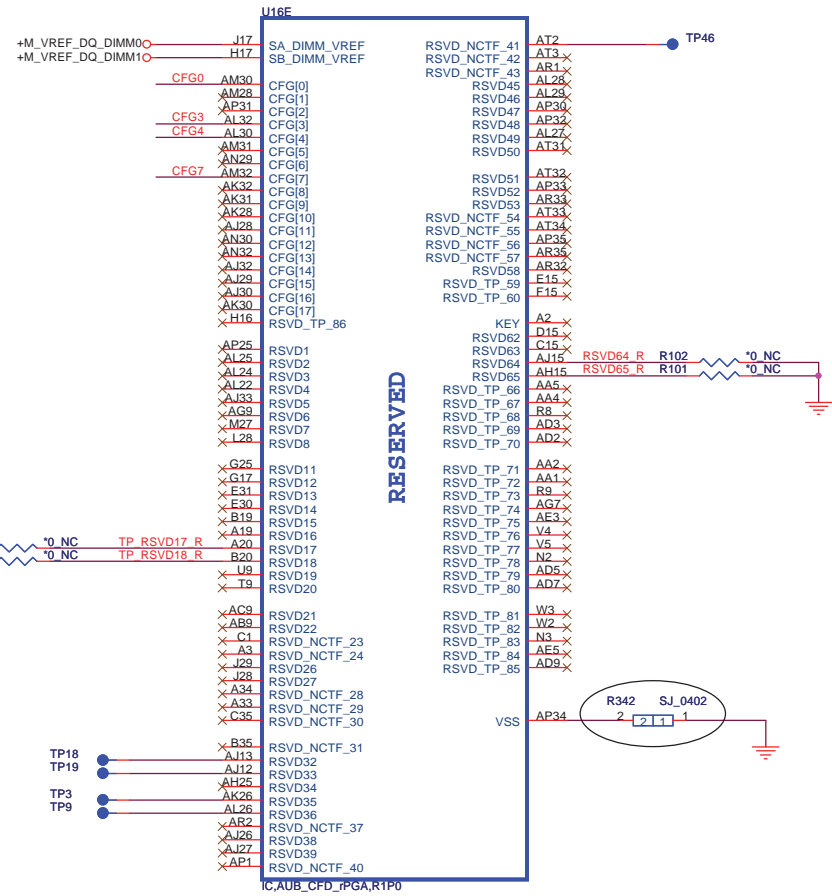
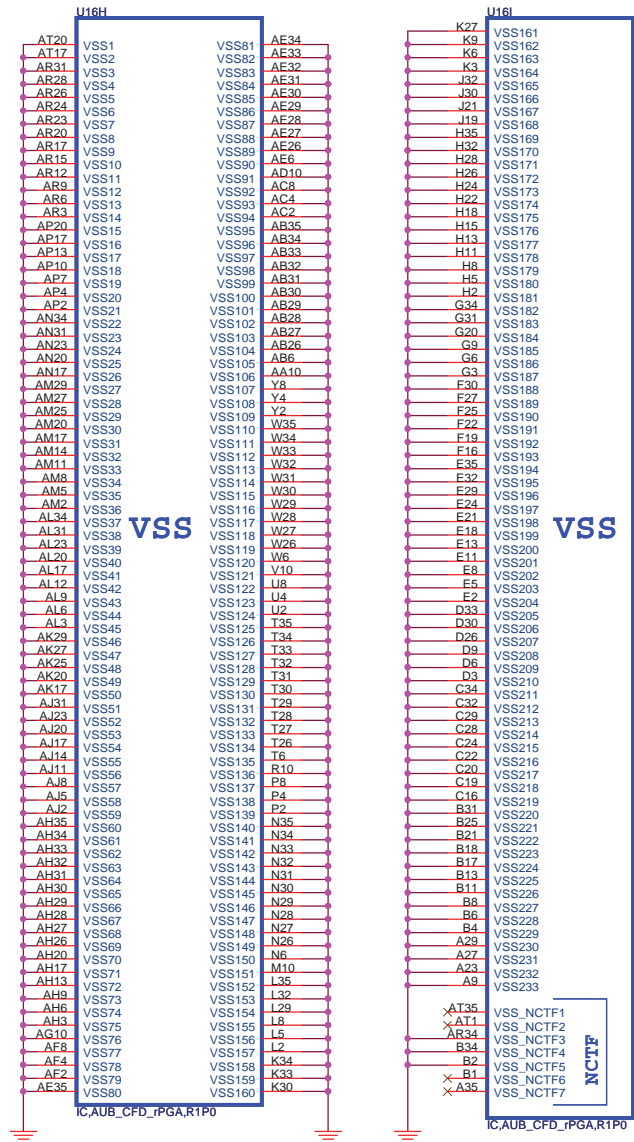
Pop it when Arrandale Graphics disable.



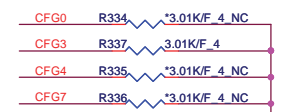
HFM_VID : Max 1.4V LFM_VID : Min 0.65V C397 close to R8361

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

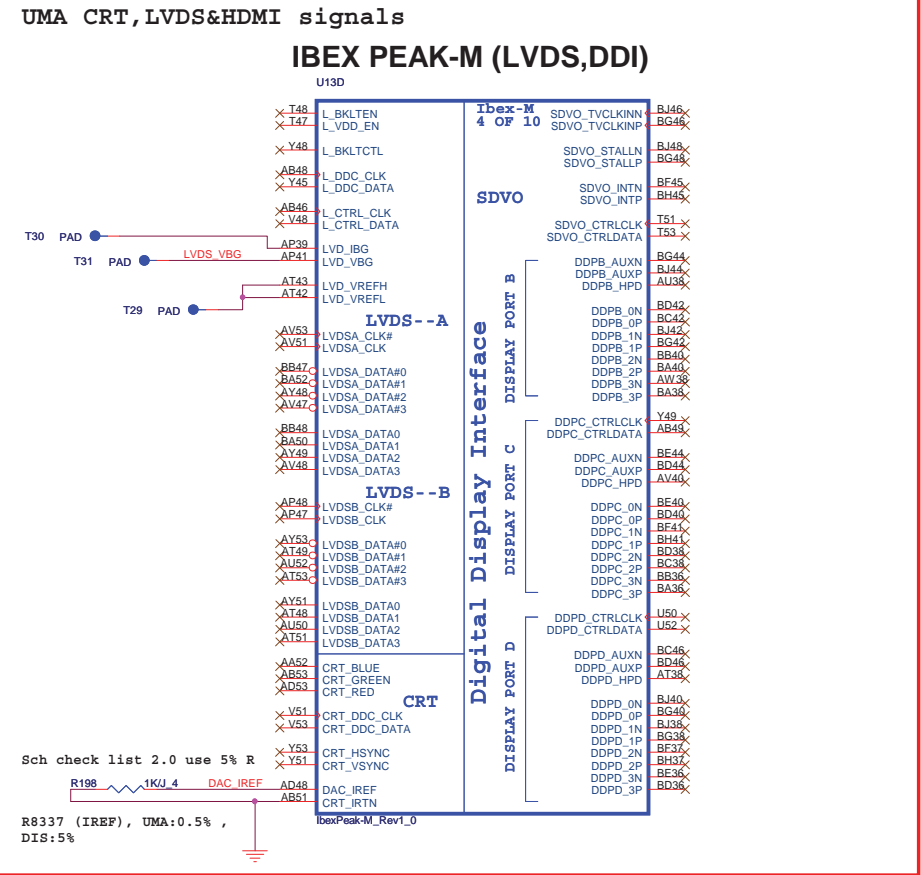
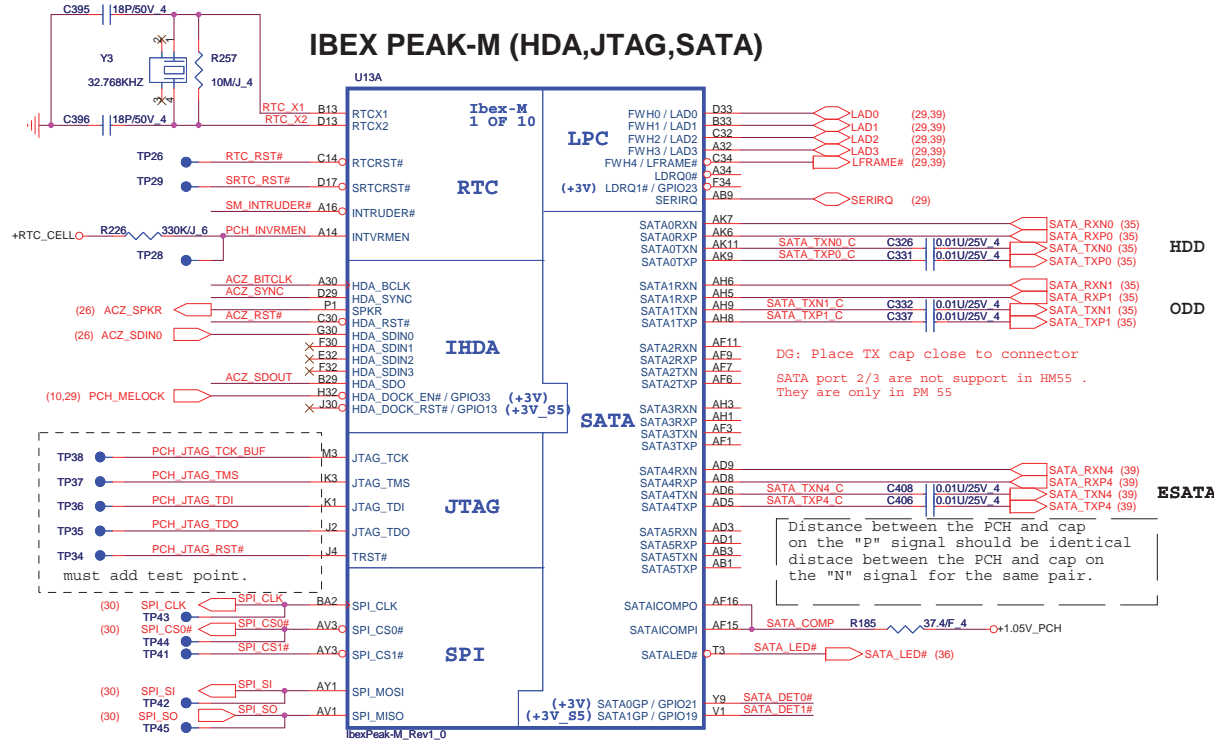
CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

Quanta Computer Inc.
 PROJECT : UM9B/C DIS

Size Document Number
PROCESSOR 4/4 (GND) Rev 3A

Date: Wednesday, January 27, 2010 Sheet 6 of 51

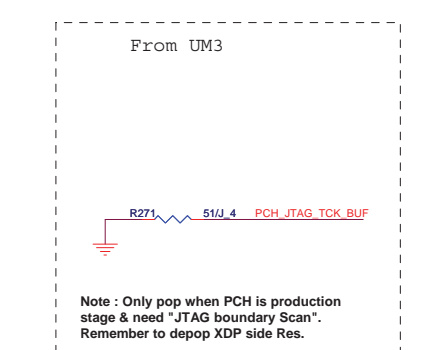
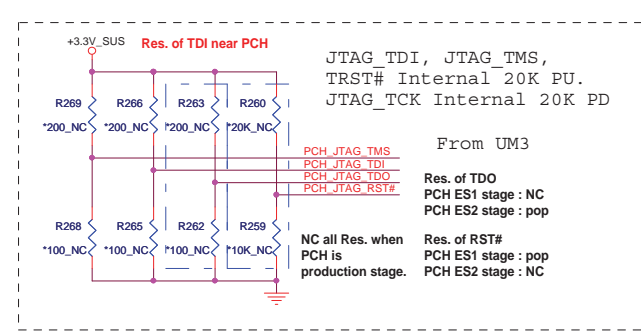
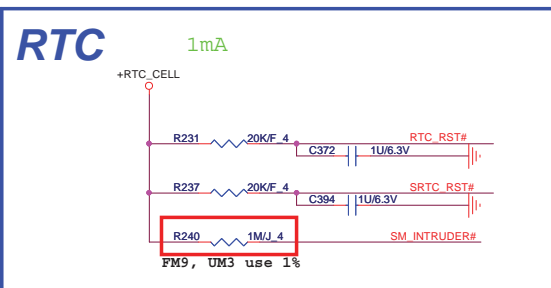
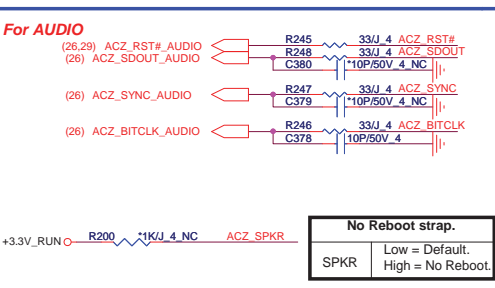
IBEX PEAK-M (HDA,JTAG,SATA)

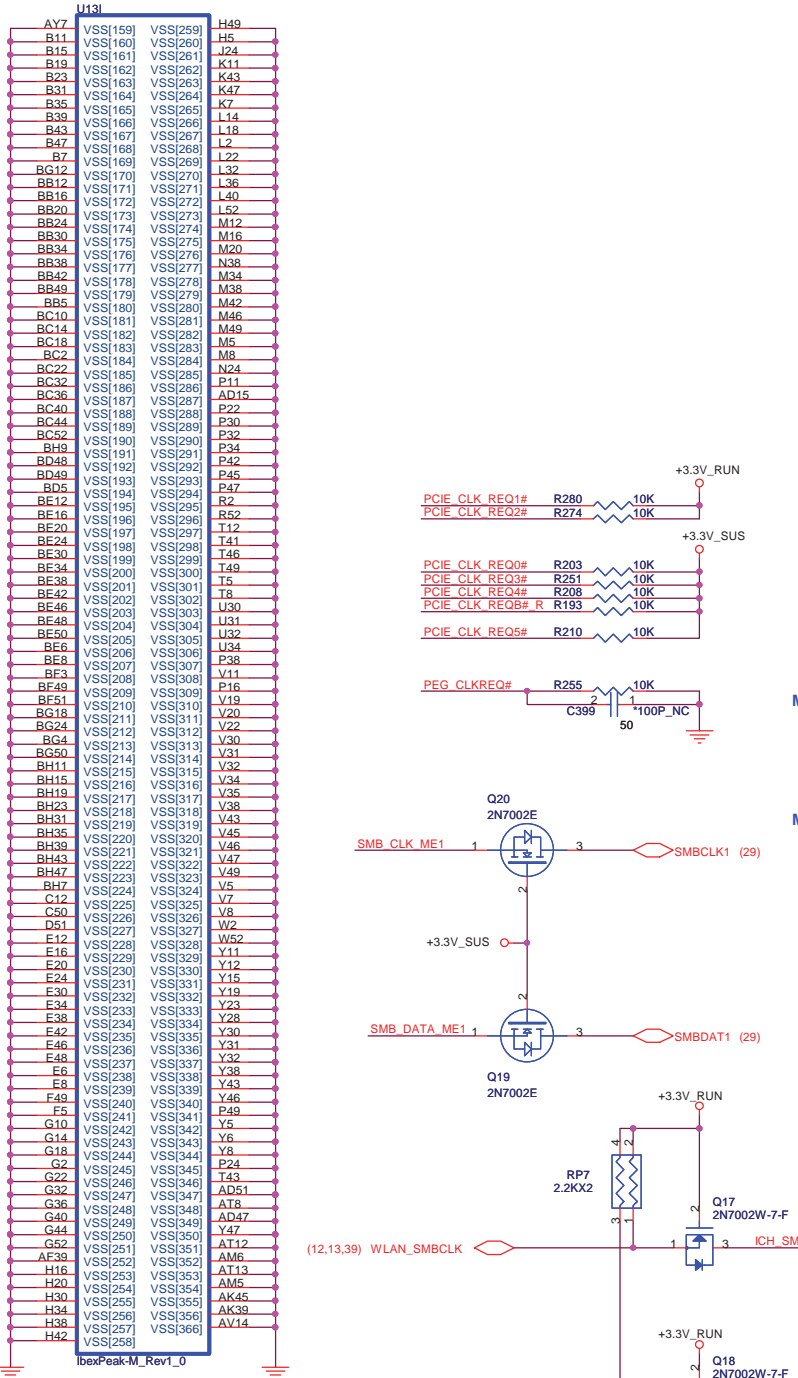


1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

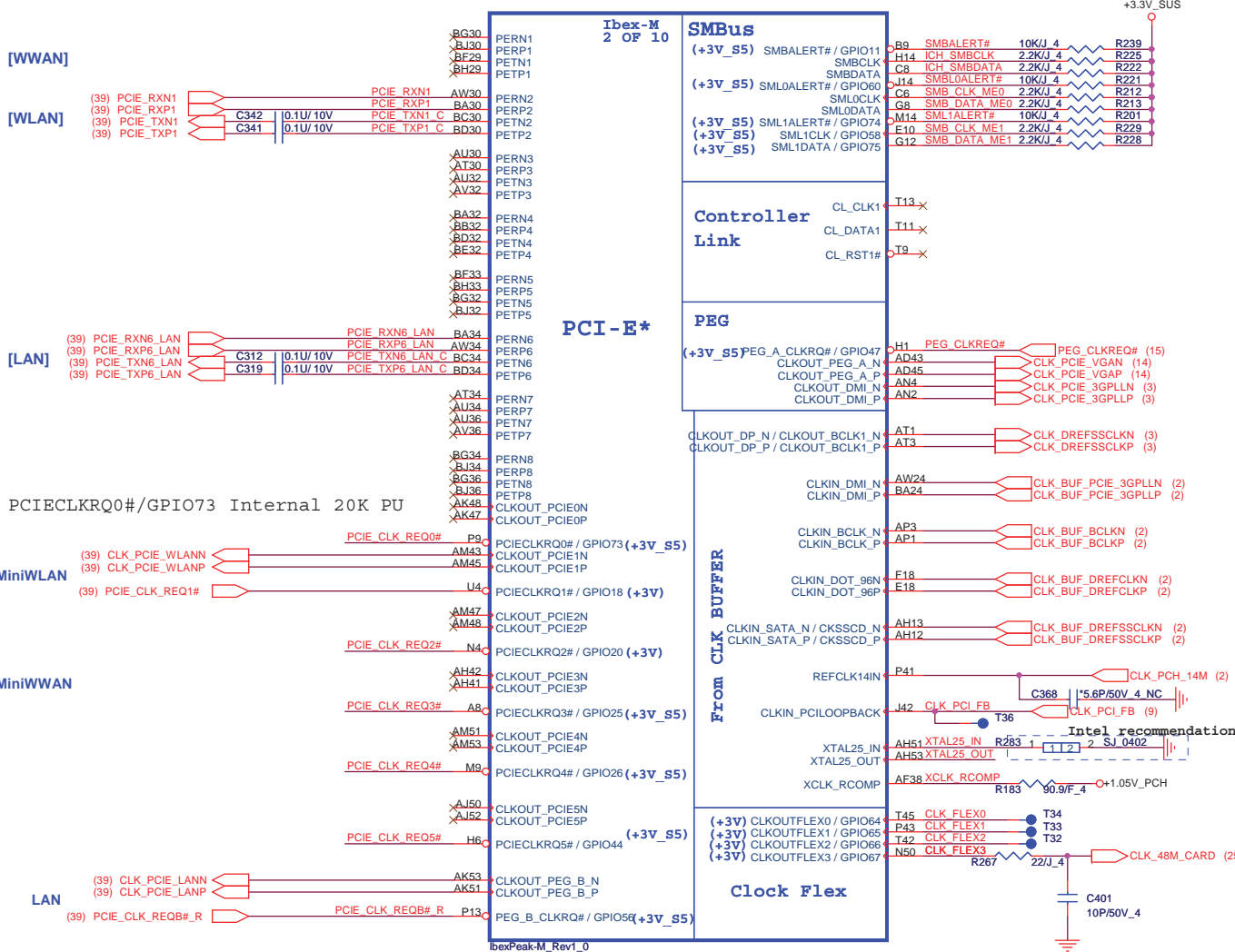
ITPM ENABLE/DISABLE
 From UM3

TPM Function	
Enable	Mount
Disable	NC (Default)



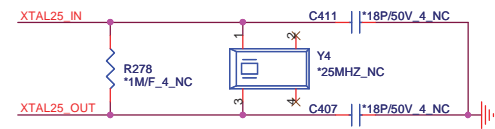


IBEX PEAK-M (PCI-E, SMBUS, CLK)



From CLK BUFFER

For UMA

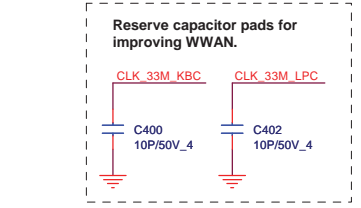
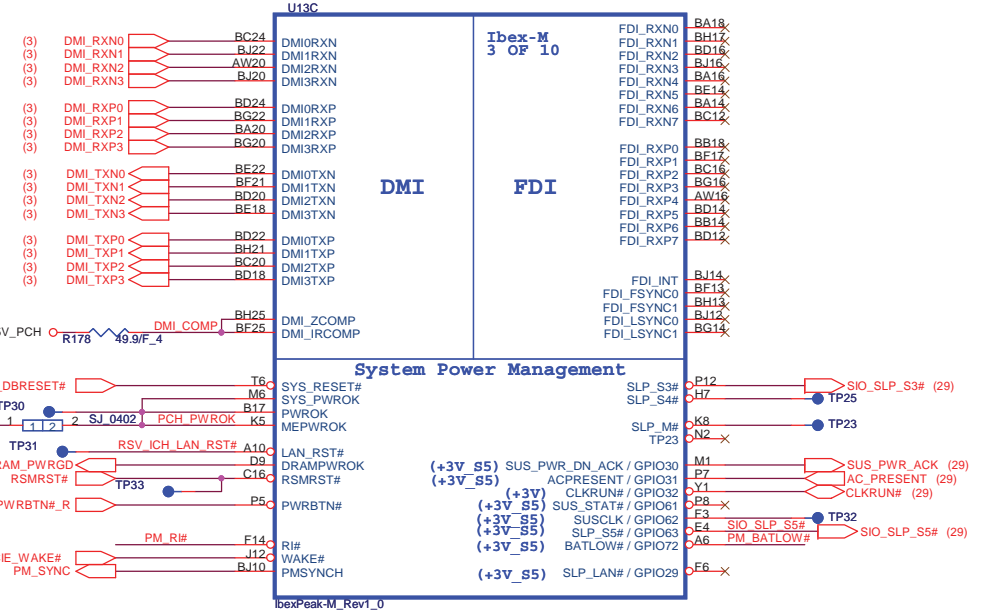
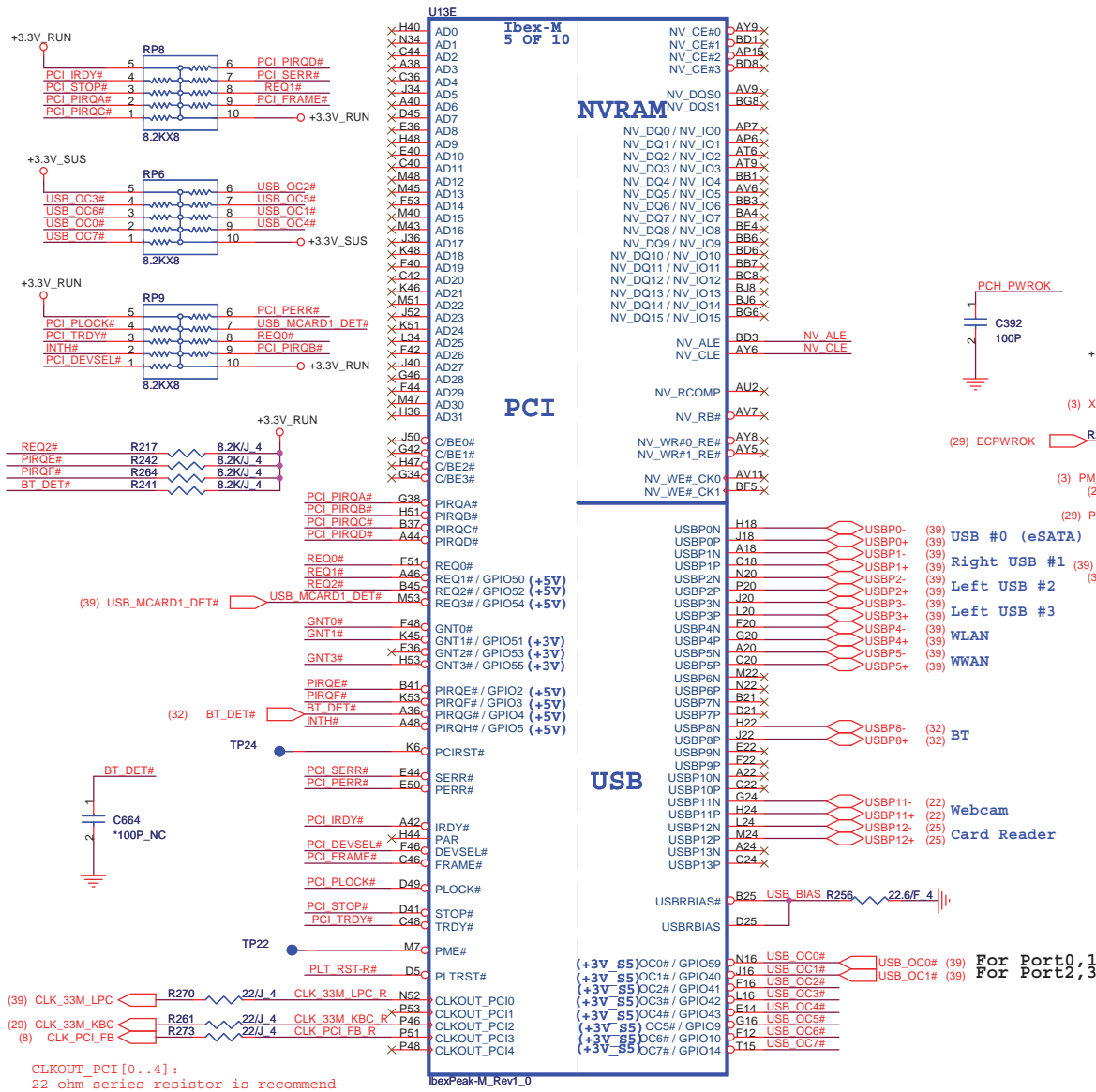


Quanta Computer Inc.
 PROJECT : UM9B/C DIS

Size	Document Number	PCH 2/5 (PCI-E, SMBUS, CK)	Rev	3A
Date:	Monday, February 01, 2010	Sheet	8	of 51

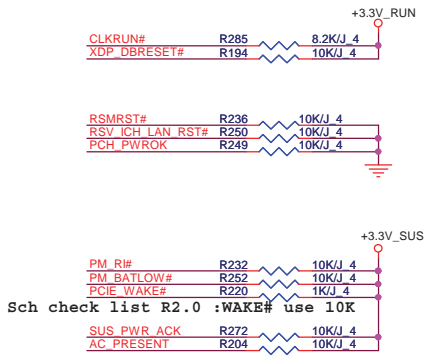
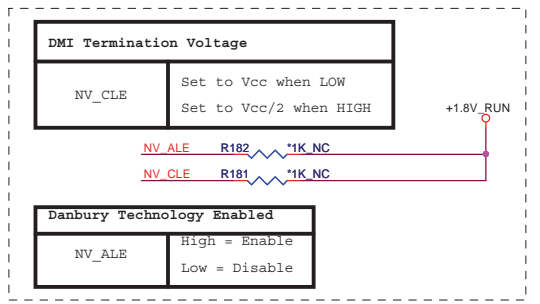
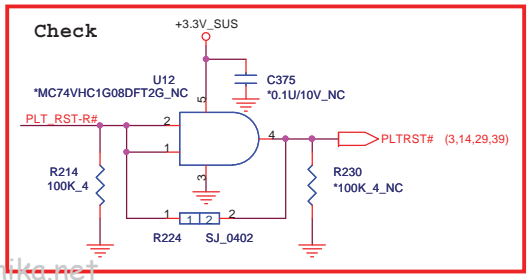
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

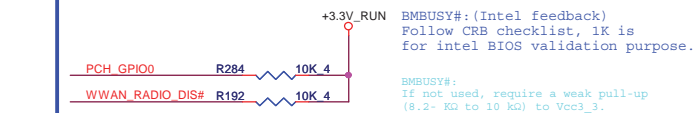
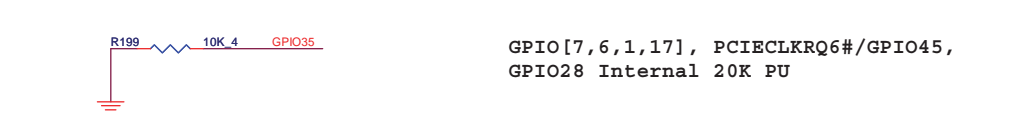
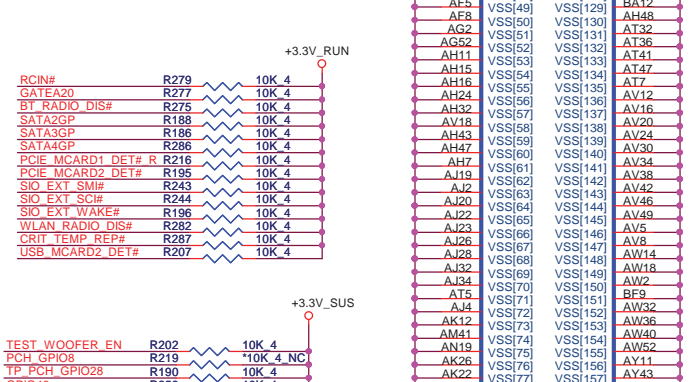
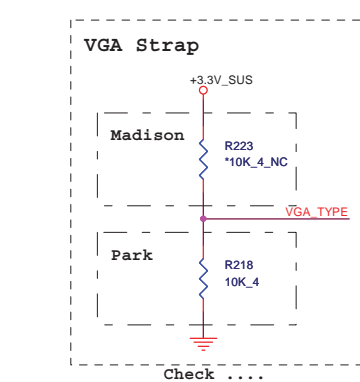
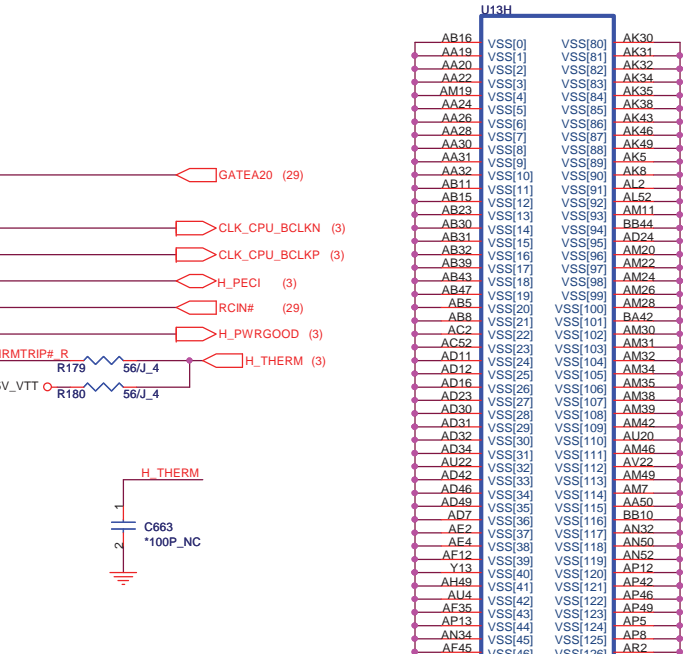
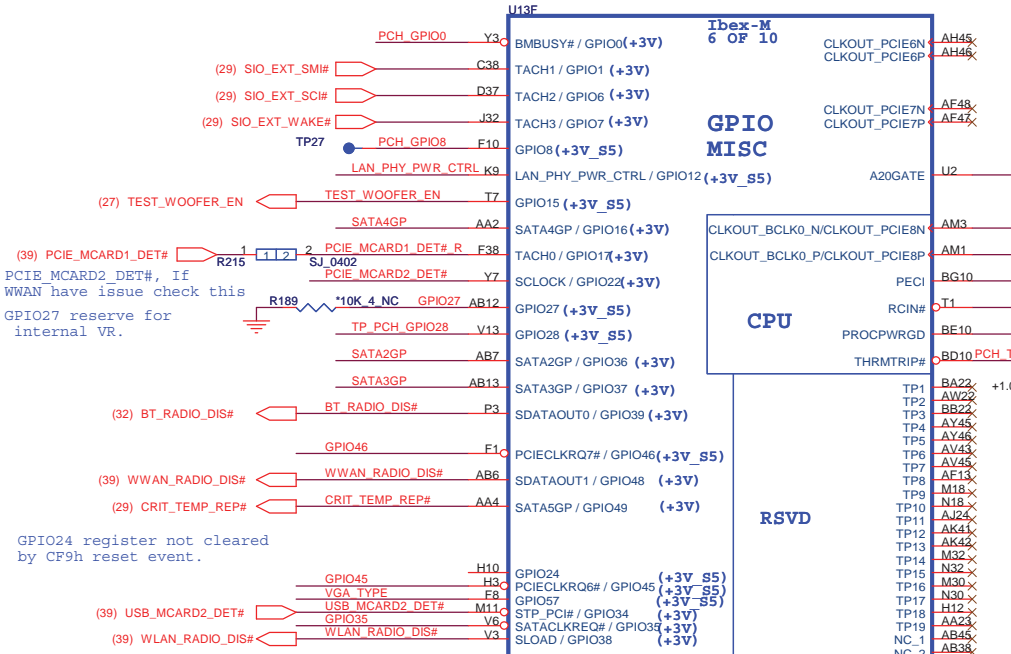
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default
0	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BATLOW#/GPIO72 Internal PU 20K

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)



Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled
--------	----------------------------------

(7,29) PCH_MELOCK R197 *1KJ_4_NC

(Internal 20K/F pull high to +3.3V_RUN)

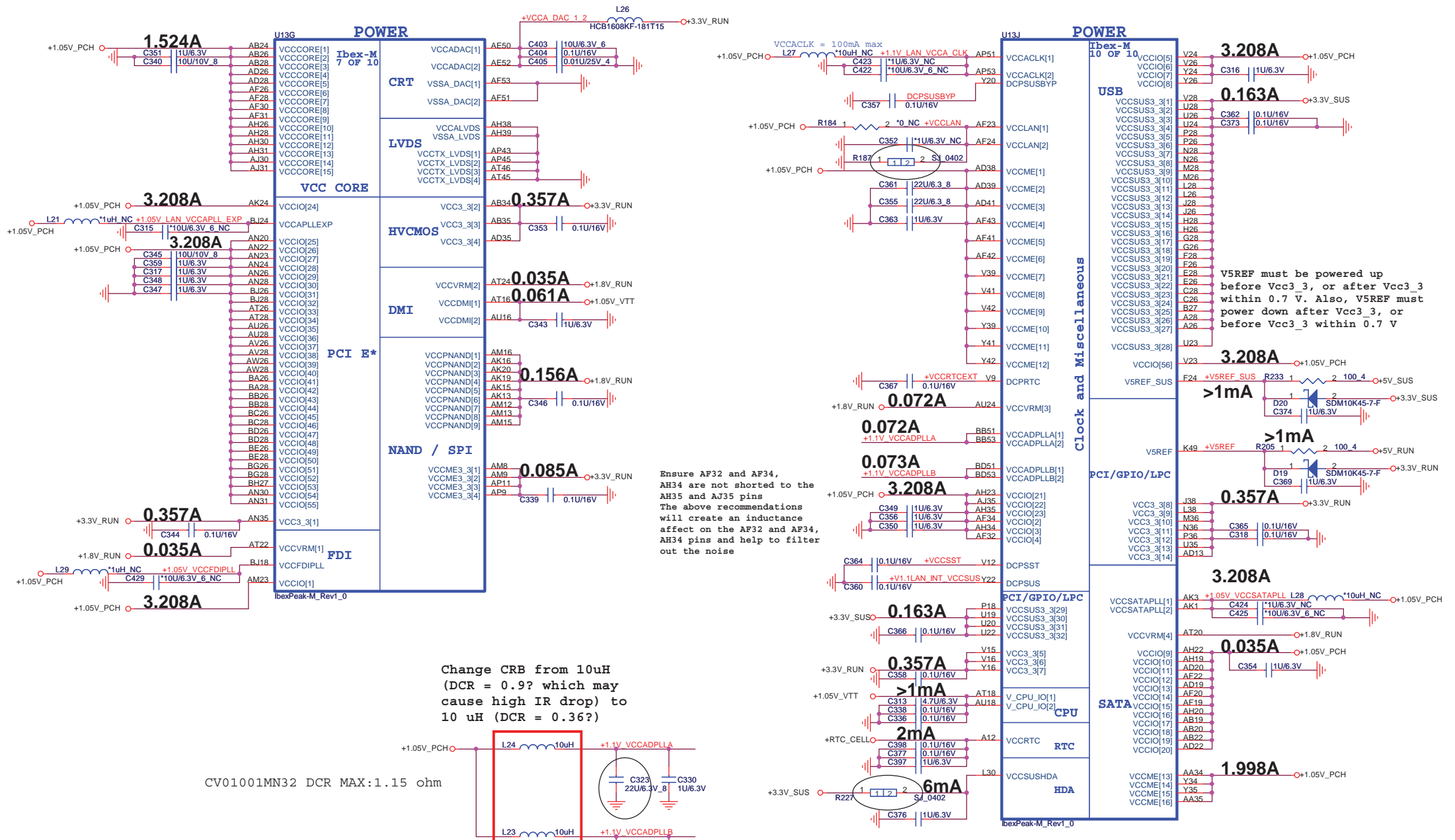
Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

WWAN_RADIO_DIS#	1-X High = Strong (Default)
-----------------	-----------------------------

Quanta Computer Inc.

PROJECT : UM9B/C DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	3A
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CV01001MN32 DCR MAX:1.15 ohm

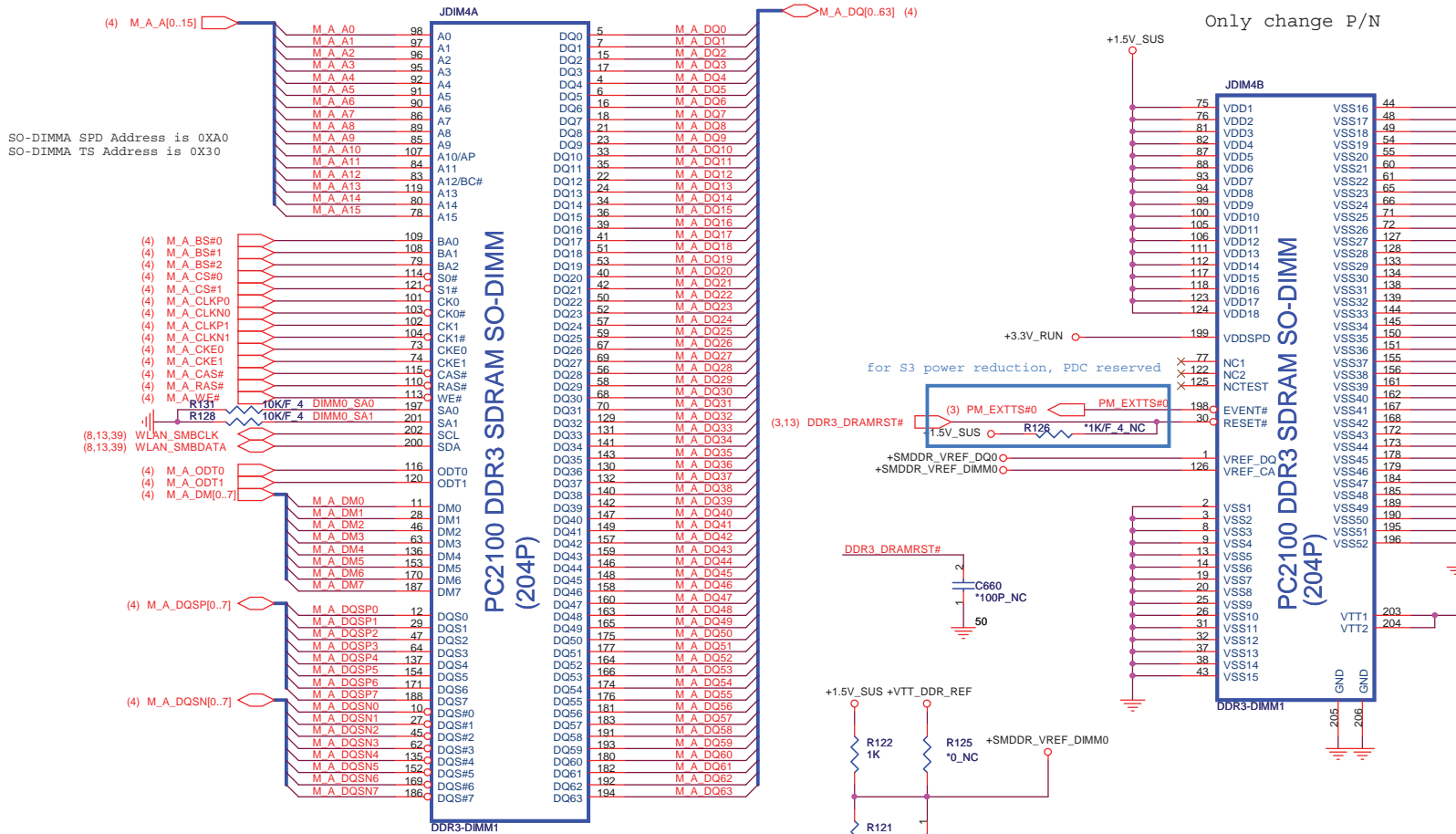
Change CRB from 10uH (DCR = 0.9? which may cause high IR drop) to 10 uH (DCR = 0.36?)

Ensure AF32 and AF34, AH34 are not shorted to the AH35 and AJ35 pins. The above recommendations will create an inductance affect on the AF32 and AF34, AH34 pins and help to filter out the noise

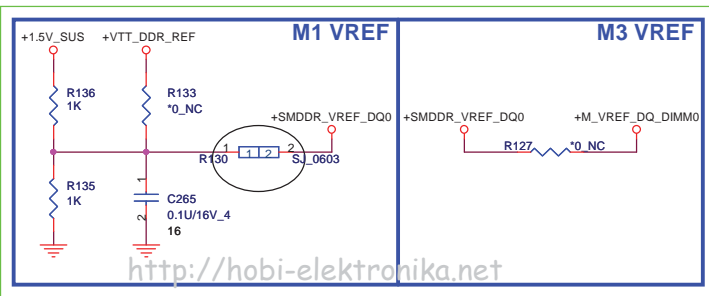
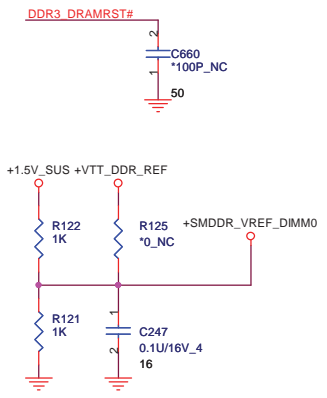
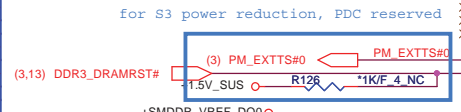
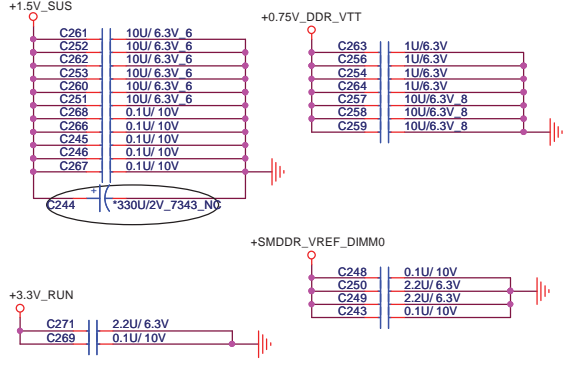
V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V

Only change P/N

Only change P/N



Place these Caps near So-Dimm0.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



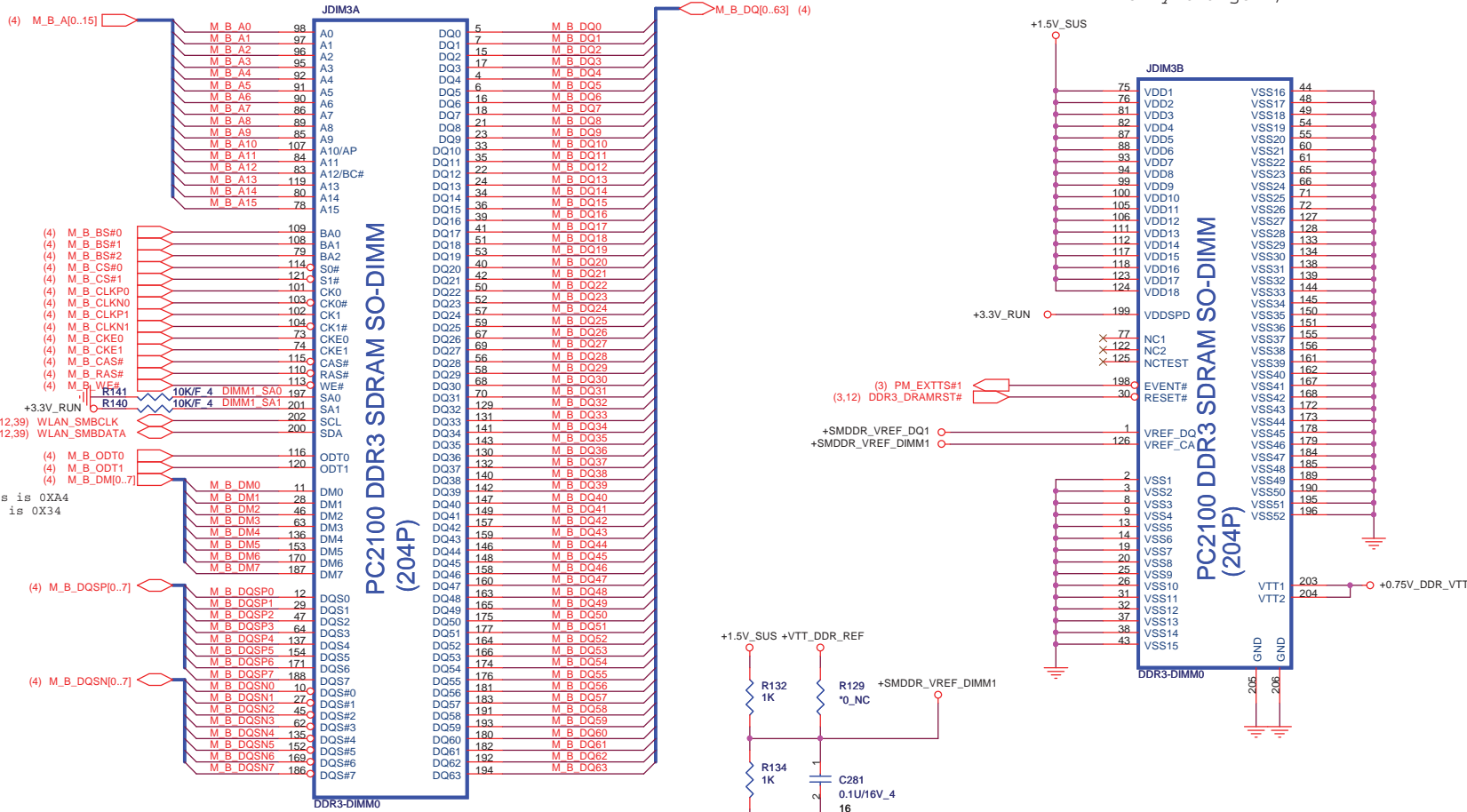
Quantities and M1/M3 follow UM3
Locations follow PDC

Quanta Computer Inc.
PROJECT : UM9B/C DIS

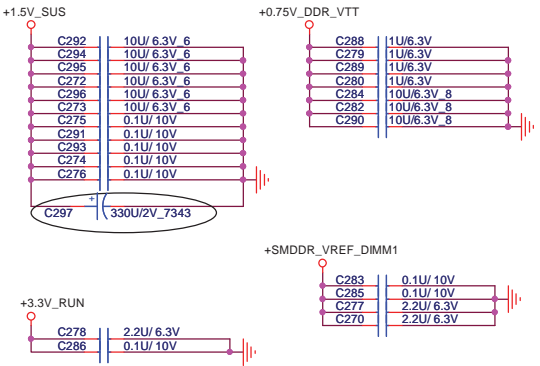
Size	Document Number	Rev
	DDR3 DIMM-0	3A
Date:	Monday, February 01, 2010	Sheet 12 of 51

Only change P/N

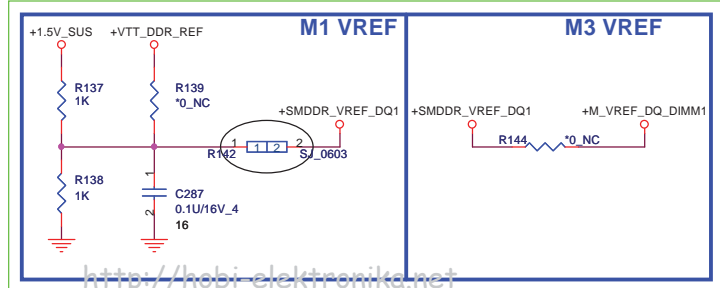
Only change P/N



Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%

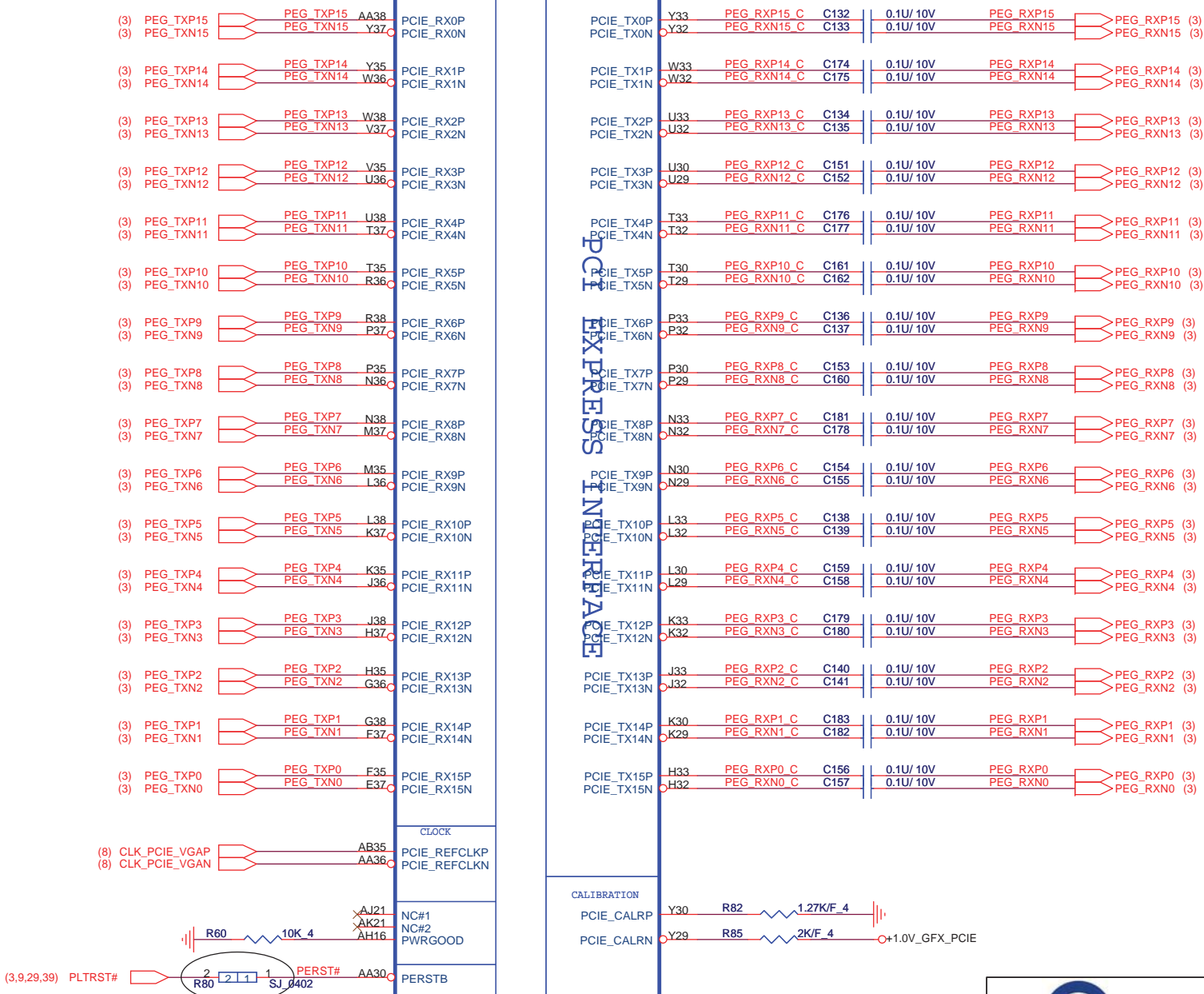


Quantities and M1/M3 follow UM3
 Locations follow PDC



U19A

PCI EXPRESS INTERFACE



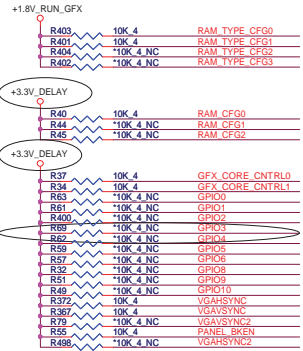
216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
		3A
Madison PCIE I/F		
Date:	Monday, February 01, 2010	Sheet 14 of 51

Memory Straps		RAM TYPE_CFG3	RAM TYPE_CFG2	RAM TYPE_CFG1	RAM TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
800 MHz 2GB(128M*16) Hynix_Orion die	H5TQ2G63BFR-12C	0	0	1	0
800 MHz 2GB(128M*16) Samsung_E die	K4W2G1646E-HC12	0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

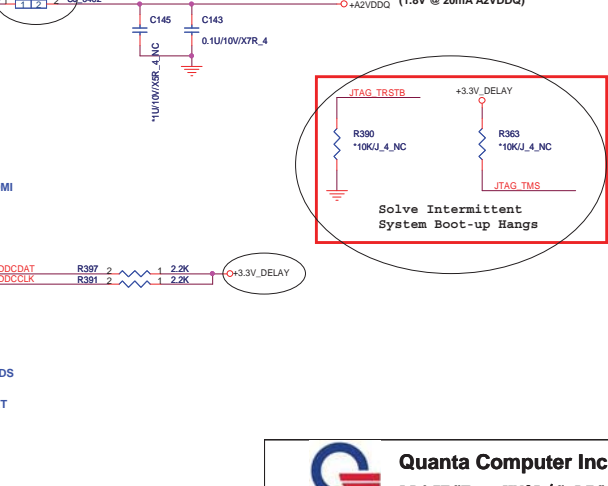
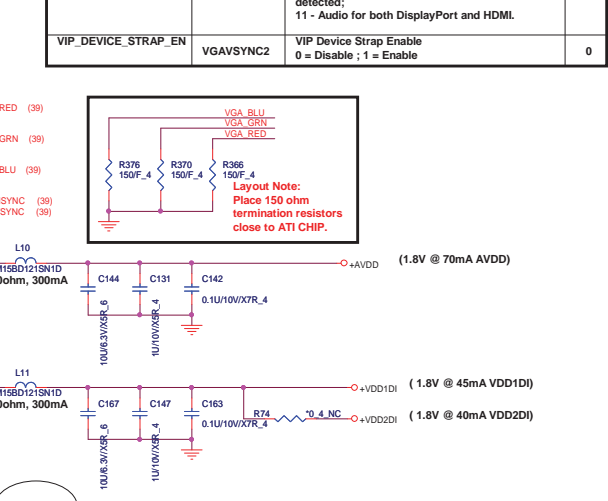
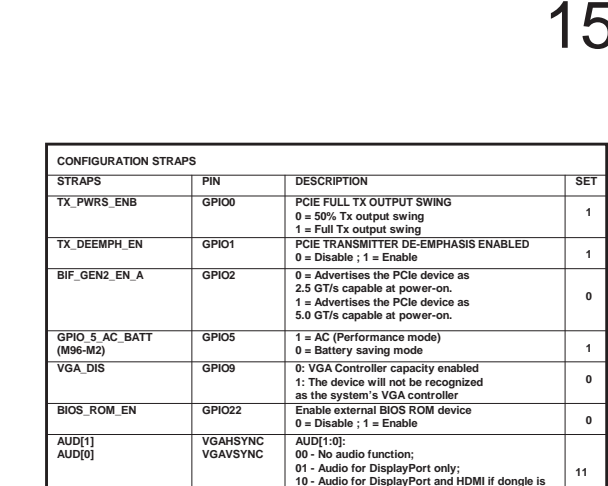
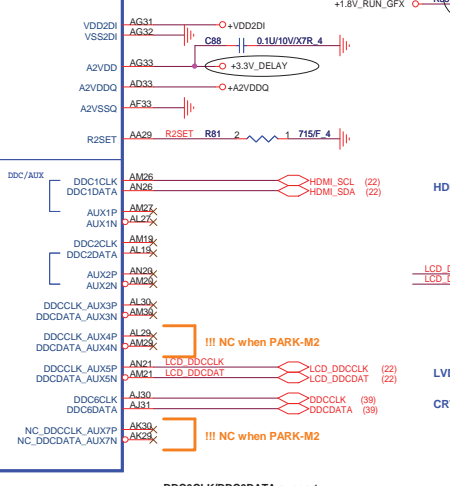
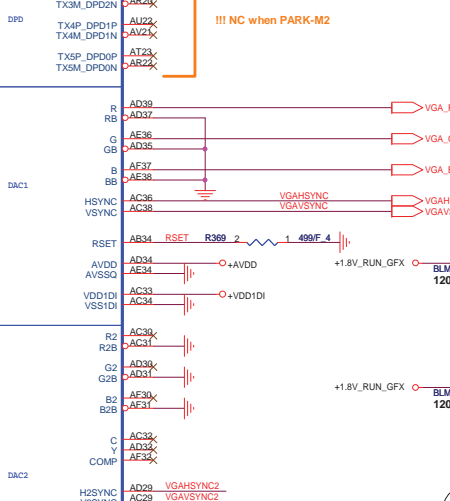
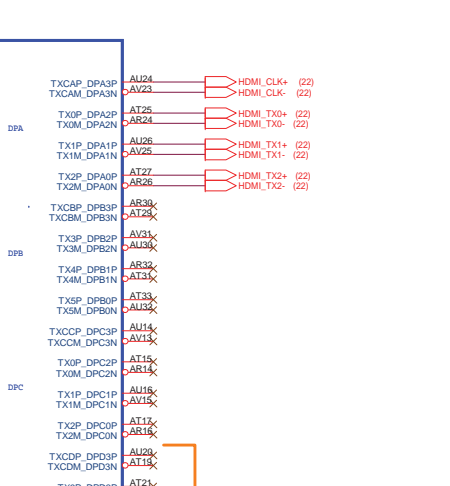
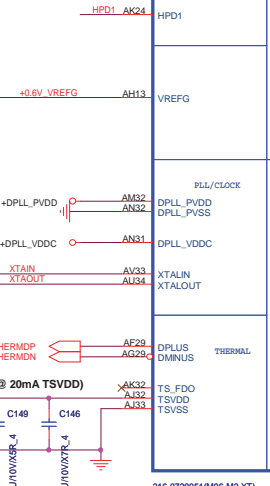
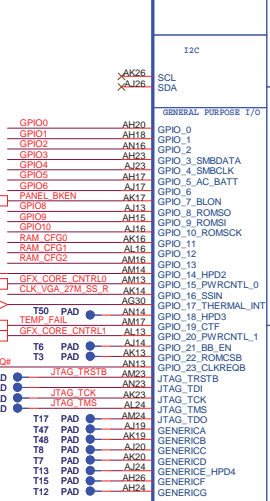
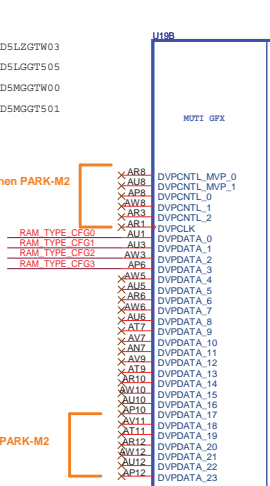
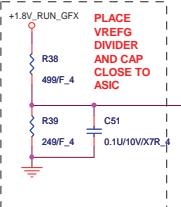
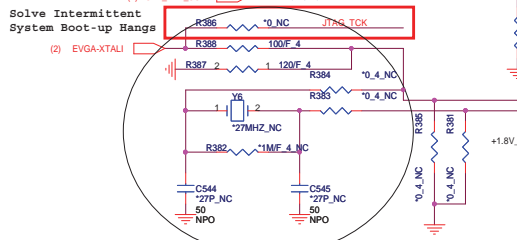
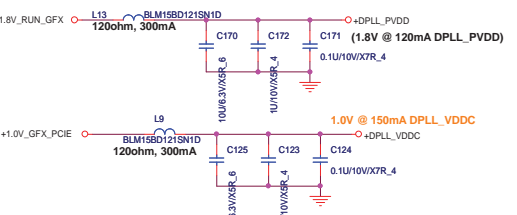


VRAM TYPE

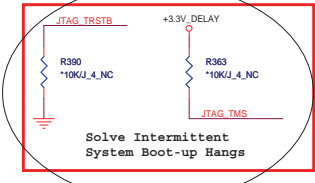
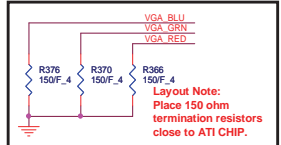
APERTURE SIZE

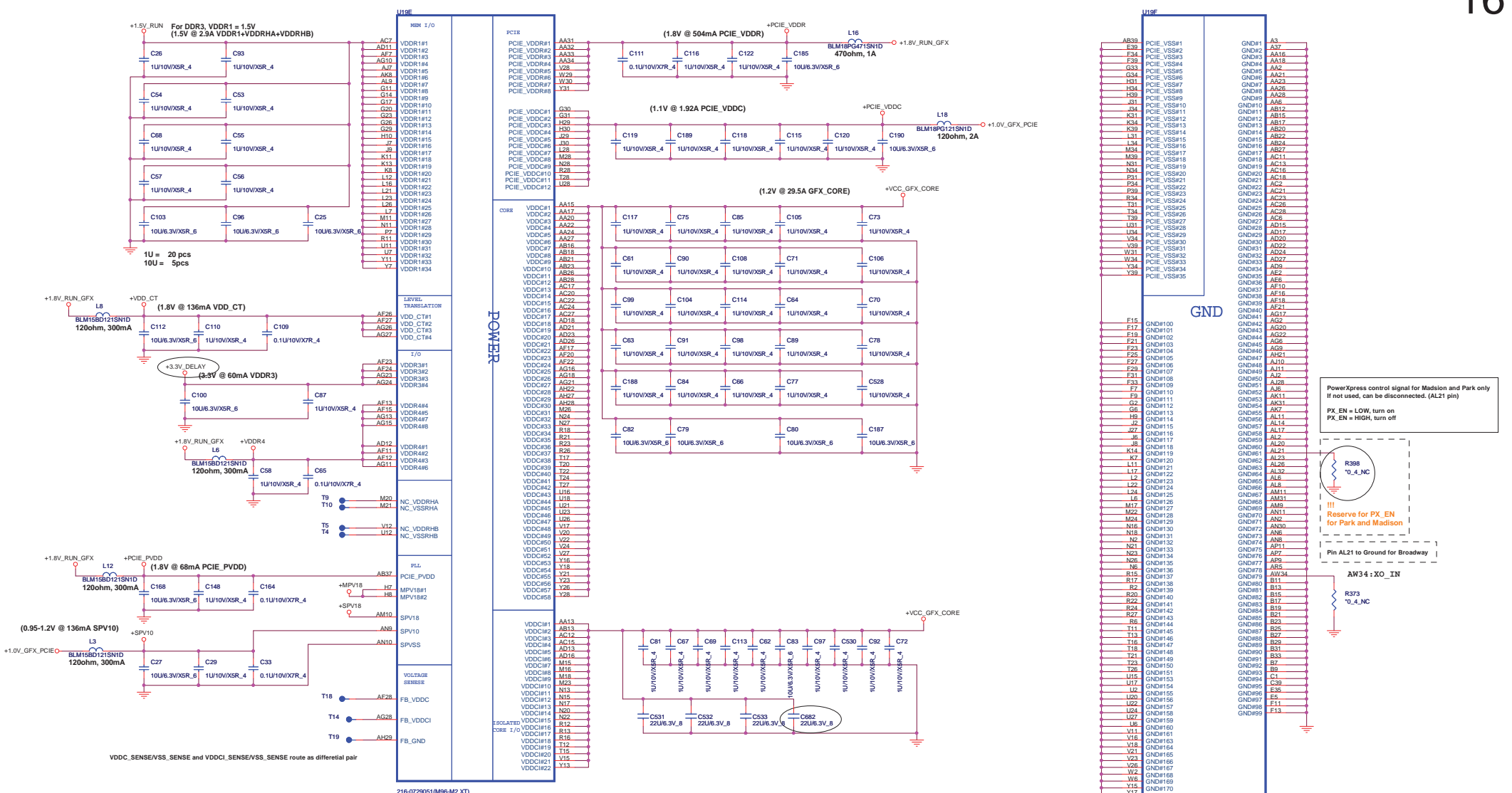
MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

- GPU Power-on sequence**
- 1 => +VGPU_CORE
 - 2 => +VGPU_IO
 - 3 => +1V
 - 4 => +1.5V_GPU
 - 5 => +3V_D
 - 6 => +1.8V_GPU
 - 7 => dGPU_PWROK

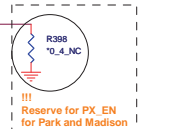


CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGASVSYNC VGASVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	VGASVSYNC2	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

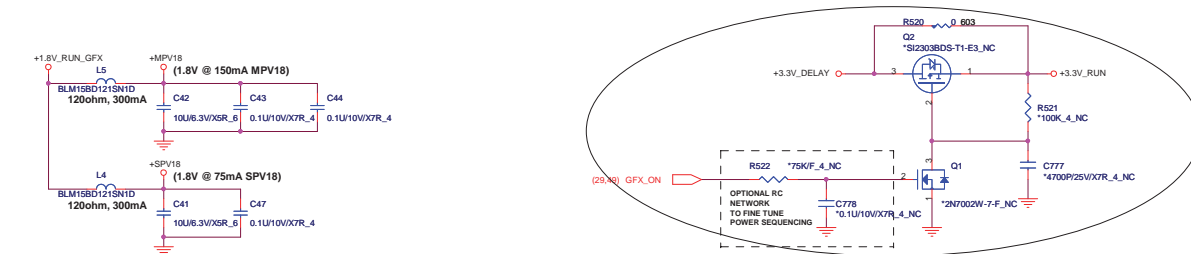
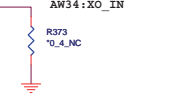




PowerXpress control signal for Madison and Park only
 If not used, can be disconnected. (AL21 pin)
 PX_EN = LOW, turn on
 PX_EN = HIGH, turn off



Pin AL21 to Ground for Broadway

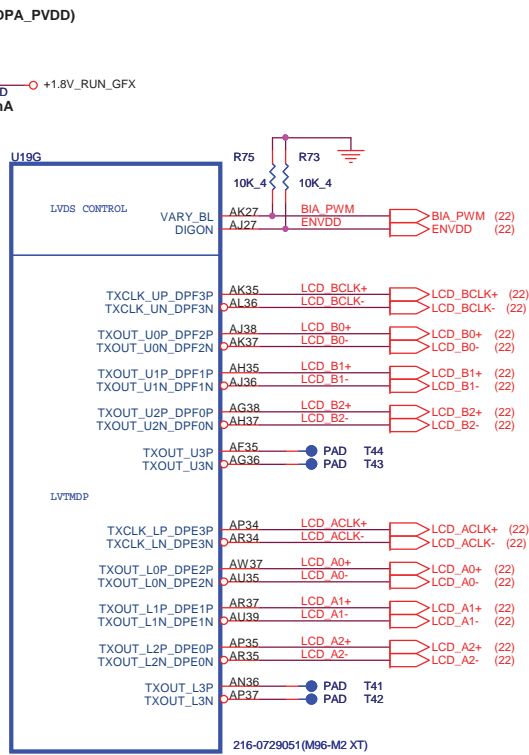
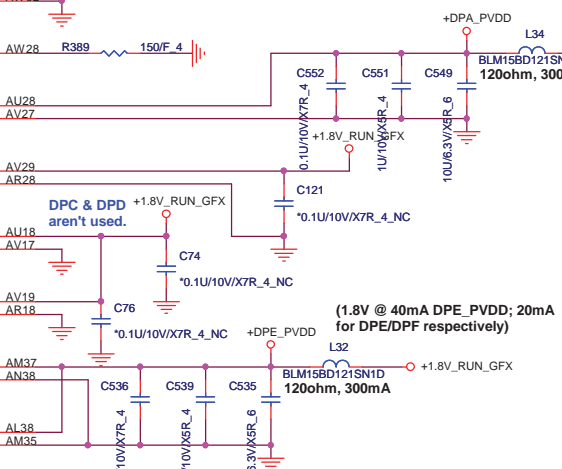
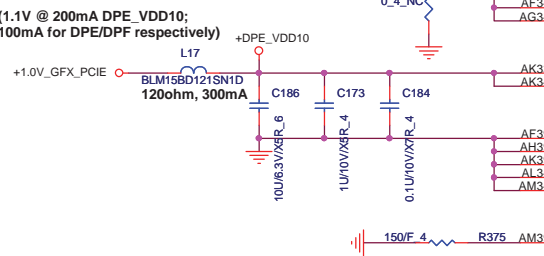
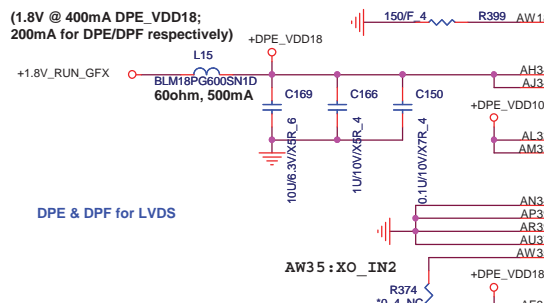
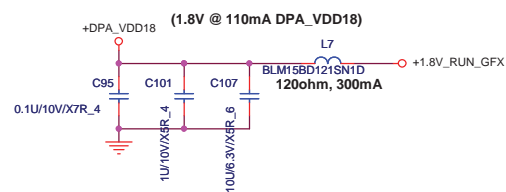
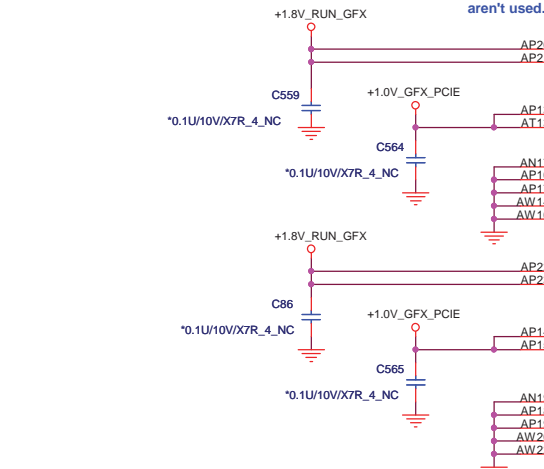


!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

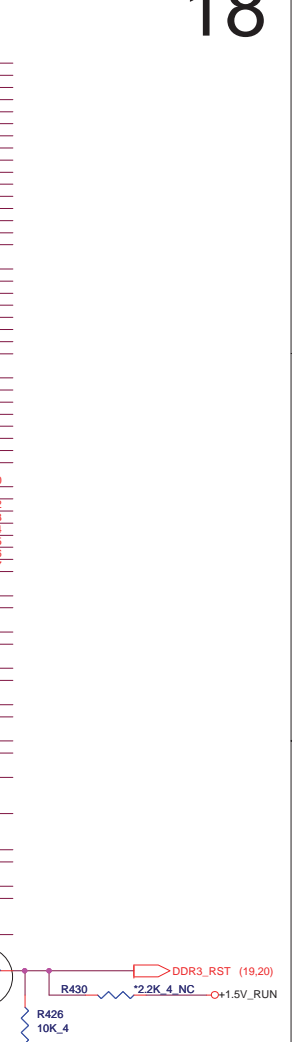
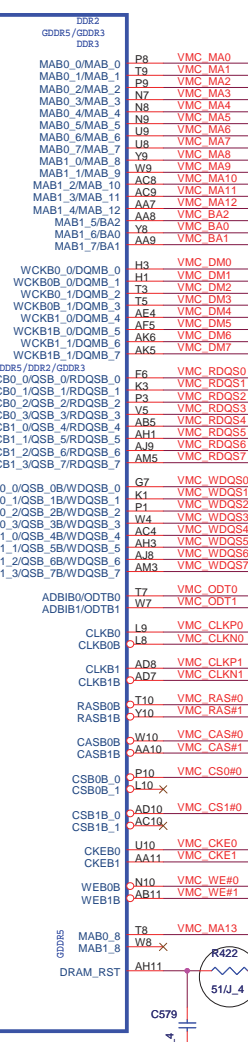
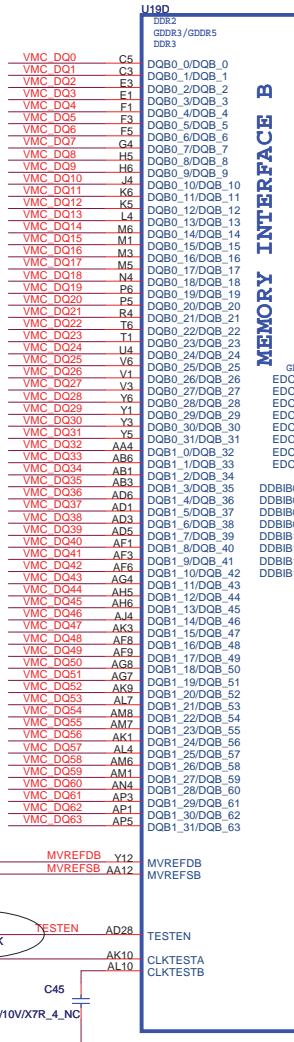
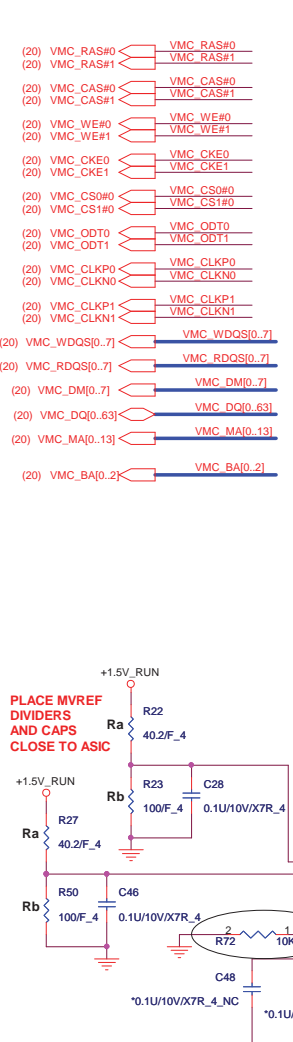
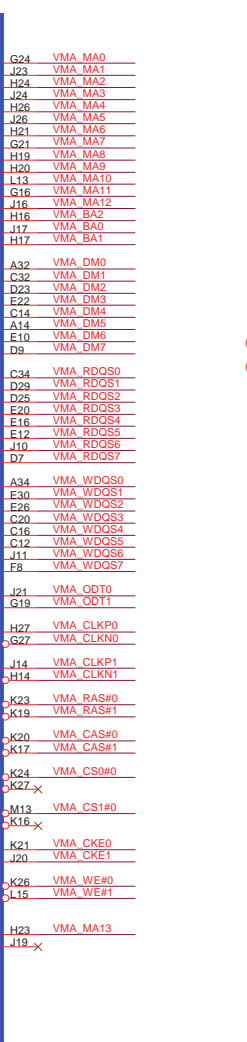
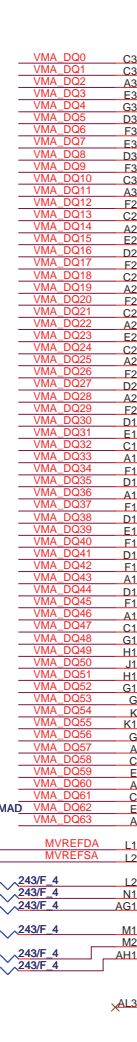
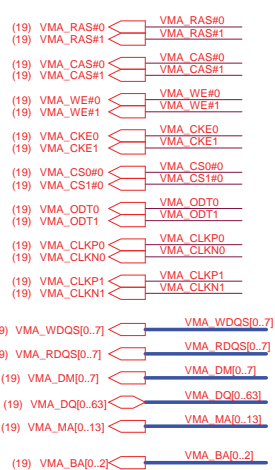
DPC & DPD aren't used.

U19H		U19G	
DP C/D POWER	DP A/B POWER	DP E/F POWER	DP PLL POWER
AP20 AP21	DPA_VDD18#1 DPA_VDD18#2	AH34 AJ34	DPA_PVDD DPA_PVSS
AP13 AT13	DPA_VDD10#1 DPA_VDD10#2	AL33 AM33	DPB_PVDD DPB_PVSS
AN17 AP16 AP17 AW14 AW16	DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5	AN34 AP39 AR39 AU37 AW35	DPC_PVDD DPC_PVSS
AP22 AP23	DPB_VDD18#1 DPB_VDD18#2	AF34 AG34	DPD_PVDD DPD_PVSS
AP14 AP15	DPB_VDD10#1 DPB_VDD10#2	AM37 AN38	DPE_PVDD DPE_PVSS
AN19 AP18 AP19 AW20 AW22	DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5	AL38 AM35	NC_DPF_PVDD NC_DPF_PVSS
			DPEF_CALR

216-0729051 (M96-M2 XT)

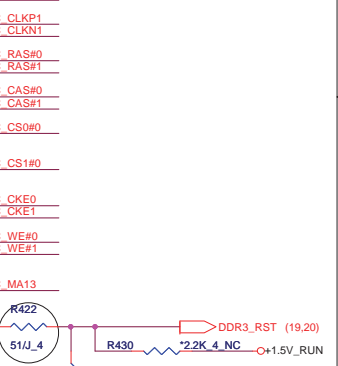
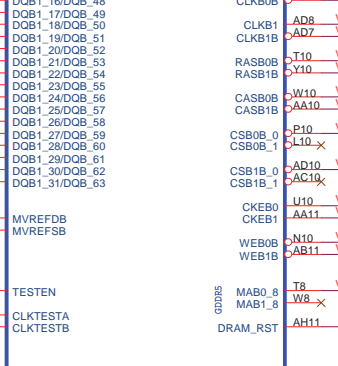
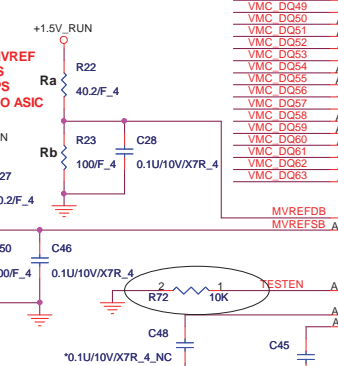
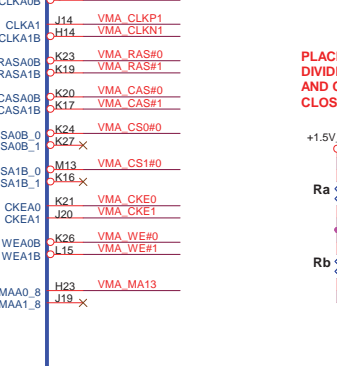
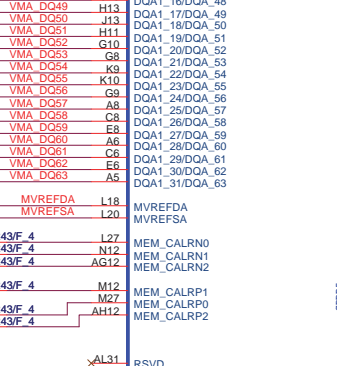
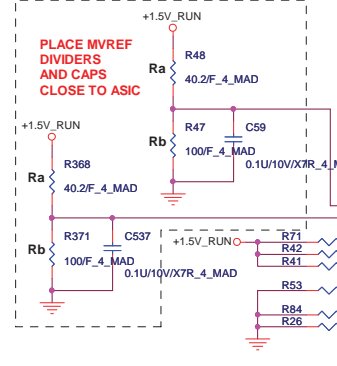


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PROJECT : UM9B/C DIS



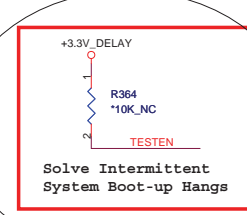
MEMORY INTERFACE A

MEMORY INTERFACE B



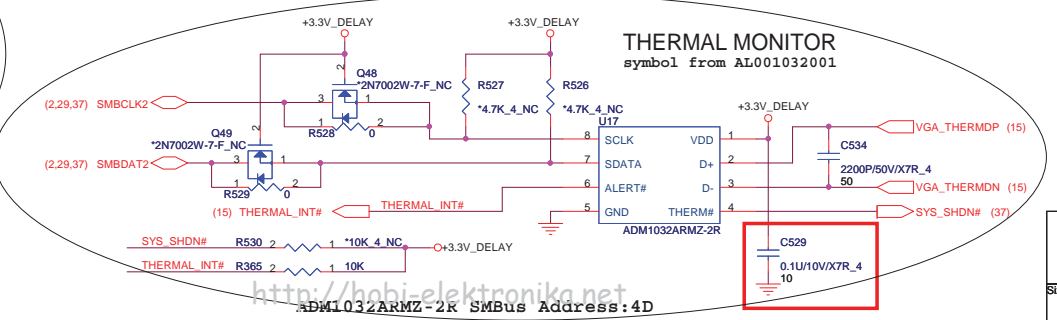
Solve Intermittent System Boot-up Hangs

VGA	ENG	MP
R386	V	
R390	V	
R363	V	
R364	V	
R72		V

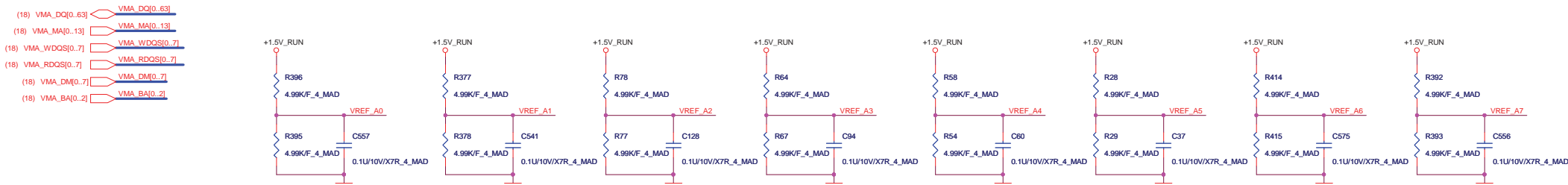
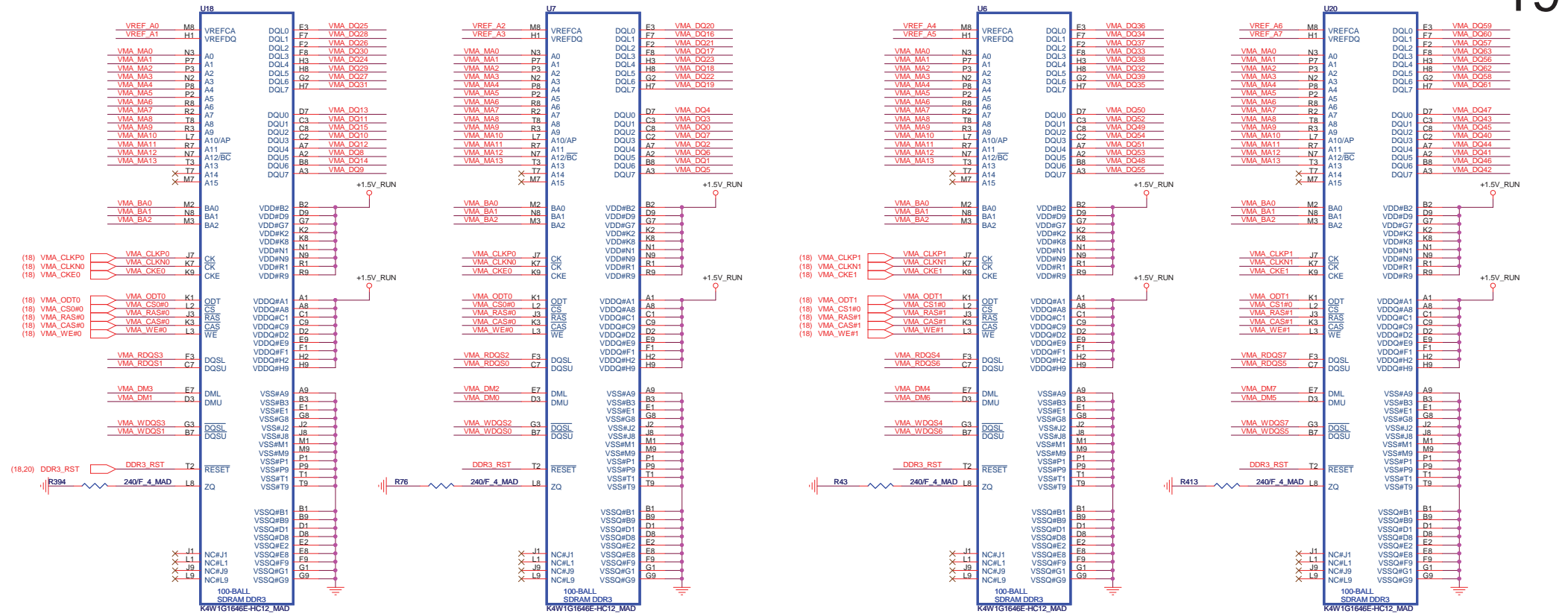


DDR3/GDDR3 Memory Stuff Option

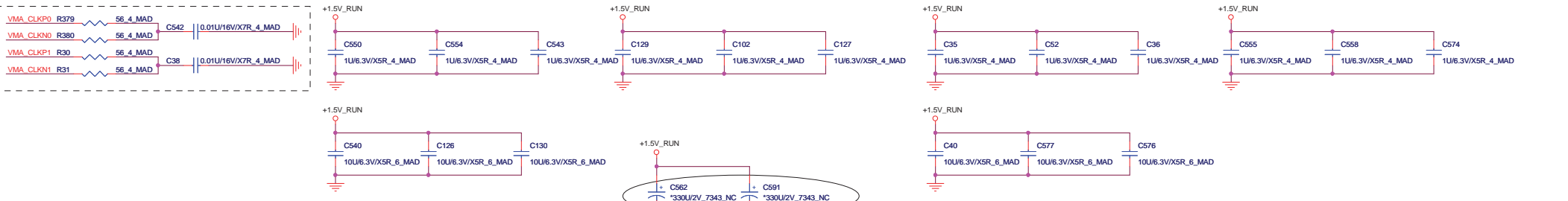
MVDDQ	GDDR3	DDR3
	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R



Quanta Computer Inc.
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Rev 3A
Date: Monday, February 01, 2010 1 Sheet 18 of 51

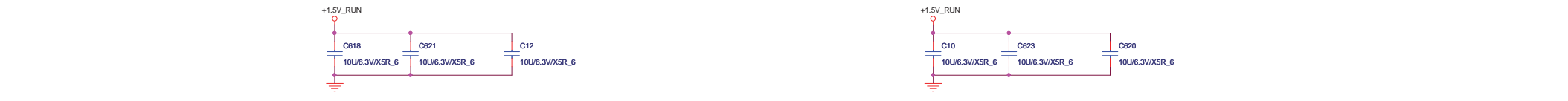
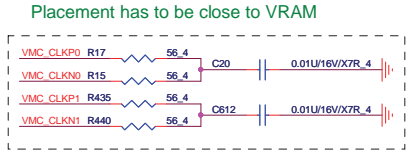
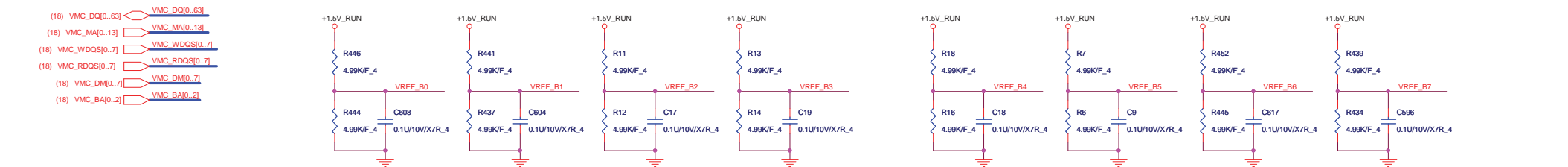
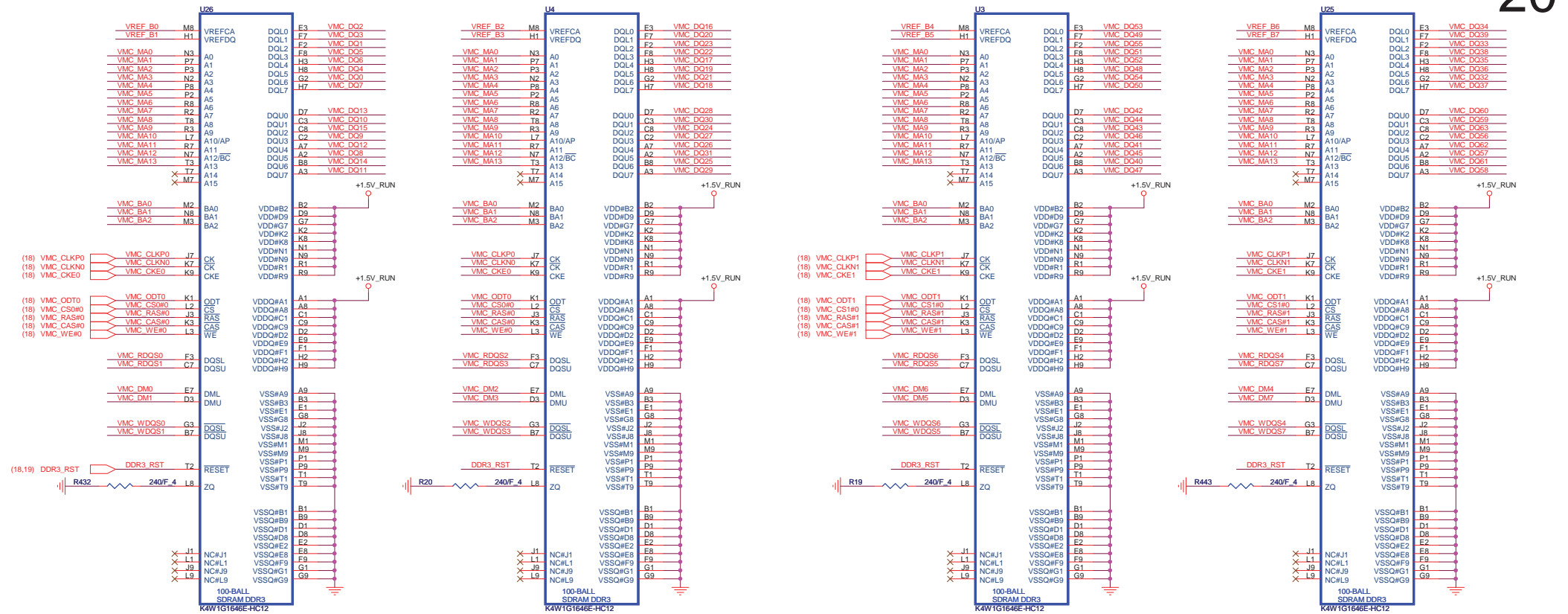


Placement has to be close to VRAM

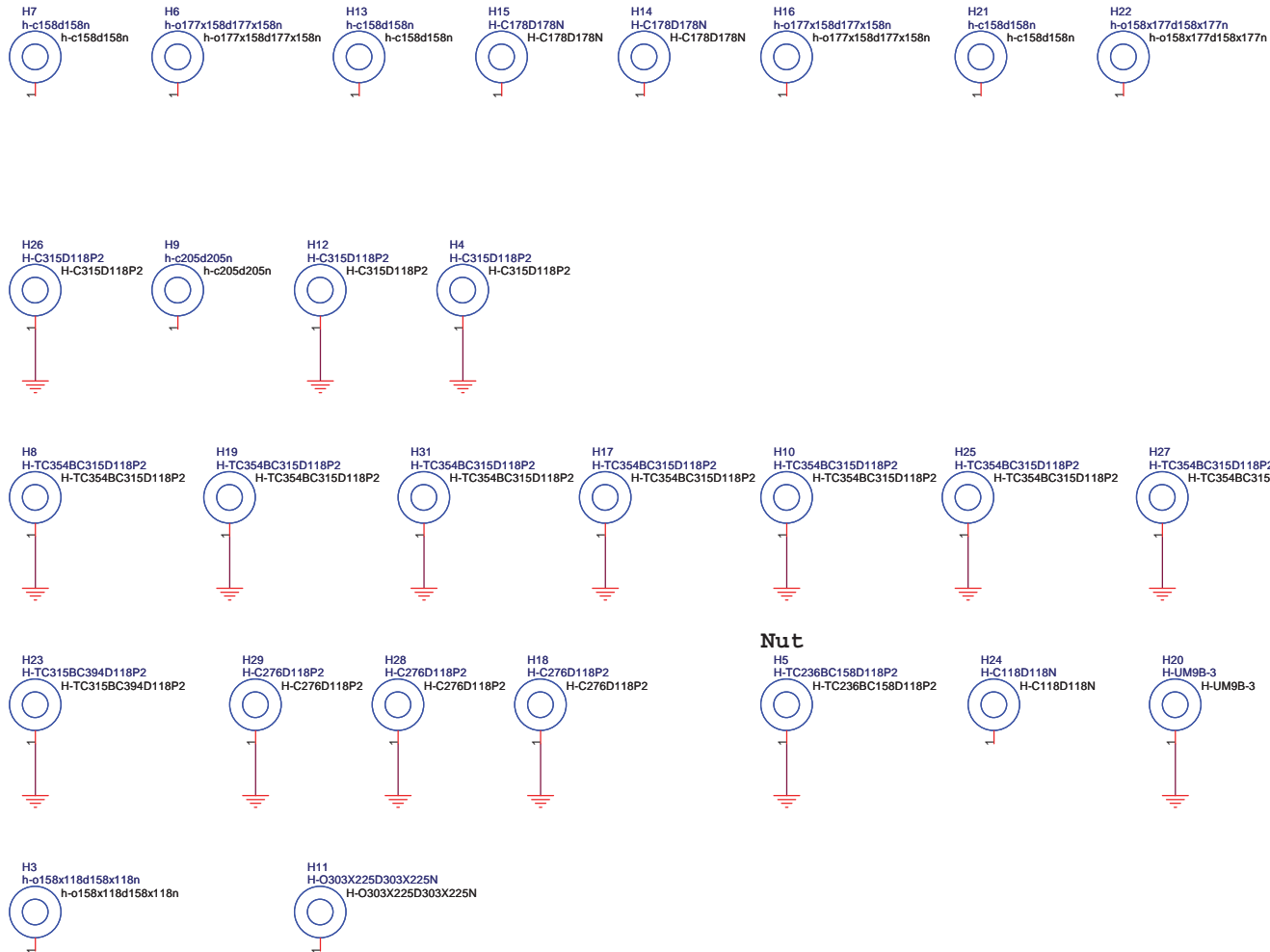


Samsung E-die K4W1G1646E-HC12) 64M*16:AKD5LGGT505
 Hynix Orion-dieH5Tq1G63BFR-12C) 64M*16:AKD5LZGTW04
 Samsung E-die K4W2G1646B-HC12) 128M*16:AKD5MGGT501
 Hynix Orion-dieH5Tq2G63BFR-12C) 128M*16:AKD5MGGTW00

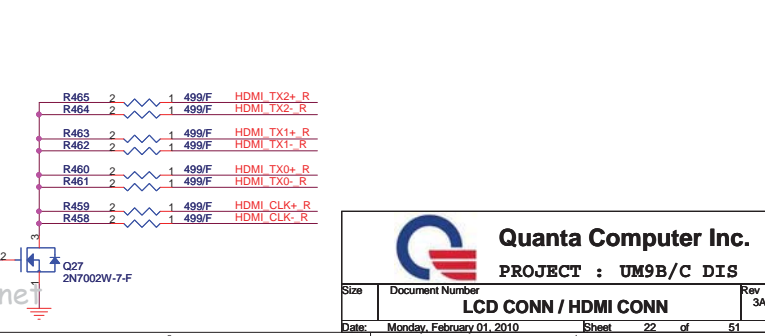
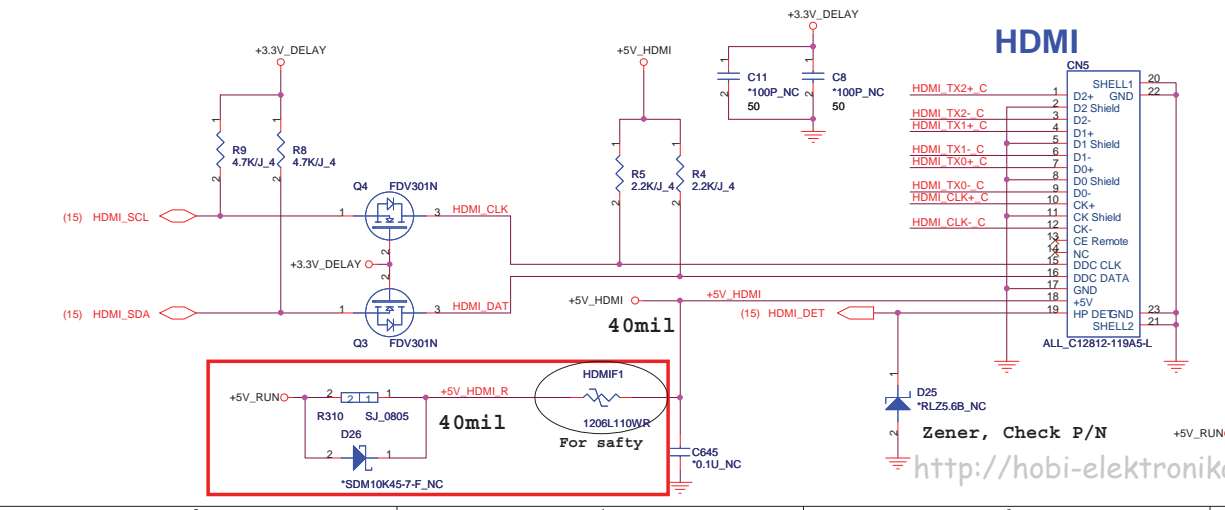
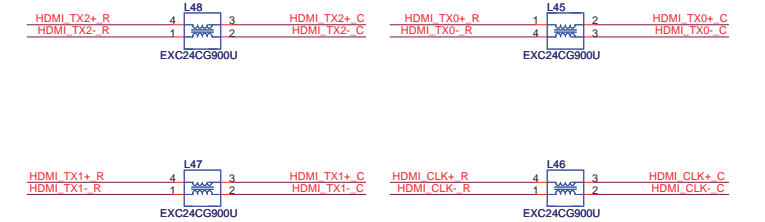
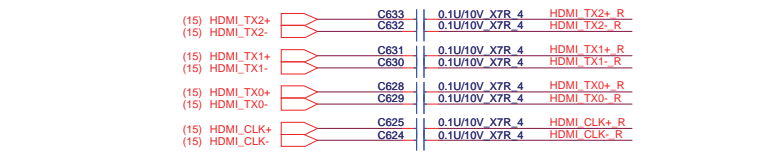
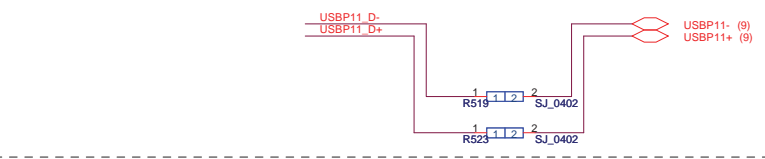
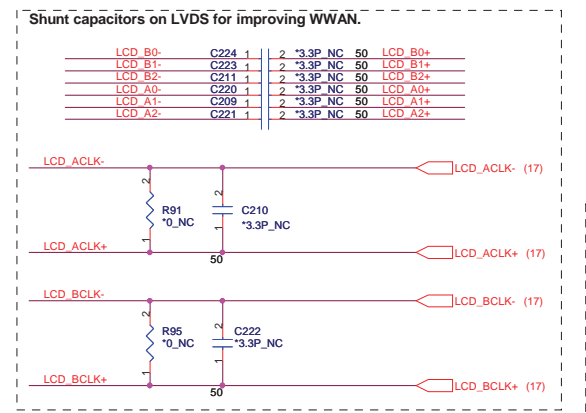
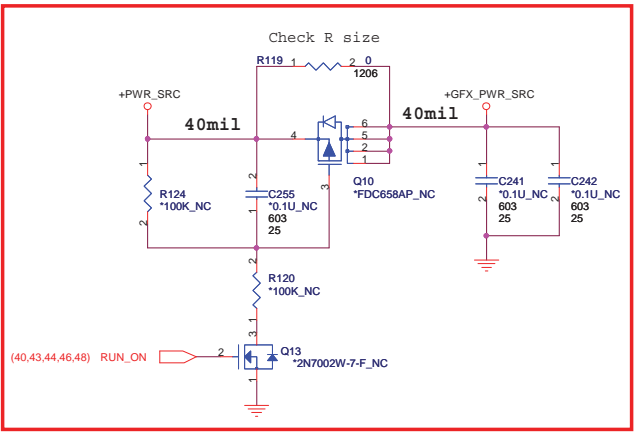
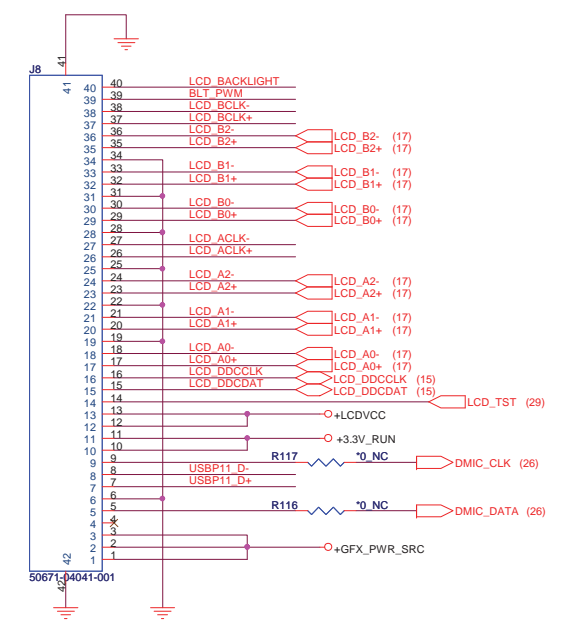
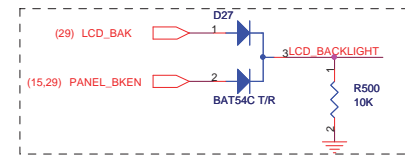
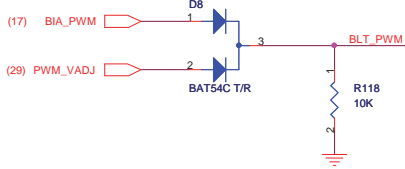
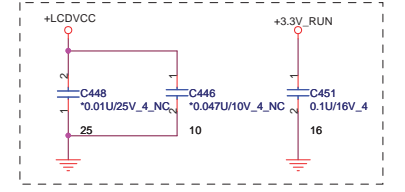
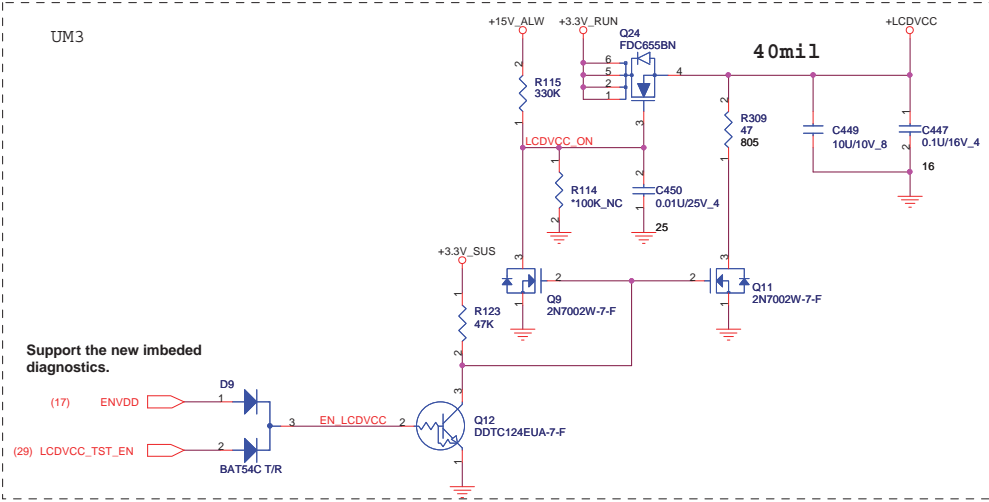
Quanta Computer Inc.
 PROJECT : UM9B/C DIS
 Size: Document Number
Madison_DDR3_A_512M
 Date: Monday, February 01, 2010 Sheet 19 of 51



Follow 9/9 mail, check GND.



Nut




Zener, Check P/N
<http://hobi-elektronika.net>

UM3


This page to CRT board

<http://hobi-elektronika.net>

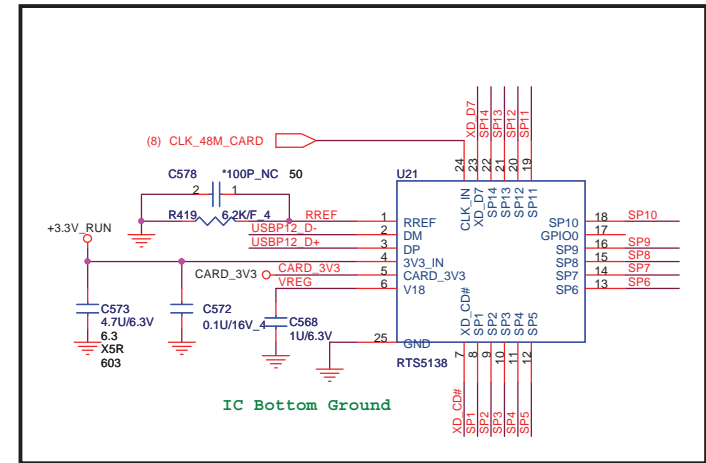
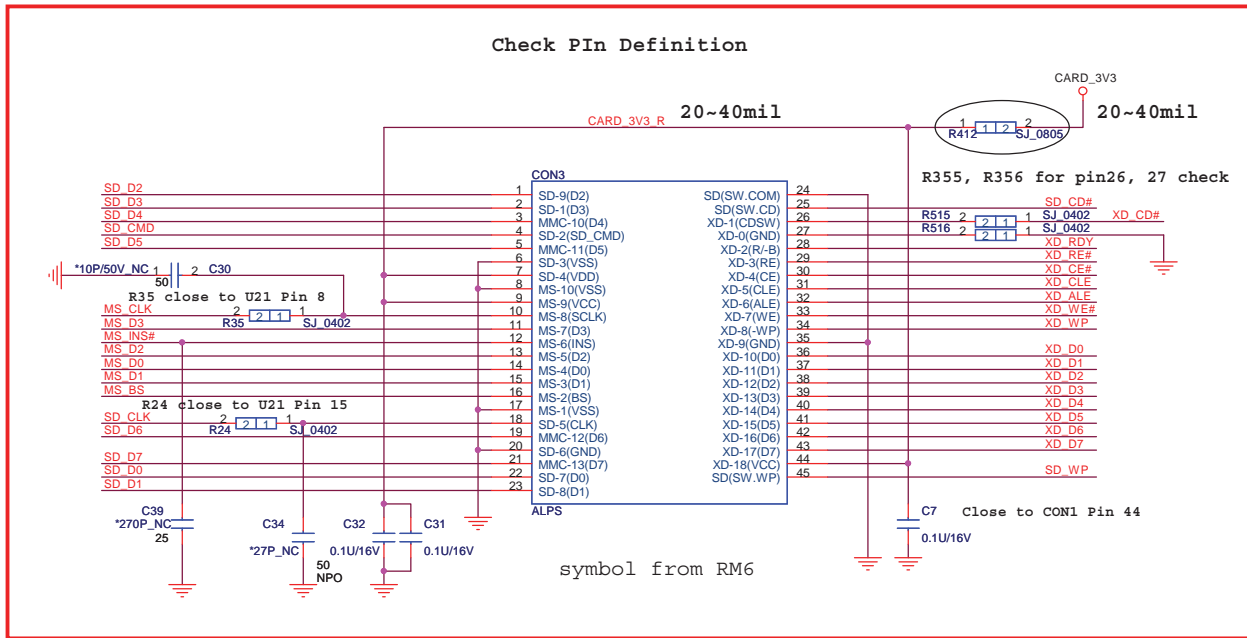
		Quanta Computer Inc.
		PROJECT : UM9B/C DIS
Size	Document Number	Rev
	CRT CONN	3A
Date:	Wednesday, January 27, 2010	Sheet 23 of 51

To CRT BOARD

<http://hobi-elektronika.net>

		Quanta Computer Inc.
		PROJECT : UM9B/C DIS
Size	Document Number	Rev
	DB CONN/Left USB	3A
Date:	Wednesday, January 27, 2010	Sheet 24 of 51

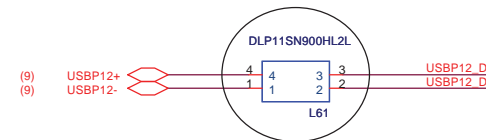
Check PIn Definition

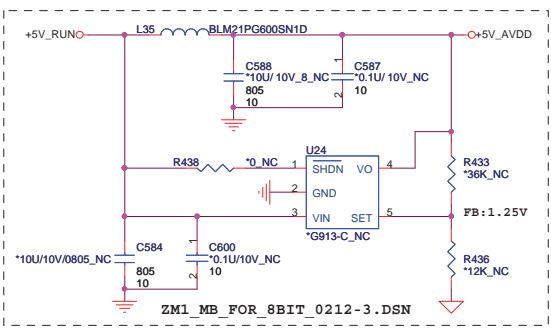


RTS5138 - QFN24

SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D3
SP4	XD CLE	SD D7	MS D7
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6	SD D1	MS BS

Share Pin





UM3, symbol from PDC

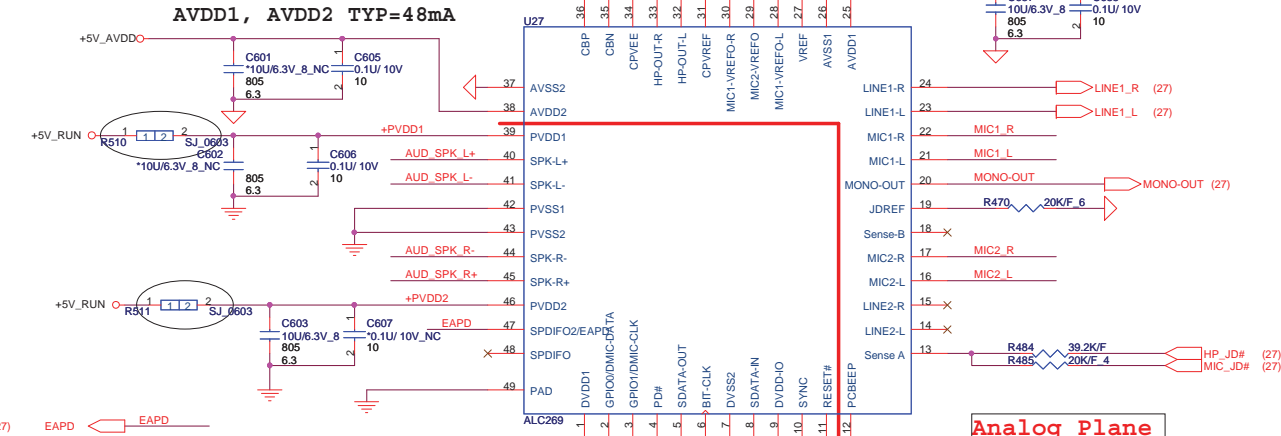
*NOTE: ALC269_VB type add the LDO circuit in IC

PIN NAME	R457	R455	R456	C636	CODEC IC
28 MIC1_VREF0-L			POP	NC	ALC269
31 CPVREF	POP	NC			VA

VA type: PIN28 作為MIC之偏壓
PIN31接A-GND

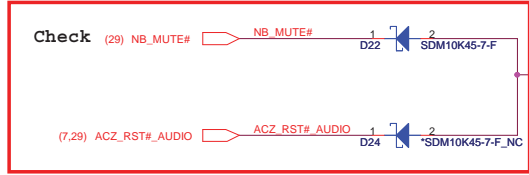
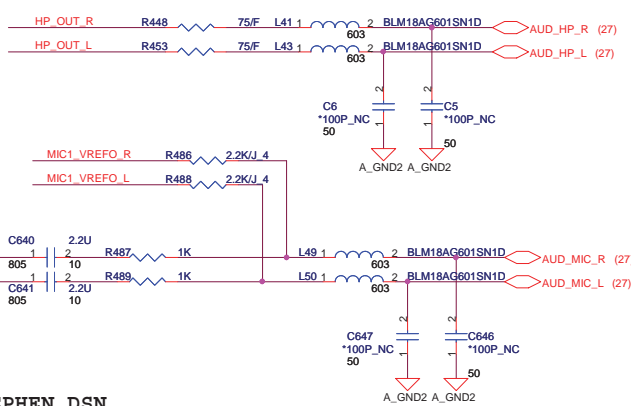
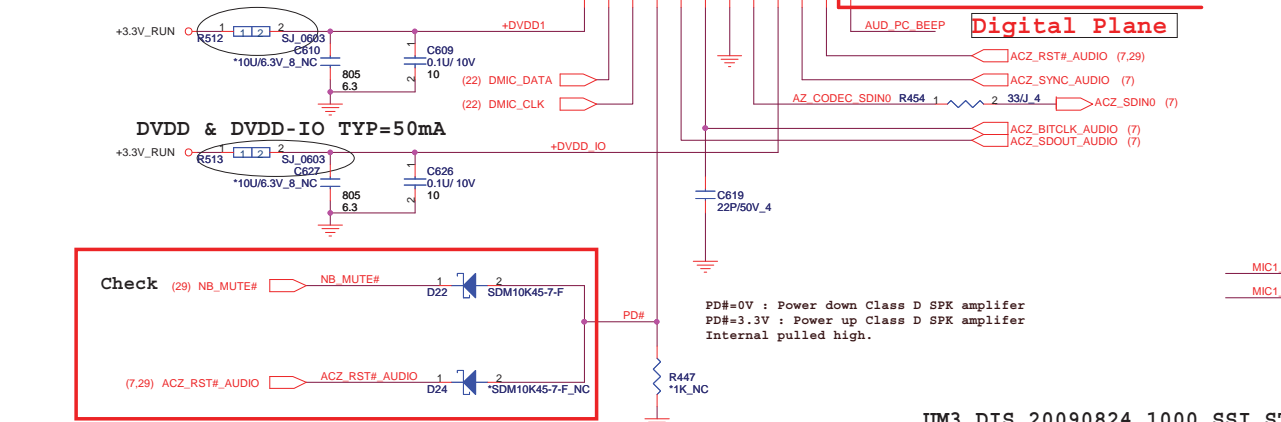
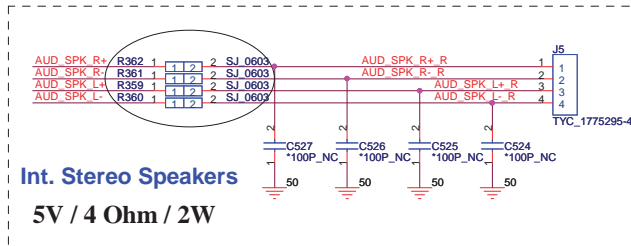
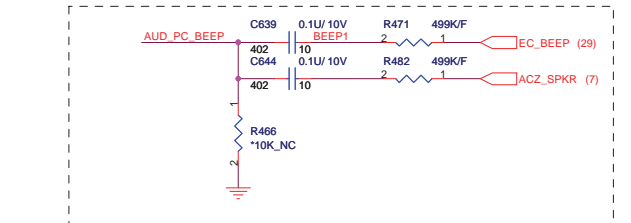
PIN NAME	R457	R455	R456	C636	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269
31 CPVREF	NC	POP			VB

VB type: PIN31 作為MIC之偏壓
PIN28接CAP作為內部LDO
output 輸出濾波用



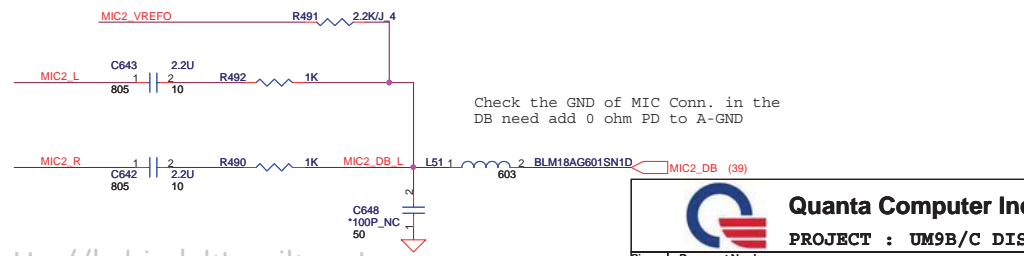
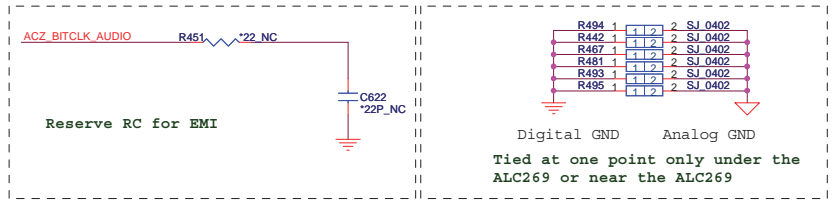
Analog Plane

Digital Plane



PD#=0V : Power down Class D SPK amplifier
PD#=3.3V : Power up Class D SPK amplifier
Internal pulled high.

UM3_DIS_20090824_1000_SSI_STEPHEN.DSN



Check the GND of MIC Conn. in the DB need add 0 ohm PD to A-GND

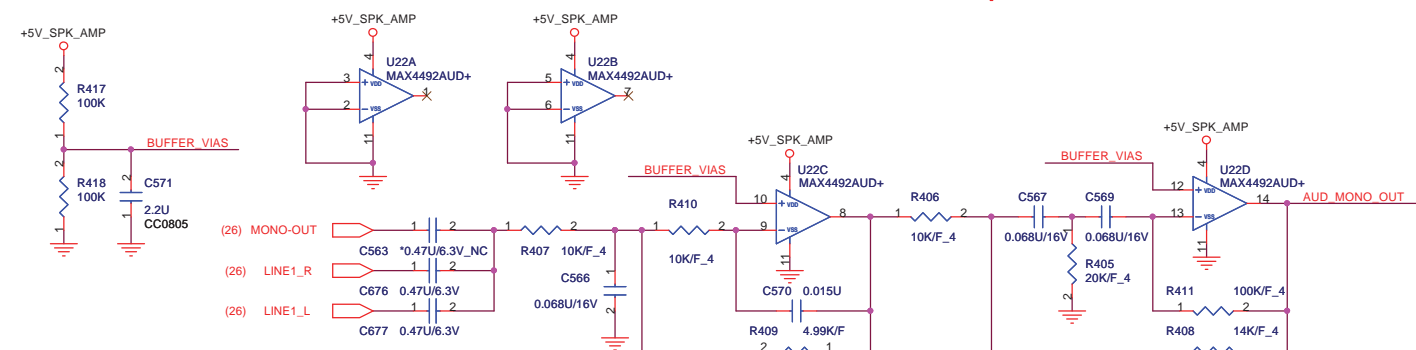
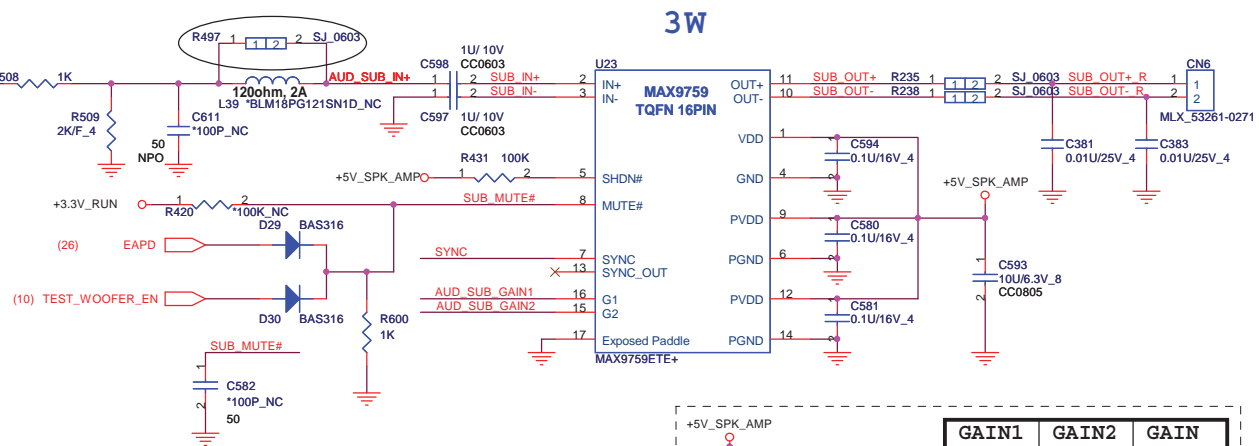
<http://hobi-elektronika.net>

Quanta Computer Inc.
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INTERNAL SUBWOOFER AMP Only for 17''

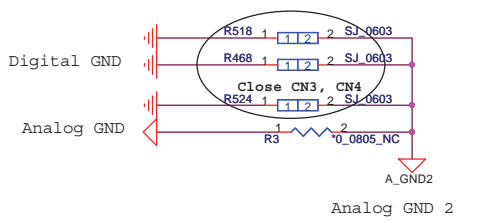
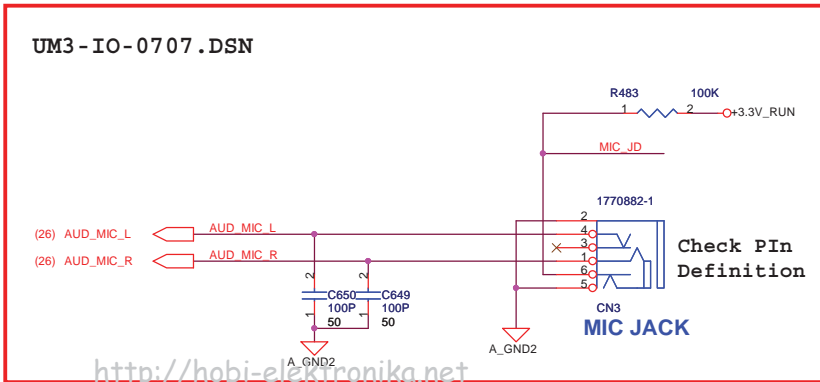
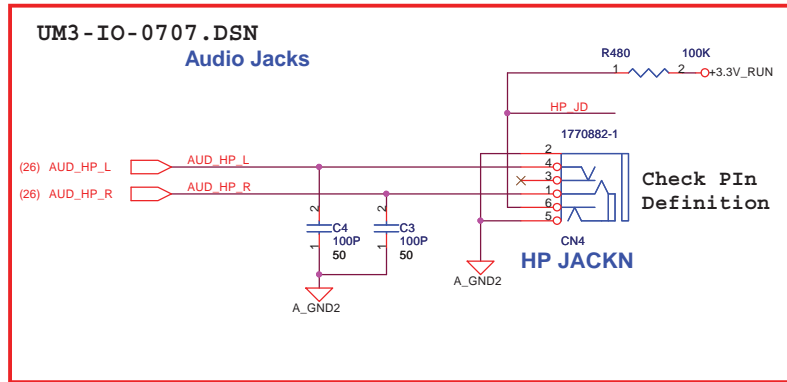
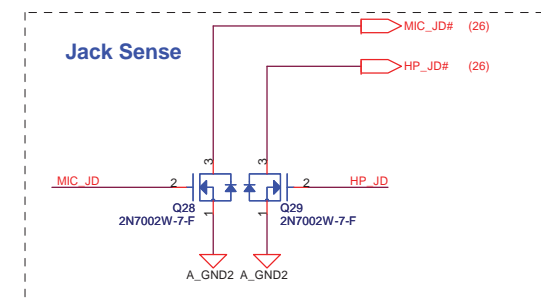
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB


FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
 Layout Note:
 Place close to pin 8.

NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_PD#	SUB_MUTE#
0	0	L (Disable SPK)	L (Disable Woofer)
0	1	L (Disable SPK)	H (Test Woofer)
1	0	H (Test SPK)	L (Disable Woofer)
1	1	H (Test SPK)	H (Test Woofer)





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(34) KSO[0..17]
(34) KSI[0..7]

ITE8502E LQFP-128L

- KSO17 57 KSO17/GPC5
- KSO16 56 KSO16/GPC3
- KSO15 55 KSO15
- KSO14 54 KSO14
- KSO13 53 KSO13
- KSO12 52 KSO12/SLCT
- KSO11 51 KSO11/ERR
- KSO10 49 KSO10/PE
- KSO9 48 KSO9/BUSY
- KSO8 44 KSO8/ACK
- KSO7 43 KSO7/PD7
- KSO6 42 KSO6/PD6
- KSO5 41 KSO5/PD5
- KSO4 40 KSO4/PD4
- KSO3 39 KSO3/PD3
- KSO2 38 KSO2/PD2
- KSO1 37 KSO1/PD1
- KSO0 36 KSO0/PD0
- KS17 65 KS17
- KS16 64 KS16
- KS15 63 KS15
- KS14 62 KS14
- KS13 61 KS13/SLIN
- KS12 60 KS12/INT
- KS11 59 KS11/AFD
- KS10 58 KS10/STB

KEYBOARD

ADC/DAC

PWM

LPC

IR/UART

SMBUS

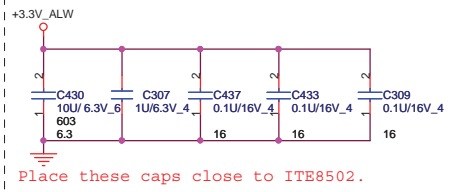
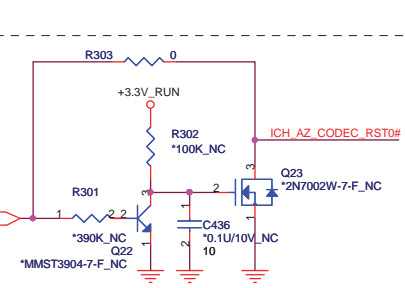
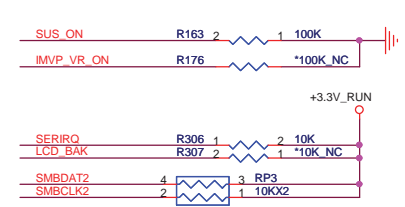
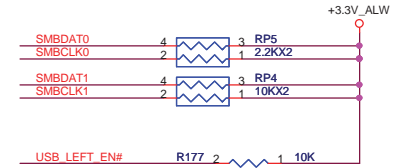
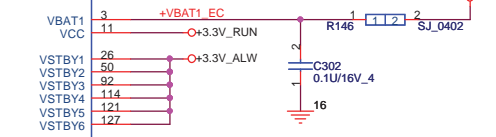
PS/2

GPIO

LPC/FWH FLASH

RGPC

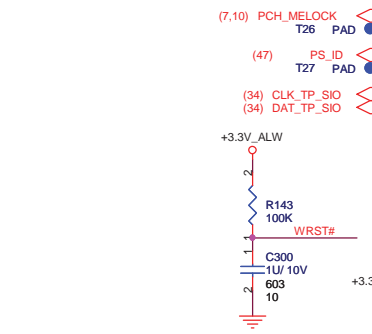
Board ID Straps



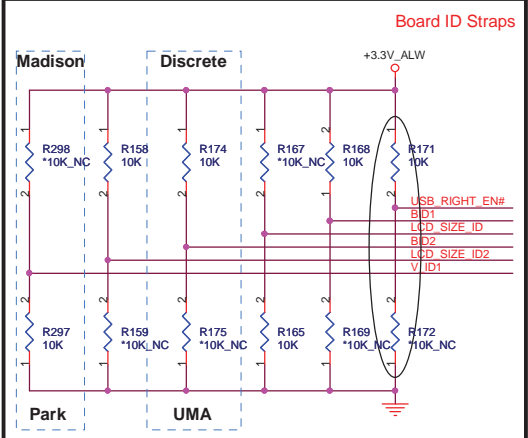
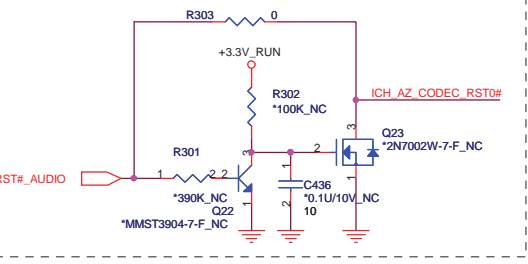
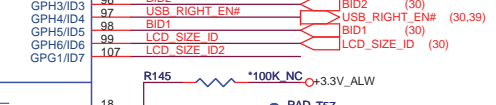
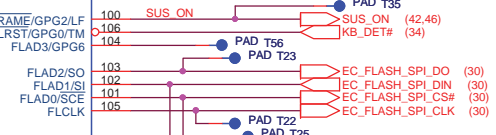
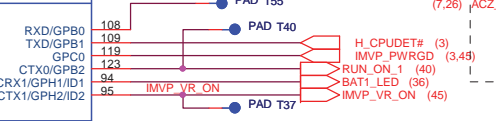
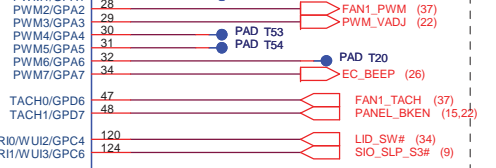
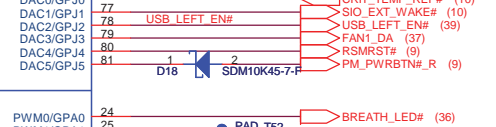
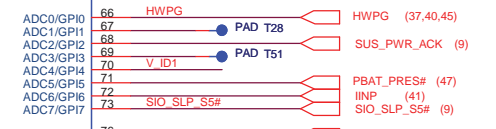
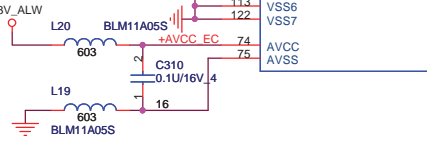
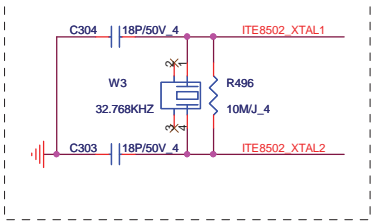
Place these caps close to ITE8502.

SERIRO
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT
PCH
VGA, LAN, Clock
Thermal IC



32KHz Clock.(Layout close to EC)

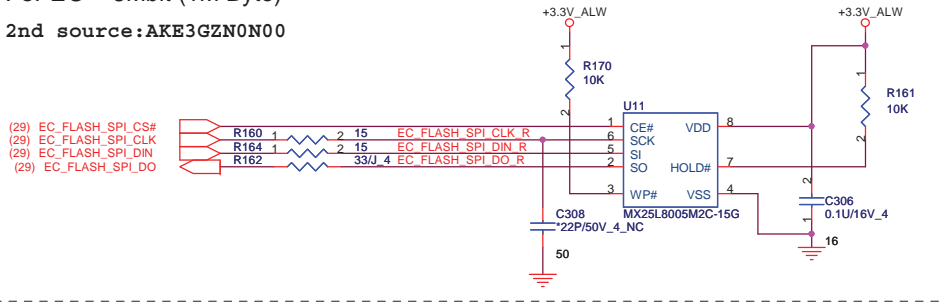


BID1	BID0	UM9(UMA)	UM9C(Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	(A01)	(A01)

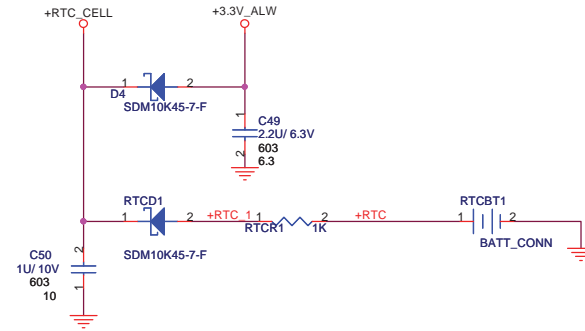
	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13.3"	0	0
14"	1	0
17"	0	1

For EC 8Mbit (1M Byte)

2nd source:AKE3GZNON00



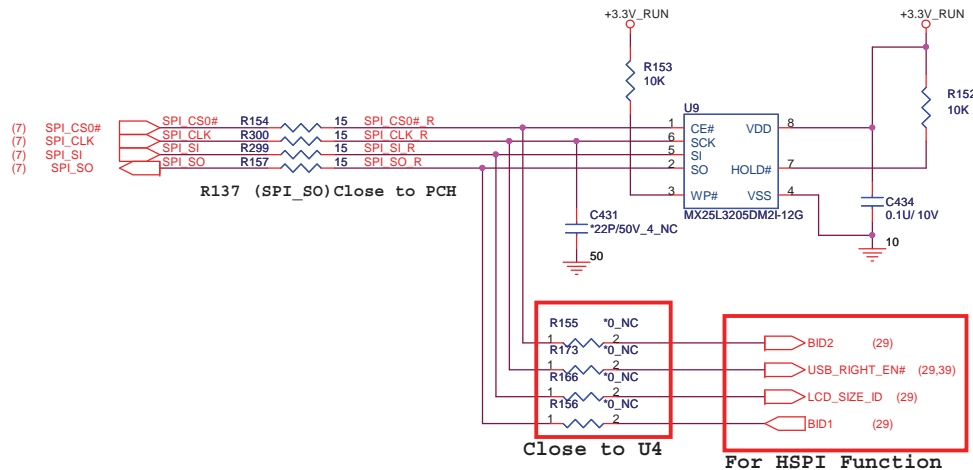
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZPON00



UM3

WWAN To DB

<http://hobi-elektronika.net>

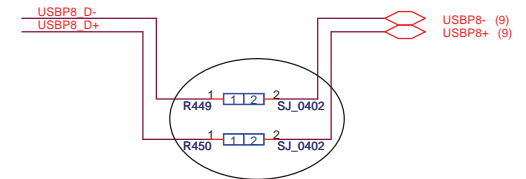
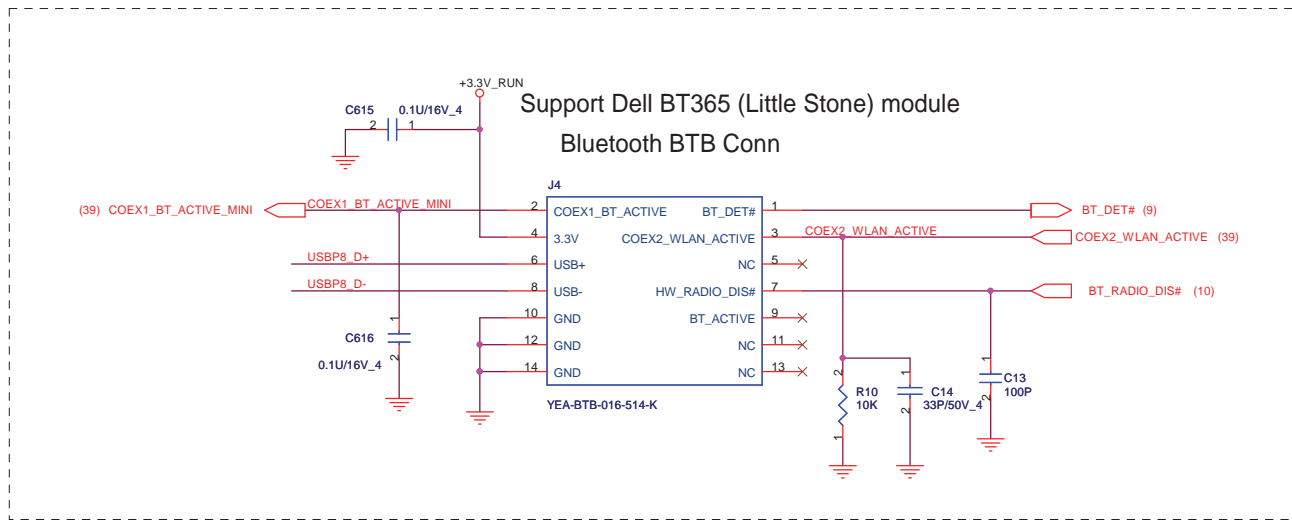


Quanta Computer Inc.

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	MINI-Card WWAN	3A
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WLAN To DB



eSATA and USB To DB

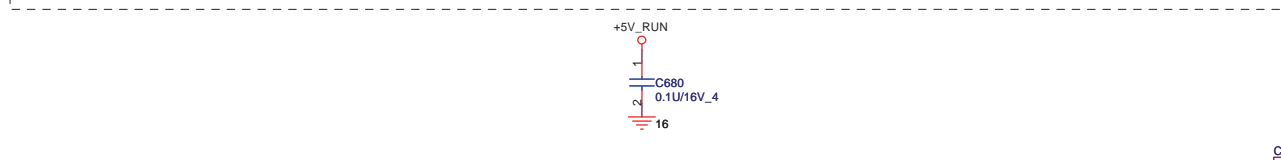
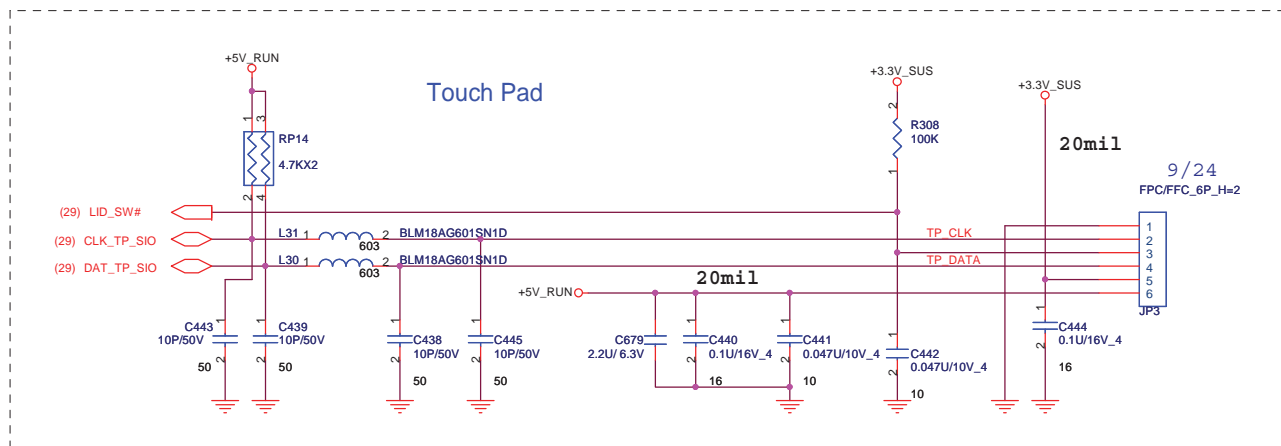
<http://hobi-elektronika.net>



Quanta Computer Inc.

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	eSATA & Right USB	3A
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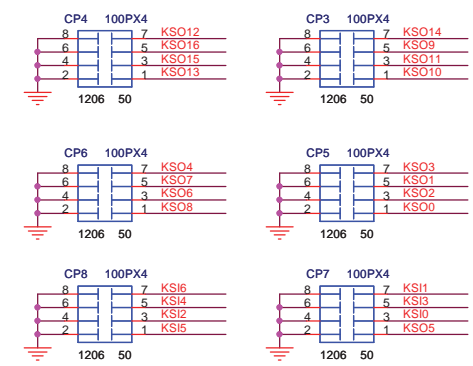
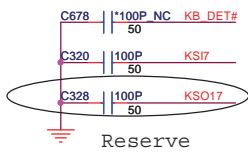
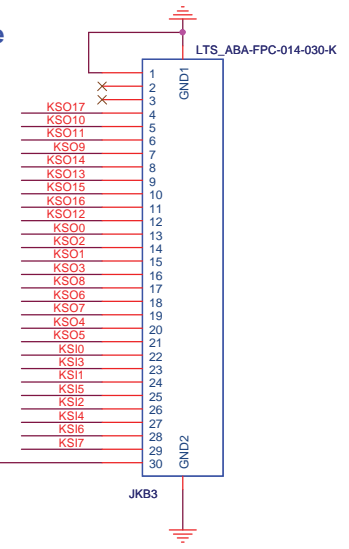


UM3 KEYBOARD CONNECTOR

Top side

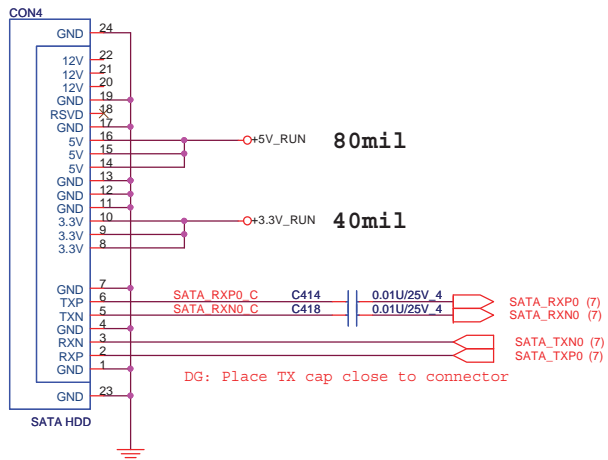
(29) KSO[0..17]
 (29) KSI[0..7]

Check KB detect function
 UM9 no KSO17



100P CAPS CLOSE TO JKB3

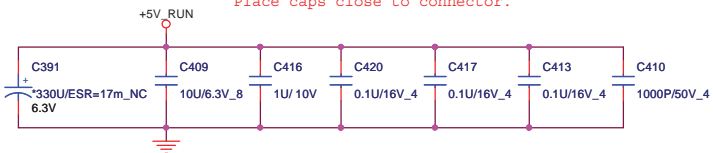
SATA Connector.



+3.3V_RUN Place caps close to connector.

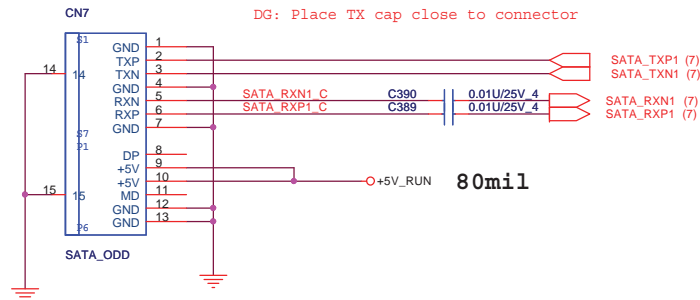


+5V_RUN Place caps close to connector.

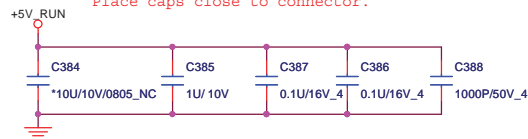


UM3

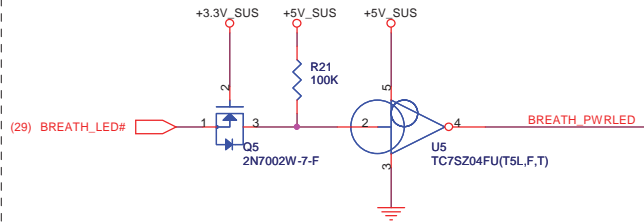
ODD Connector



Place caps close to connector.

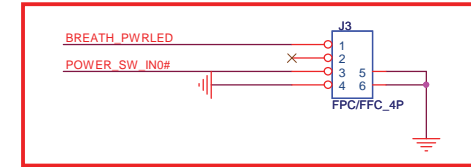


Power

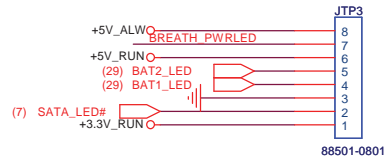


UM3

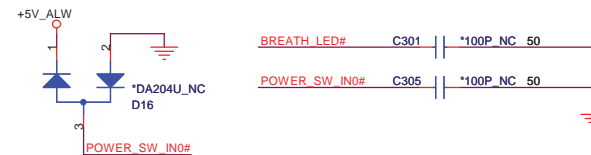
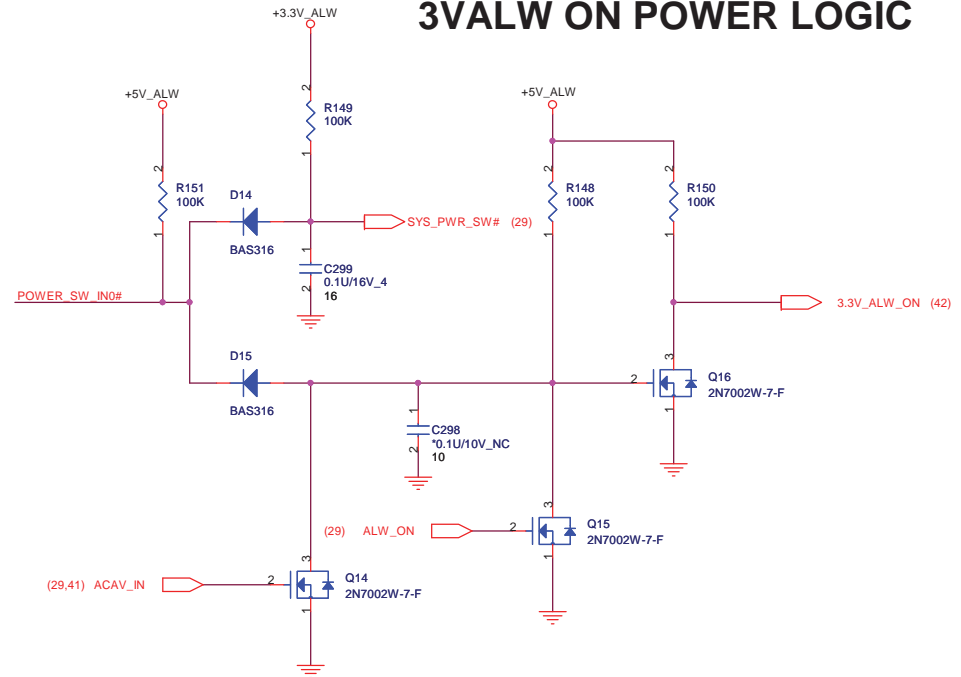
Power button Cable



Check Connector P/N and footprint

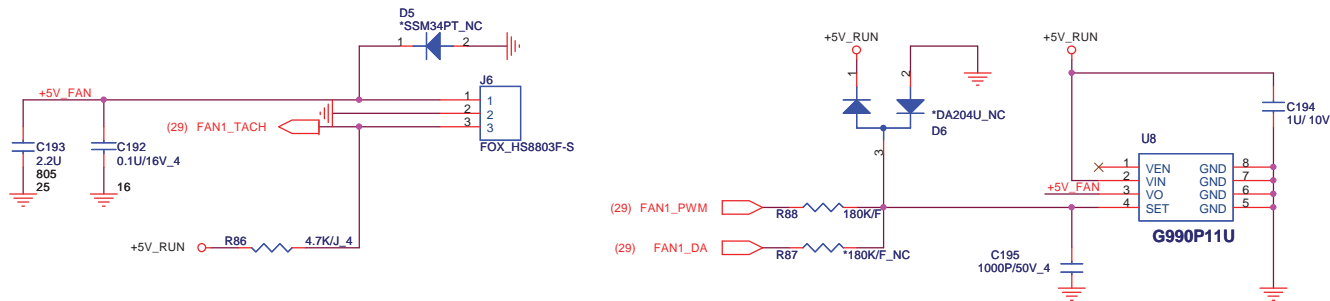


3VALW ON POWER LOGIC

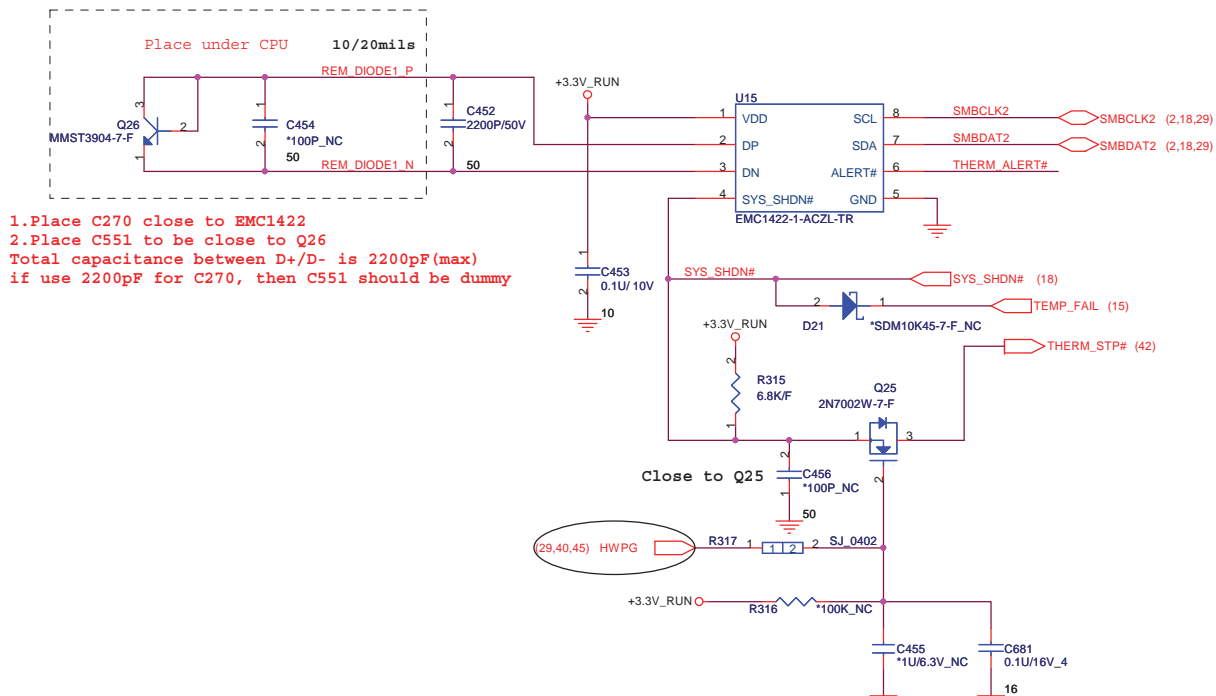


FAN CONTROL

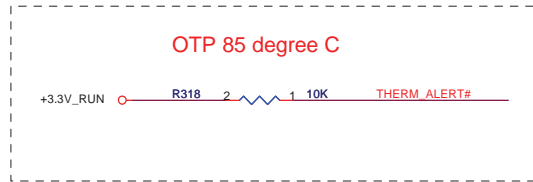
6/23 COPY FROM RM6



UM3




1. Place C270 close to EMC1422
 2. Place C551 to be close to Q26
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C270, then C551 should be dummy

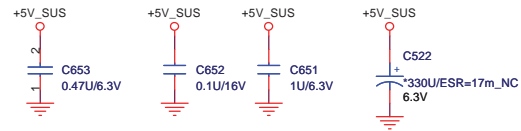
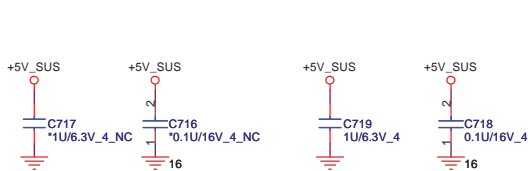
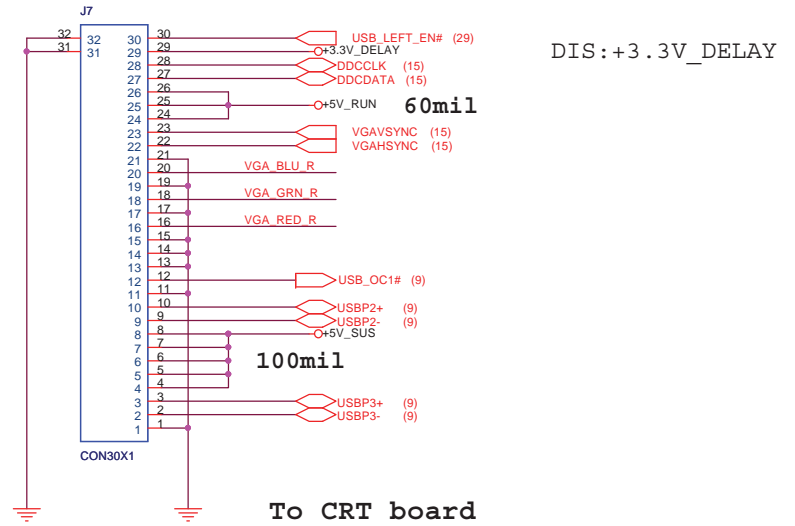
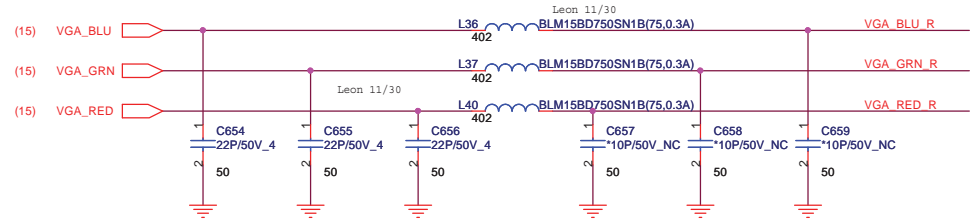
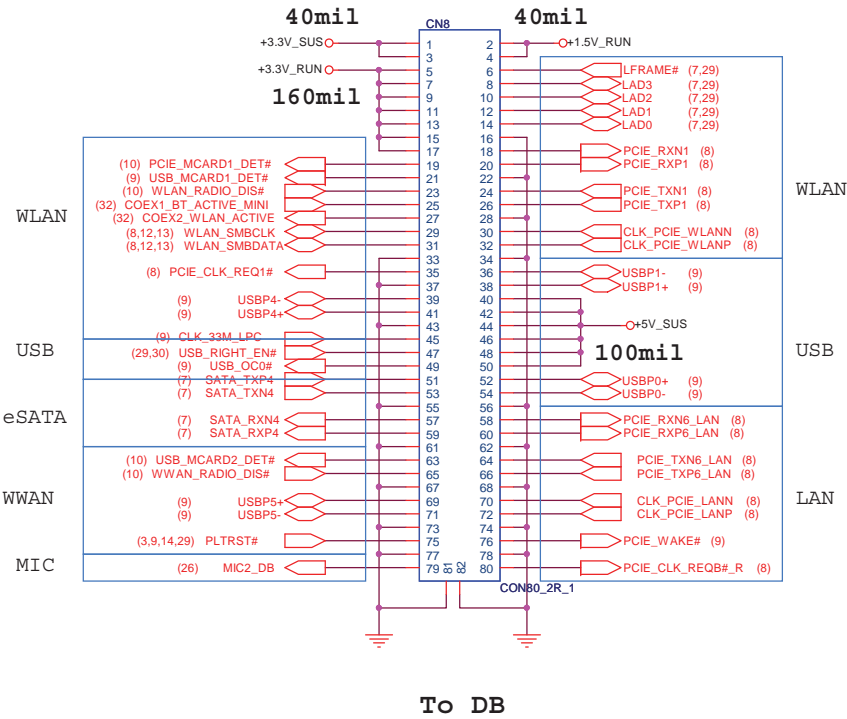


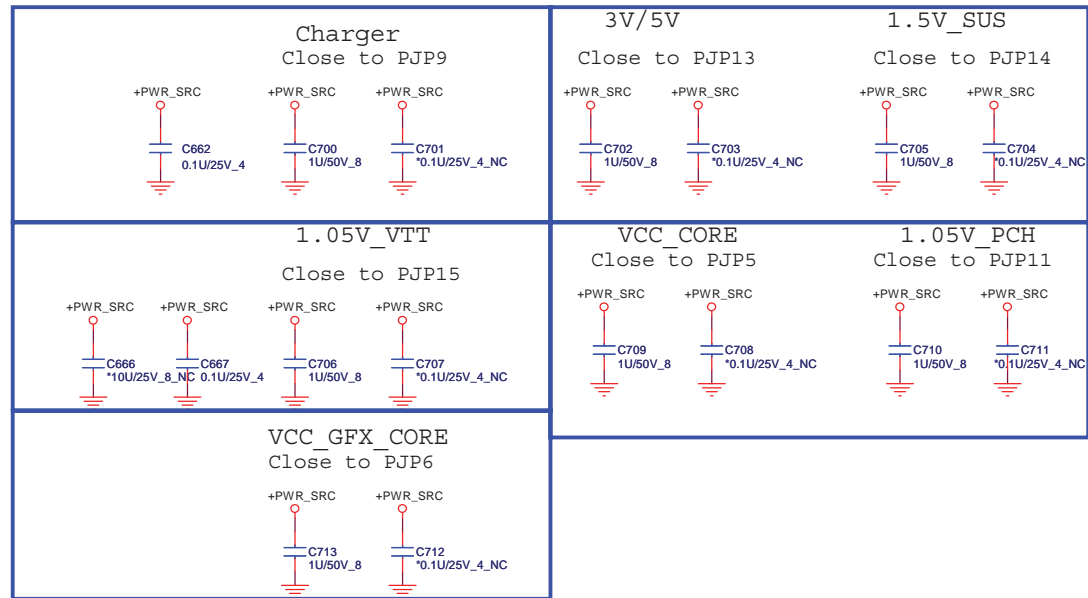
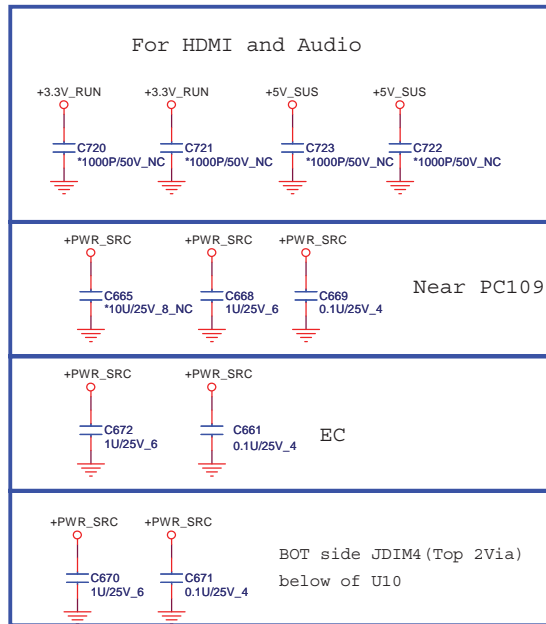
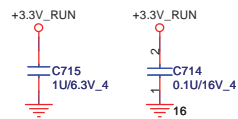
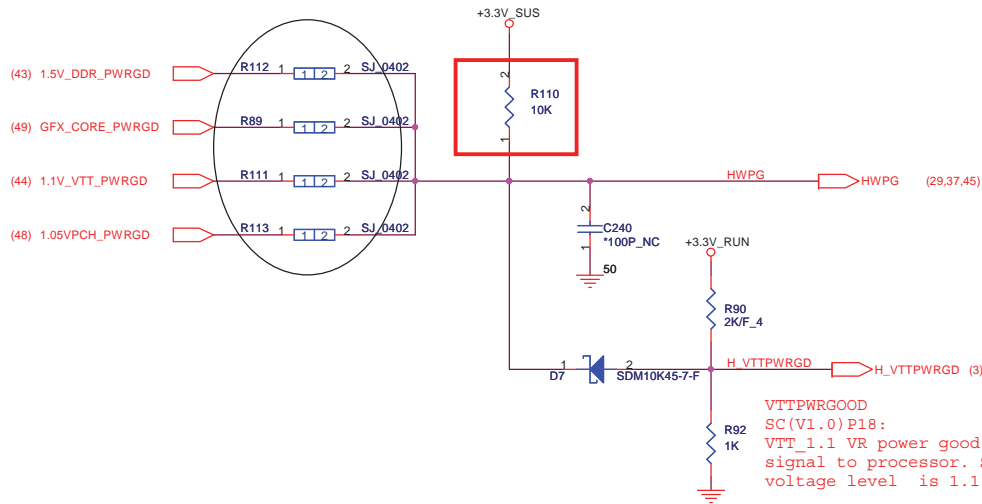
<http://hobi-elektronika.net>

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		FAN & THERMAL Date: Monday, February 01, 2010 Sheet 37 of 51

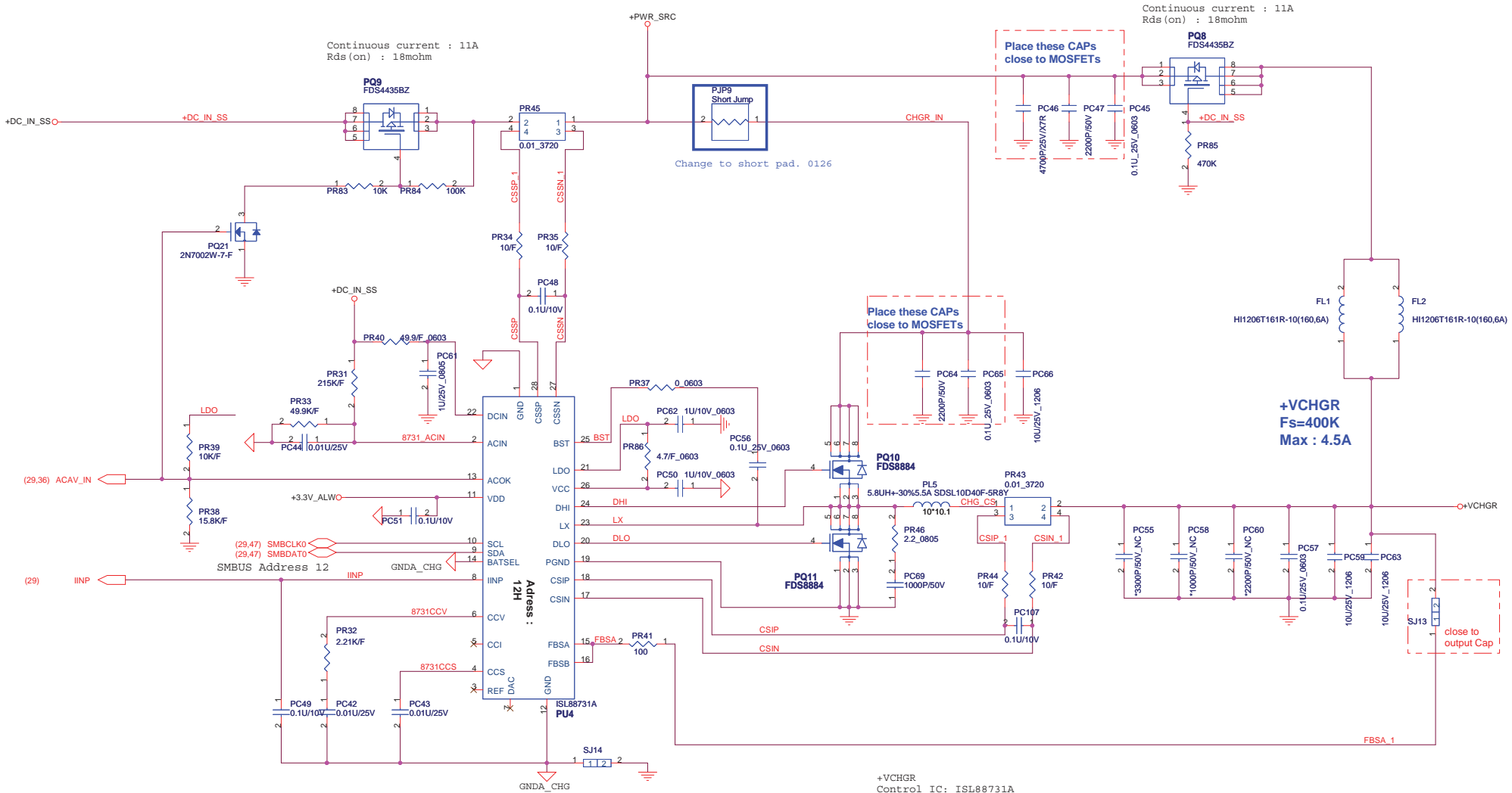
LAN To DB

		Quanta Computer Inc.
		PROJECT : UM9B/C DIS
Size	Document Number	Rev
	LAN(AR8152/RJ-45)	3A
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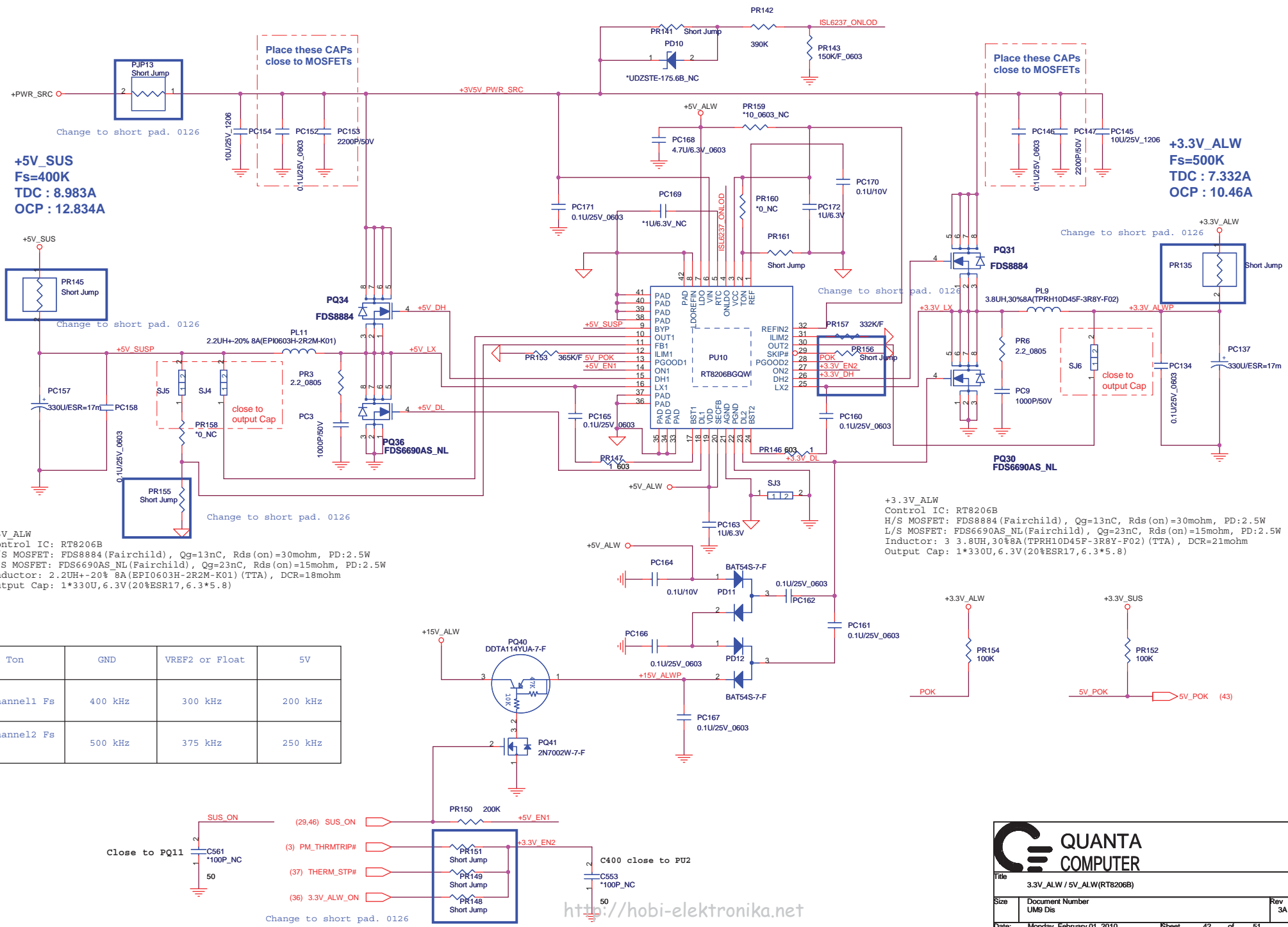


UM9-MADISON-0909 OF POWER.DSN



+VCHGR
 Control IC: ISL88731A
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 Inductor: 5.8uH +30% 5.5A SDSL10D40F-5R8Y (TTA), DCR=21mohm
 Output Cap: 2*10u 25V (+-10%, X6S, 1206)

		Title	
		Charger (ISL88731)	
Size	Document Number	Rev	
UM9 Dis		3A	
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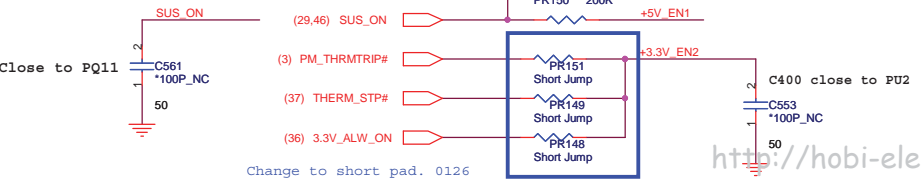
+5V_SUS
Fs=400K
TDC : 8.983A
OCP : 12.834A

+3.3V_ALW
Fs=500K
TDC : 7.332A
OCP : 10.46A

+5V_ALW
 Control IC: RT8206B
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS_NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 2.2UH+20% 8A (EPI0603H-2R2M-K01) (TTA), DCR=18mohm
 Output Cap: 1*330U, 6.3V (20%ESR17, 6.3*5.8)

+3.3V_ALW
 Control IC: RT8206B
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS_NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 3.8UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
 Output Cap: 1*330U, 6.3V (20%ESR17, 6.3*5.8)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



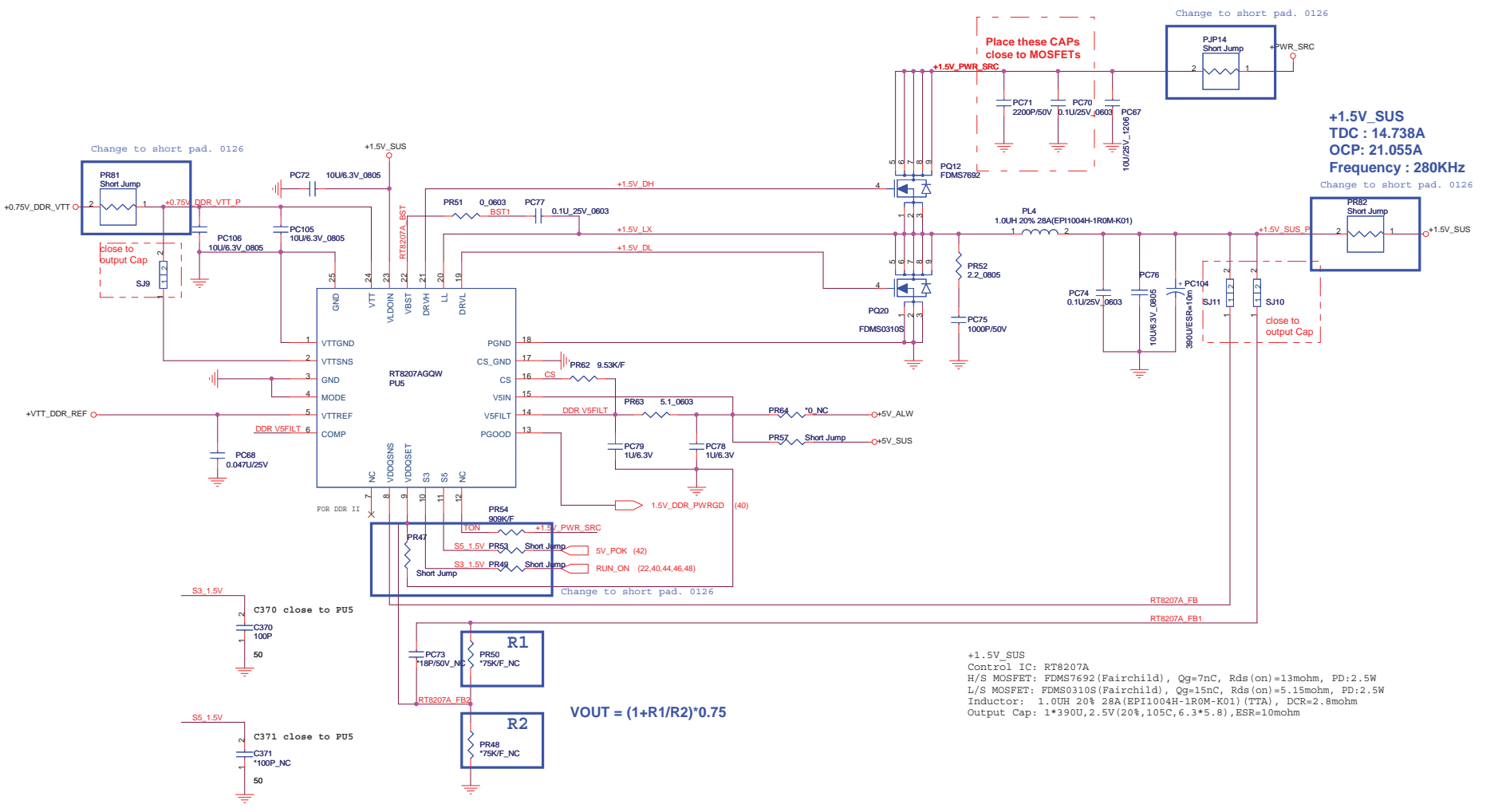
<http://hobi-elektronika.net>

**QUANTA
COMPUTER**

Title: 3.3V_ALW / 5V_ALW (RT8206B)

Size	Document Number	Rev
	UMG Dis	3A

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$$V_{OUT} = (1 + R1/R2) * 0.75$$

+1.5V_SUS
 Control IC: RT8207A
 H/S MOSFET: FDMS7692 (Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
 L/S MOSFET: FDMS0310S (Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
 Inductor: 1.0UH 20% 28A (EPI1004H-1R0M-K01) (TTA), DCR=2.8mohm
 Output Cap: 1*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

VDDQ and VTT discharge control

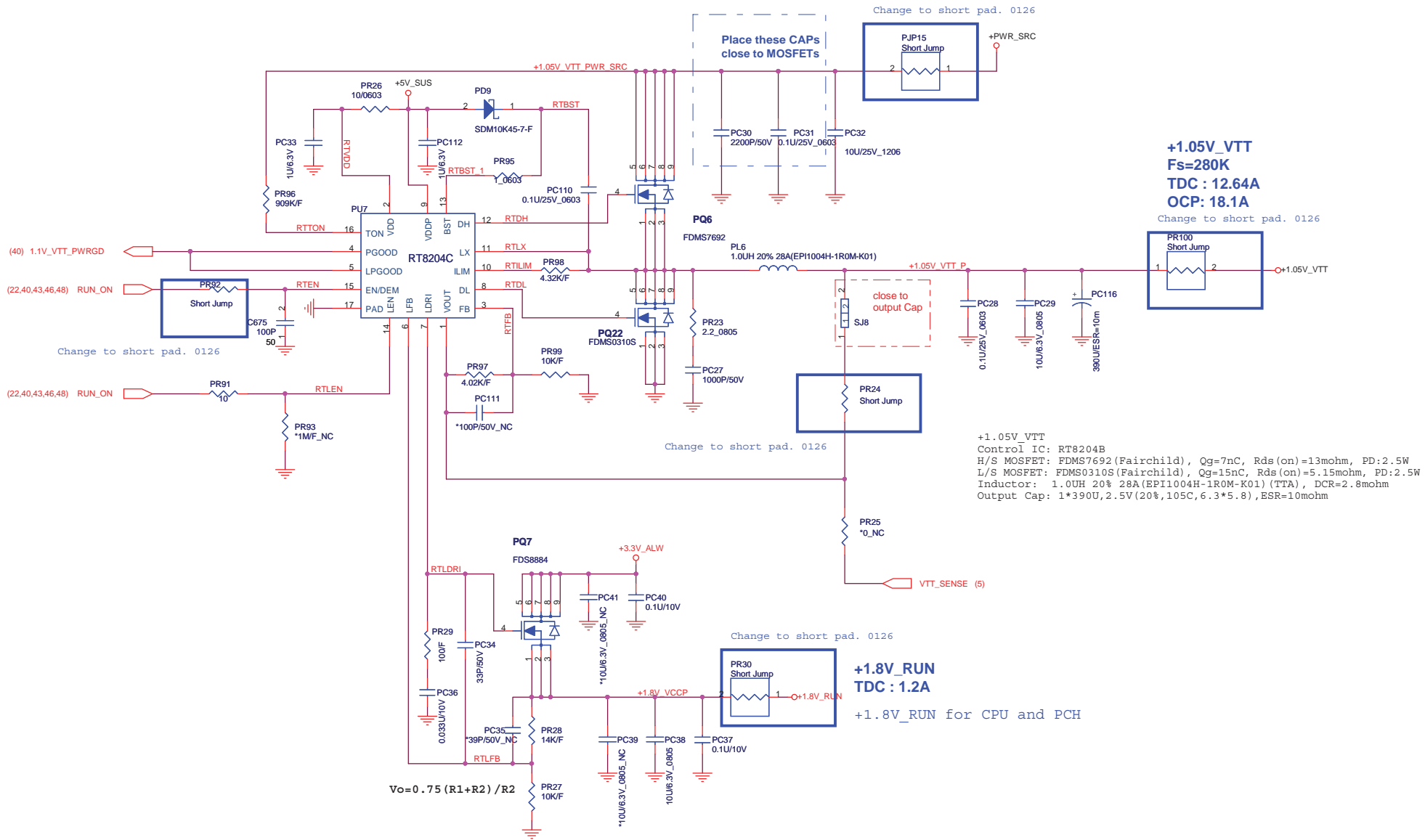
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

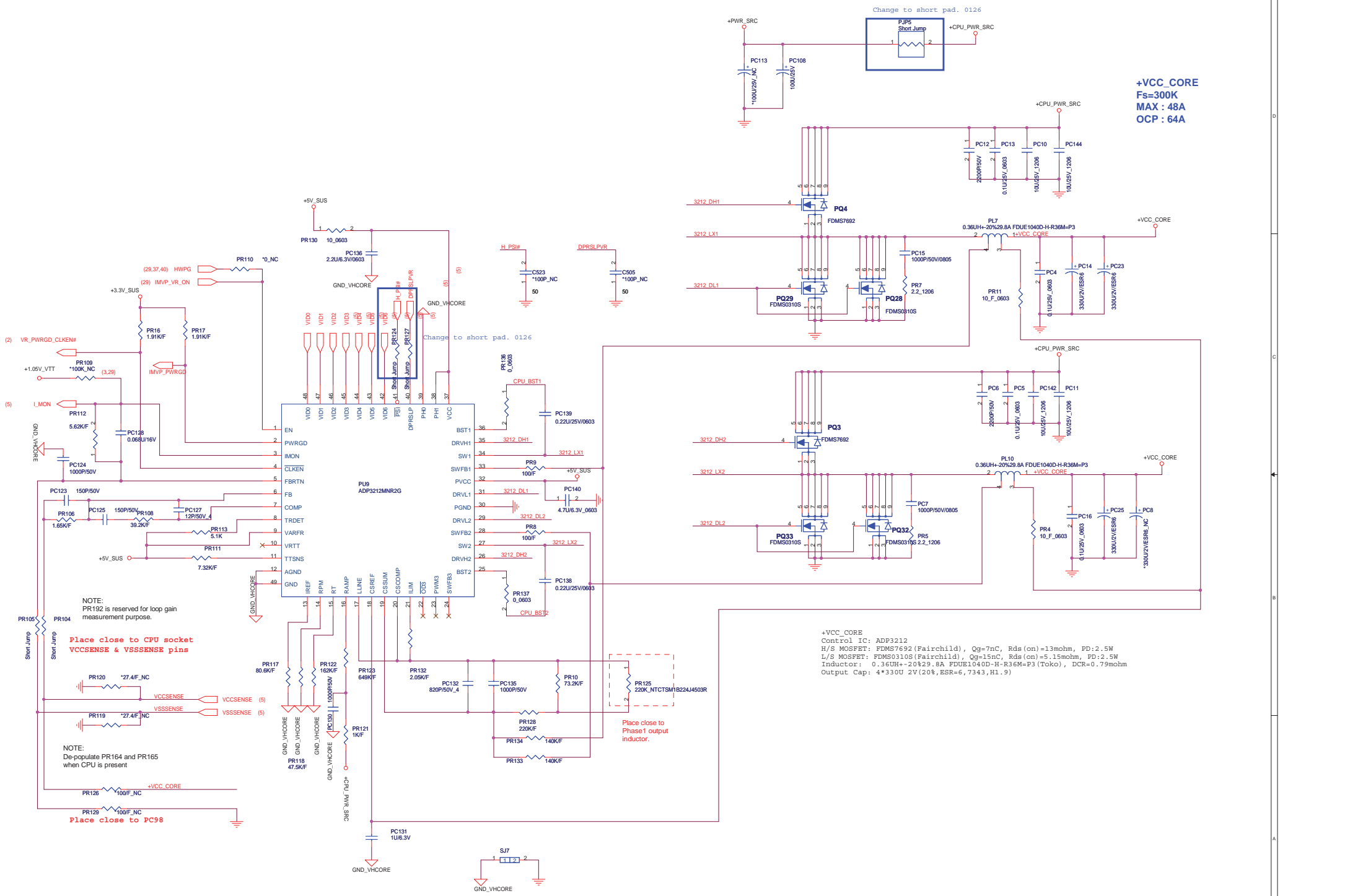
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



Title		
+1.05V_VTT(RT8204C)		
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	UMG Dis	3A
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+VCC_CORE
Fs=300K
MAX : 48A
OCF : 64A

NOTE:
 PR192 is reserved for loop gain measurement purpose.

Place close to CPU socket
VCCSENSE & VSSSENSE pins

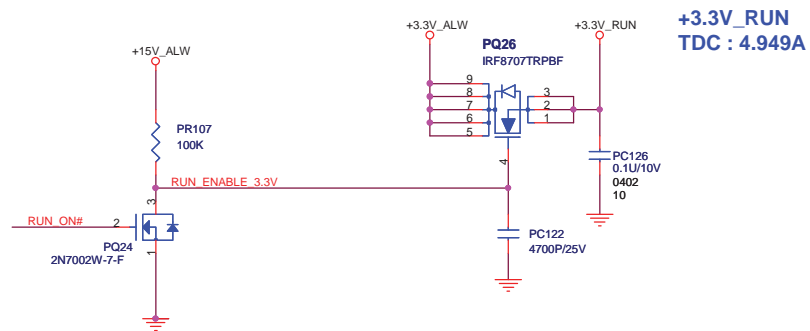
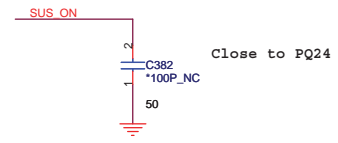
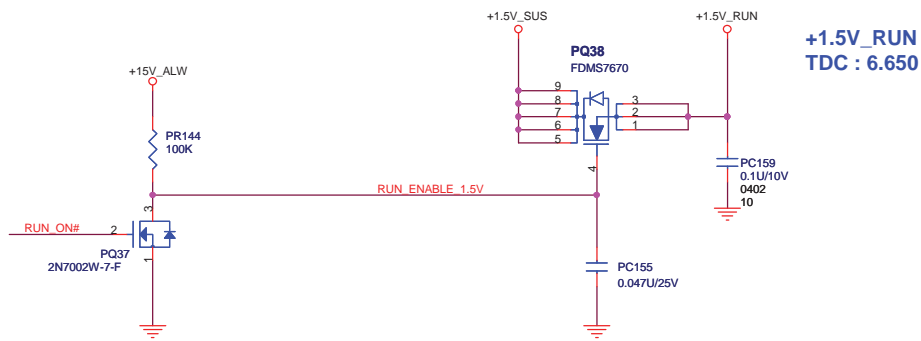
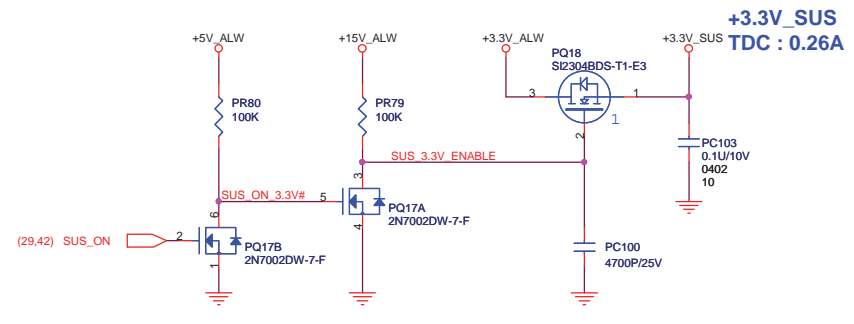
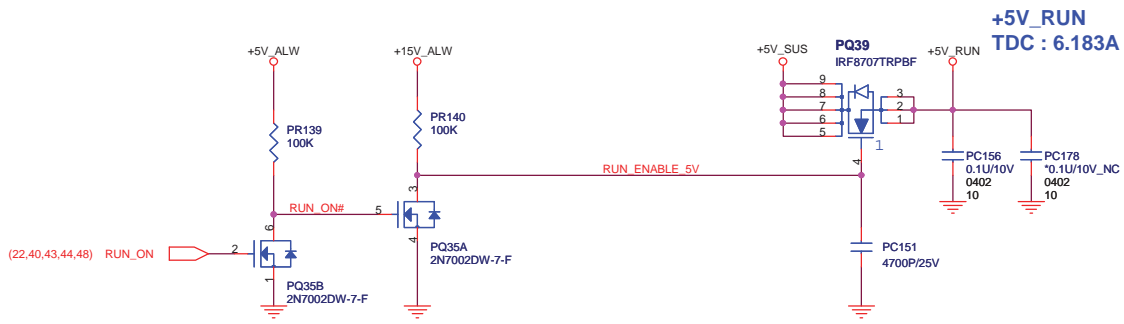
NOTE:
 De-populate PR164 and PR165 when CPU is present

Place close to CPU socket
VCCSENSE & VSSSENSE pins

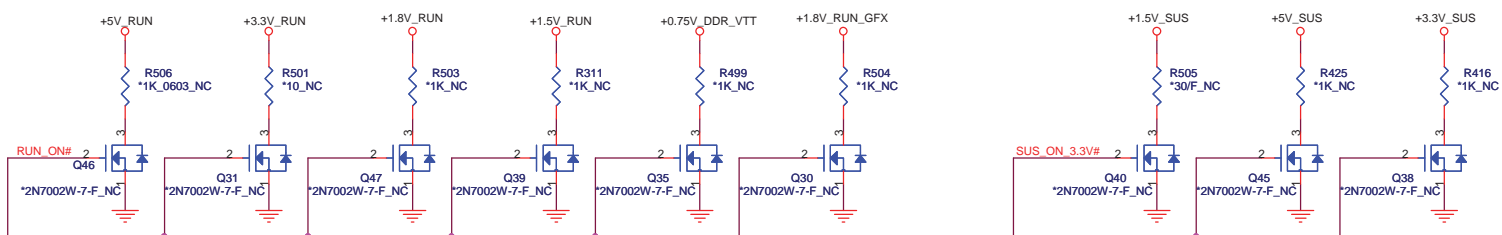
Place close to Phase1 output inductor.

+VCC_CORE
 Control IC: ADP3212
 H/S MOSFET: FDM57692 (Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
 L/S MOSFET: FDM5310S (Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
 Inductor: 0.36uH+20%±29.8A FDUE1040D-H-R36M-P3 (Tokko), DCR=0.79mohm
 Output Cap: 4*330U 2V(20%,ESR=6,7343,H1.9)

Title		CPU core (ADP3212MNR2G)	
Size	Document Number	Rev	
UMB Dis		3A	
Date:	Monday, February 01, 2010	Sheet	45 of 51



Reserve discharge path



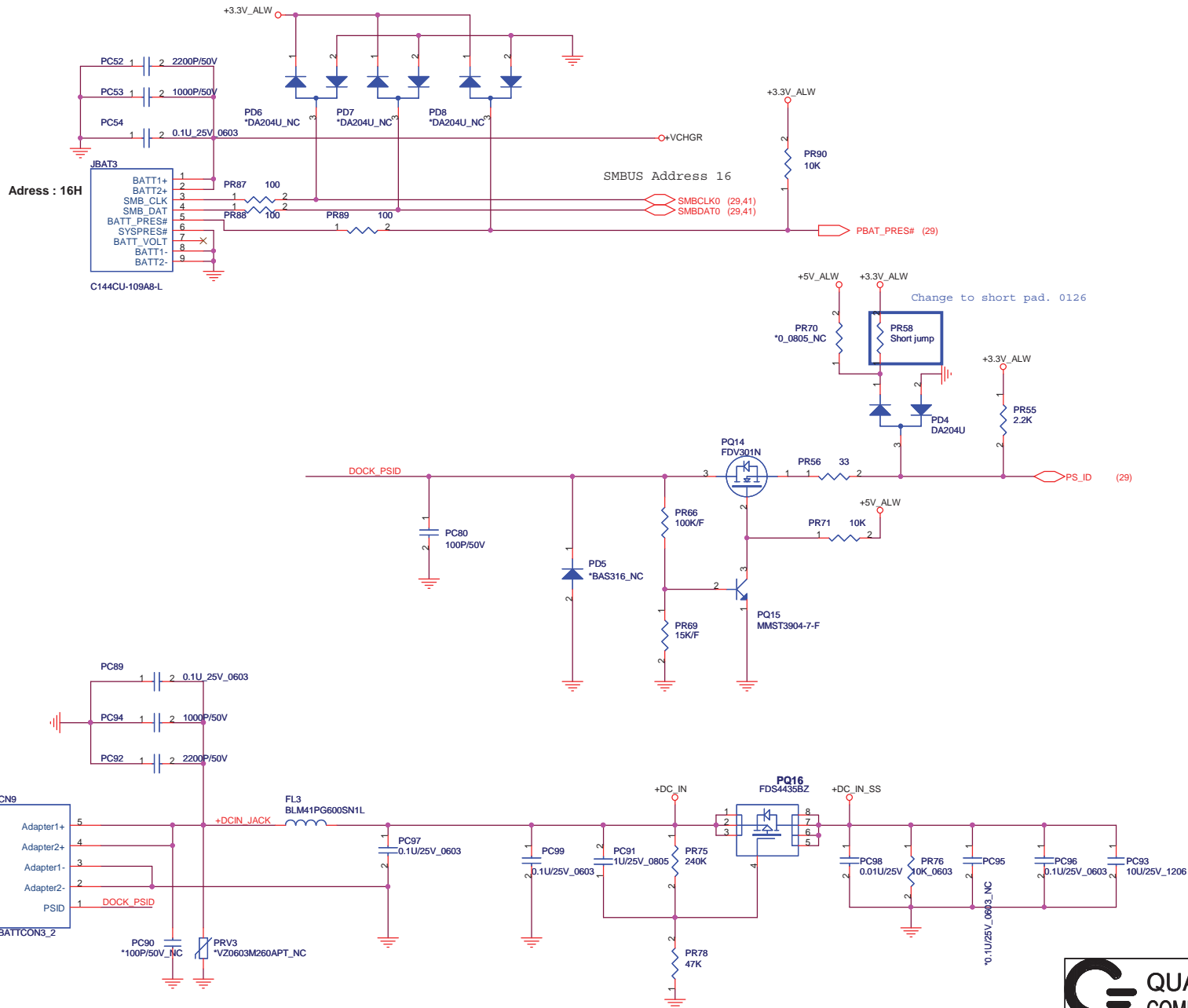
<http://hobi-elektronika.net>

**QUANTA
COMPUTER**

Title: RUN / SUS POWER SW

Size	Document Number UMG Dis	Rev 3A
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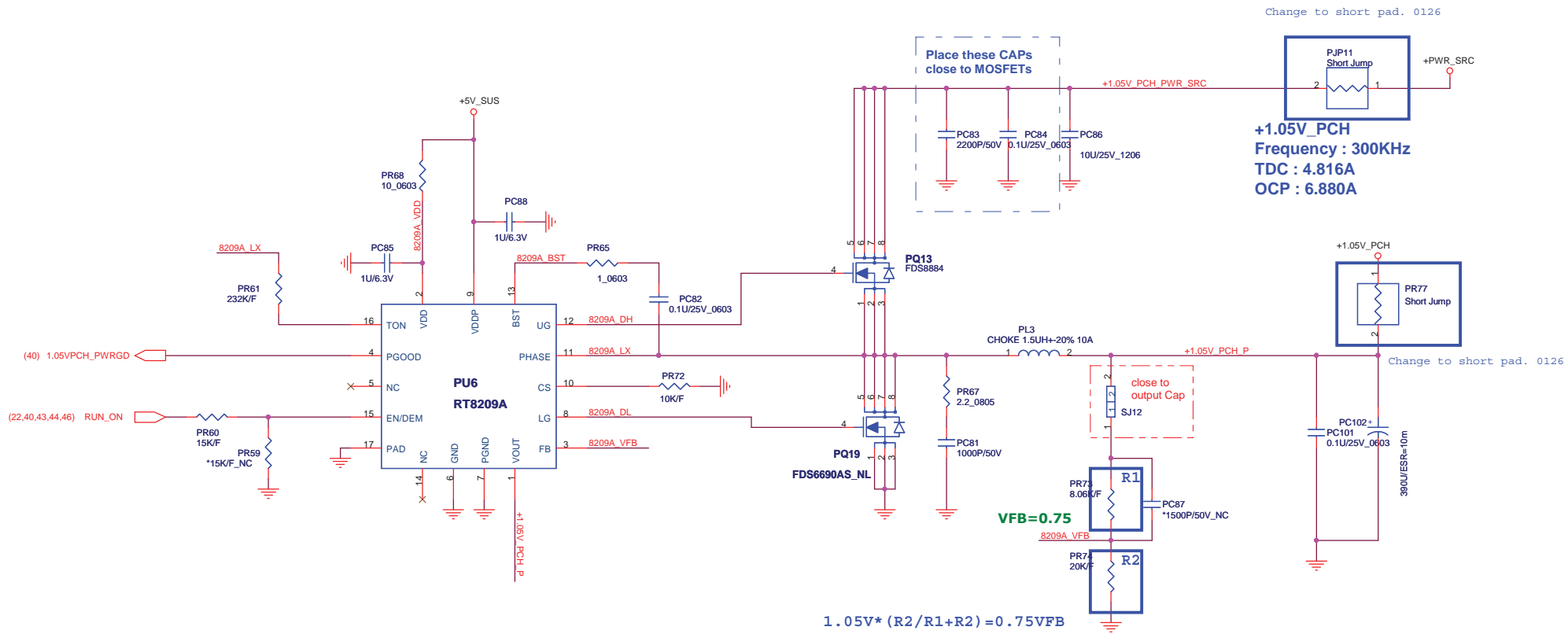
Date: Monday, February 01, 2010 Sheet 46 of 51



Change to short pad. 0126

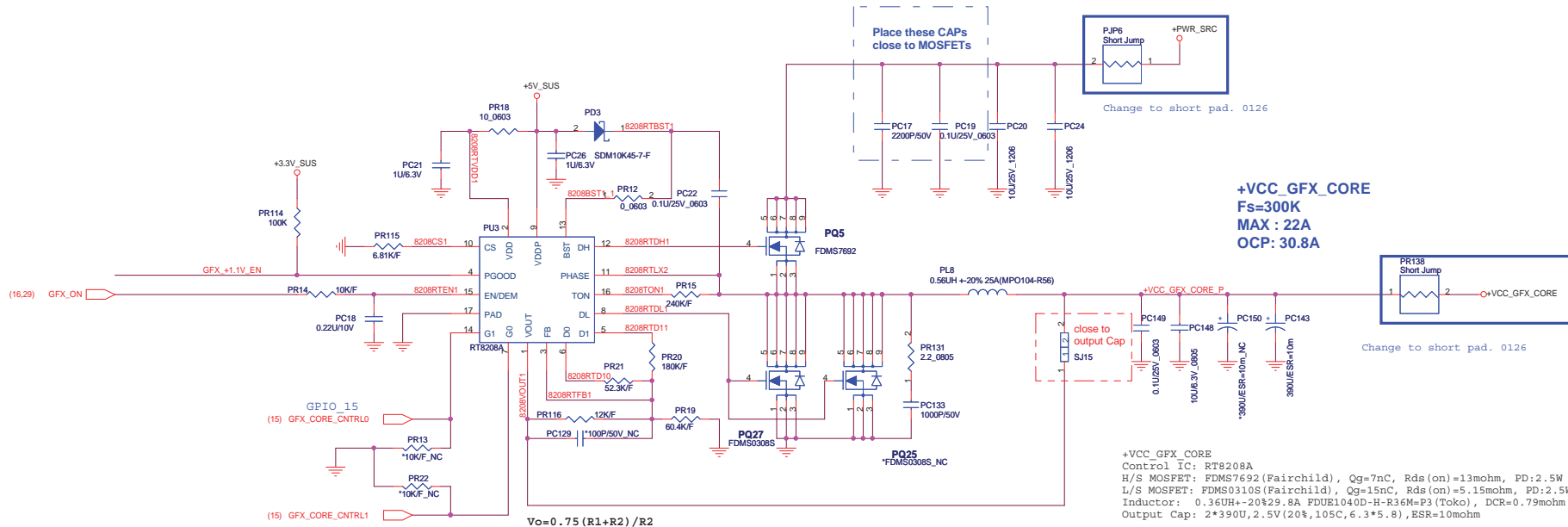


Title DCIN,BATT CONNECTOR		
Size UM9 Dis	Document Number UM9 Dis	Rev 3A
Date: Monday, February 01, 2010	Sheet 47	of 51



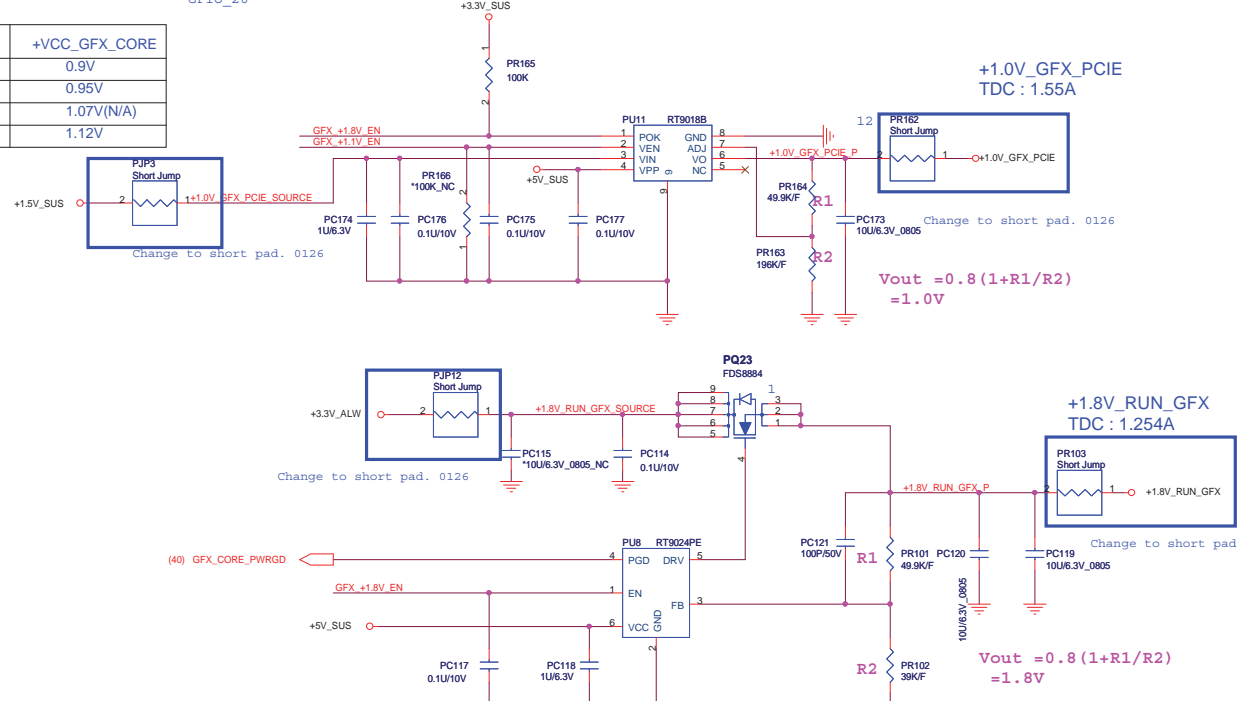
+1.05V_PCH
 Control IC: RT8209A
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD=2.5W
 L/S MOSFET: FDS6690AS_NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD=2.5W
 Inductor: 1.5uH+-20% 9A (10D40F-1R5M) (TTA), DCR=10.5mohm
 Output Cap: 1*390u, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

Title		
+1.05V_PCH(RT8209A)		
Size	Document Number	Rev
	UMG Dis	3A
Date:	Monday, February 01, 2010	Sheet 48 of 51



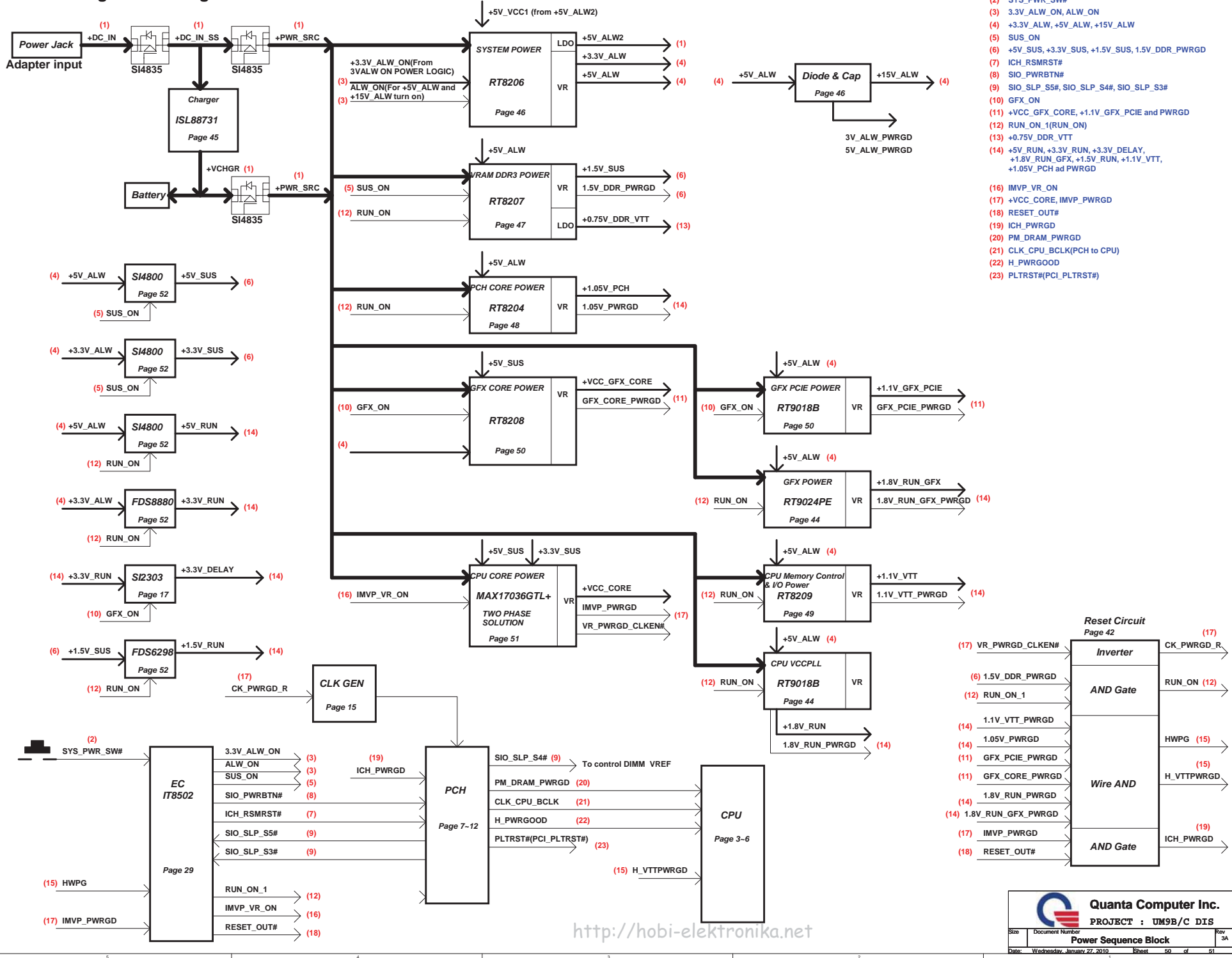
For Park-XT:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V

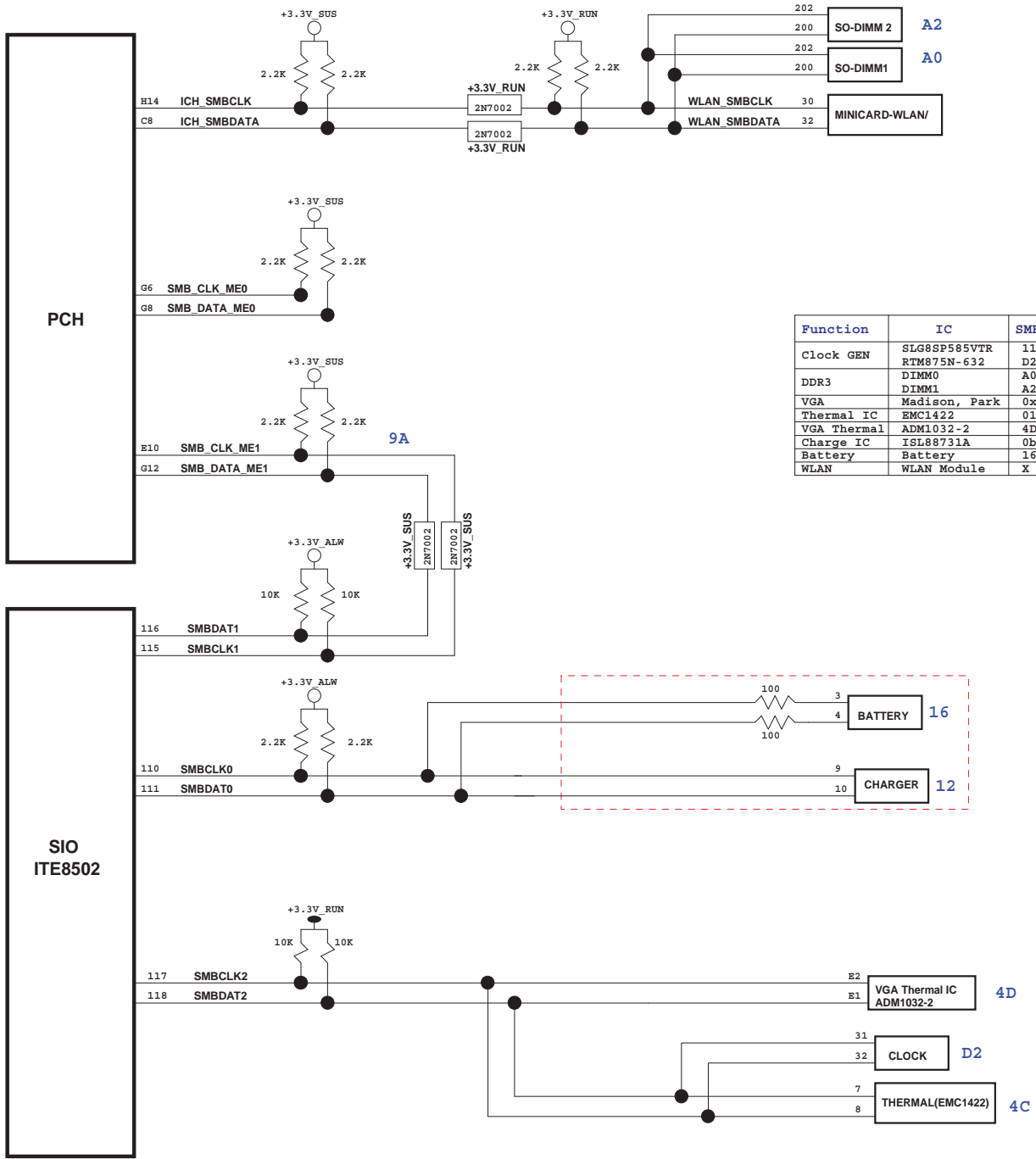


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Power Design Block Diagram 2009/08/24



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Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h) D2h
DDR3	DIMM0 DIMM1	A0 A2
VGA	Madison, Park	0x41
Thermal IC	EMC1422	0100 1100b (4Ch)
VGA Thermal	ADM1032-2	4D
Charge IC	ISL88731A	0b0001001 (0x12)
Battery IC	Battery	16h
WLAN	WLAN Module	X