SIO IT8721F-BX/DX in Ibex Peak platform cause S3 resume fail issue

Issue Topic:

Technical Issue Survey Form

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Document Version History:

Reversion	Change List	Release Date
V.A	Draft	1/08/2009

1. Technical Issue Survey Priority/Schedule

Priority	☐ Urgent	■ High	☐ Low
Target Schedule	2010/1/25		

Note:

A). Urgent: To finish the survey and solution implementation within one or two days.

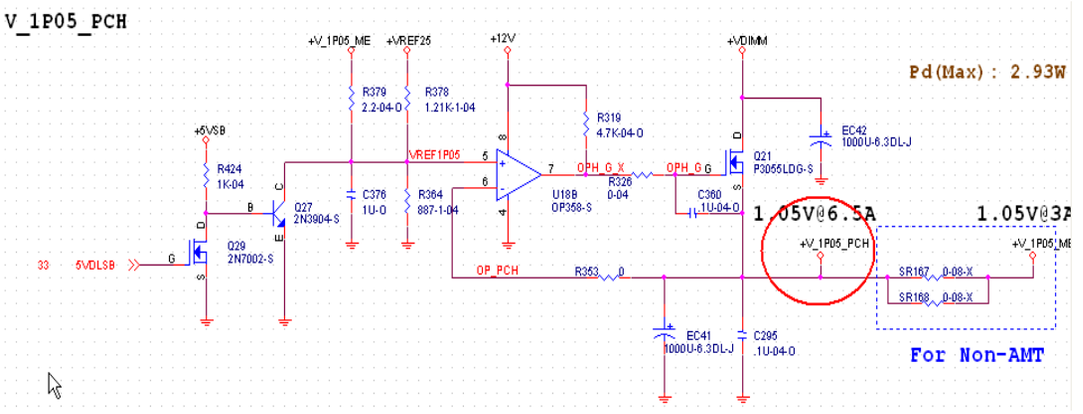
B). High: To finish the survey and solution implementation within one week.

C). Low: To finish the survey within two or three weeks for reference.

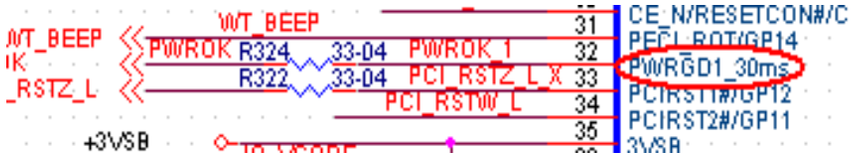
2. Technical Issue Description

- System will power shutdown when resume from S3 state, refer to below measurement of comparison with the perspective signals PCH circuit core 1.05V and SIO PWROK in failure state:

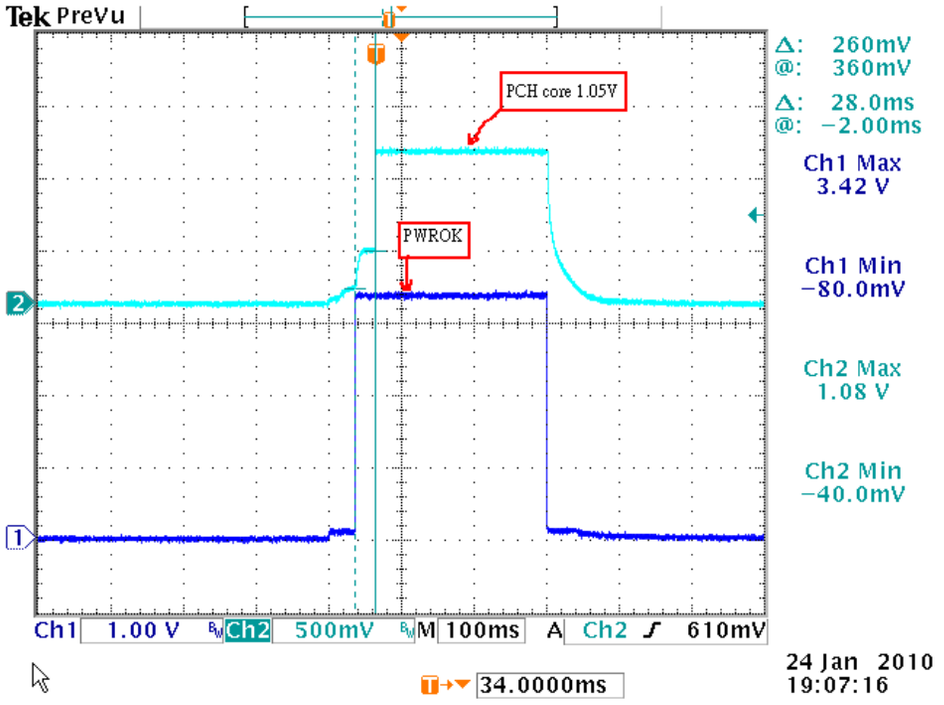
1)PCH core 1.05V circuit:



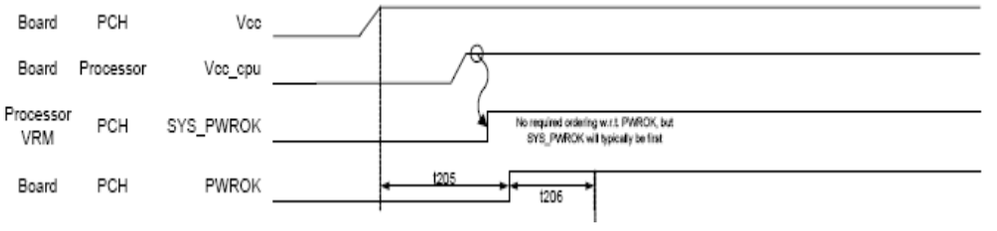
2)SIO PWROK connect to pin 32 PWRGD1_30ms :



3)Below waveform demonstrate fail state of PWROK is ready 28 ms after PCH core 1.05V active:



■ Below timing diagram of IBX EDS demonstrate power sequence from S3 to S0, the relation between PCH core 1.05V and PWROK are described when PCH core 1.05V is ready minima 10ms after PWROK active.

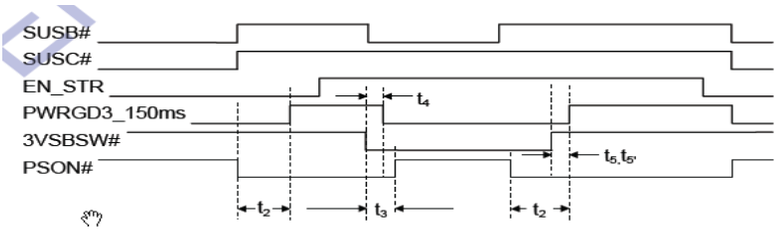


Sym	Parameter	Min	Max	Units	Notes	Fig
t200	VccRTC active to RTCRST# inactive	9	—	ms		8-1
t201	VccSUS active to RSMRST# inactive	10	—	ms	1	8-1
t202	RSMRST# inactive to SUSCLK toggling	97	—	ms	2	8-1
t203	SLP_S5# high to SLP_S4# high	30		us	3	8-2
t204	SLP_S4# high to SLP_S3# high	30		us	4	8-2
t205	VccCORE stable to PWROK active	10	—	ms	5	8-2, 8-3
t206	PWROK deglitch time	1	—	ms	6	8-2, 8-3

- Root cause : Power sequence between PCH core 1.05V and PWROK resume from S3 to S0 are failure.
- Solution : PWROK output signal changed from pin 32 PWRGD1_30ms to pin 78 PWRGD3_150ms to meet the correctly power sequence of PCH core 1.05V stable to PWROK active specification , and configure SIO PWRGD3_150ms time t5 to 135ms from register address 2A , Bit 0=1, refer to below picture:

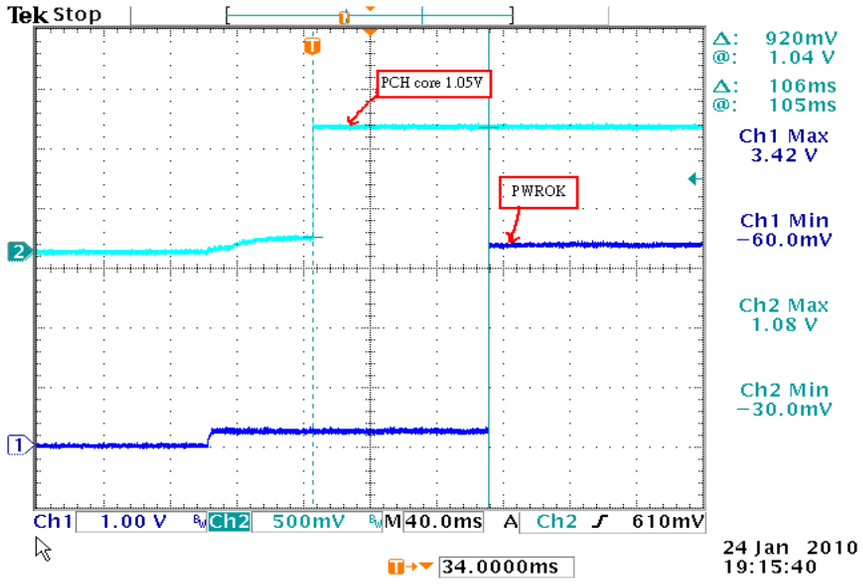
1)SIO connect to pin78 :

2)SIO register set address 2A,Bit 0=1 :



t_5	Delay time of 3VSBSW# rising edge to PWRGD3_150ms rising edge	1 Note:2A<Bit 0>=0 (Default)	usec
$t_{5'}$		135 Note:2A<Bit 0>=1	msec

3)Correctly waveform with implementation of solution , PCH core 1.05V stable 106 ms to PWROK active :



■ If your design is similar was described above , please fill the survey form :

1-PWROK connect to PWRGD3_150ms pin 78 of SIO IT8721F-BX/DX.

2-SIO IT8721F-BX/DX pin PWRGD3_150ms delay 135 ms configure register address 2A , Bit 0=1.

3-Make sure your power sequence resume S3 to S0 of PCH core 1.05V and PWROK are correctly.

3. Technical Issue Response/Confirmation by Project Team

Project Team/Owner	Project Name List	Checking Result
RD1		
H/W 1: Eric		**OK**
		NG
H/W 2: Fish	H55H-LAIO : SIO IT8721F-BX BOM changed.	**OK**
		NG
H/W 3: Mutai		**OK**
		NG
CRD: Yonghua		**OK**
		NG
RD2		
H/W 1: Jacy		**OK**
		NG
H/W 2: Jeff		**OK**
		NG
H/W 3: Rios		**OK**
		NG

CRD: Huadong		**OK**
		NG

Note: **a). The model name should include extended model which has different BOM/CKD, but same PCB version**

4. Implementation Plan/Action for NG project

4.1 Project List for solution implementation

Project Team/Owner	Project Name List (NG → OK)	Solution / Status
RD-1_H/W 1: Eric		
RD1_H/W 2: Fish		
RD1_H/W 3: Mutai		
RD1_CRD: Yonghua		
RD2_H/W1: Jacy		
RD2_H/W2: Jeff		
RD2_H/W3: Rios		
RD2_CRD: Huadong		

4.2 Solution Description/Implementation

- ECN/DCN:
  - After approval finishing and PM/customer agreement release.
- Design Checklist:
  - Yes
- Schematic modify:
  - Yes