Compal Confidential

HCW50 Schematics Document

AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

2006 / 02 / 28 Rev:0.3 (For PVT)

Security Classification	Compal Secret Data		
Issued Date	2005/05/09	Deciphered Date	2006/03/08

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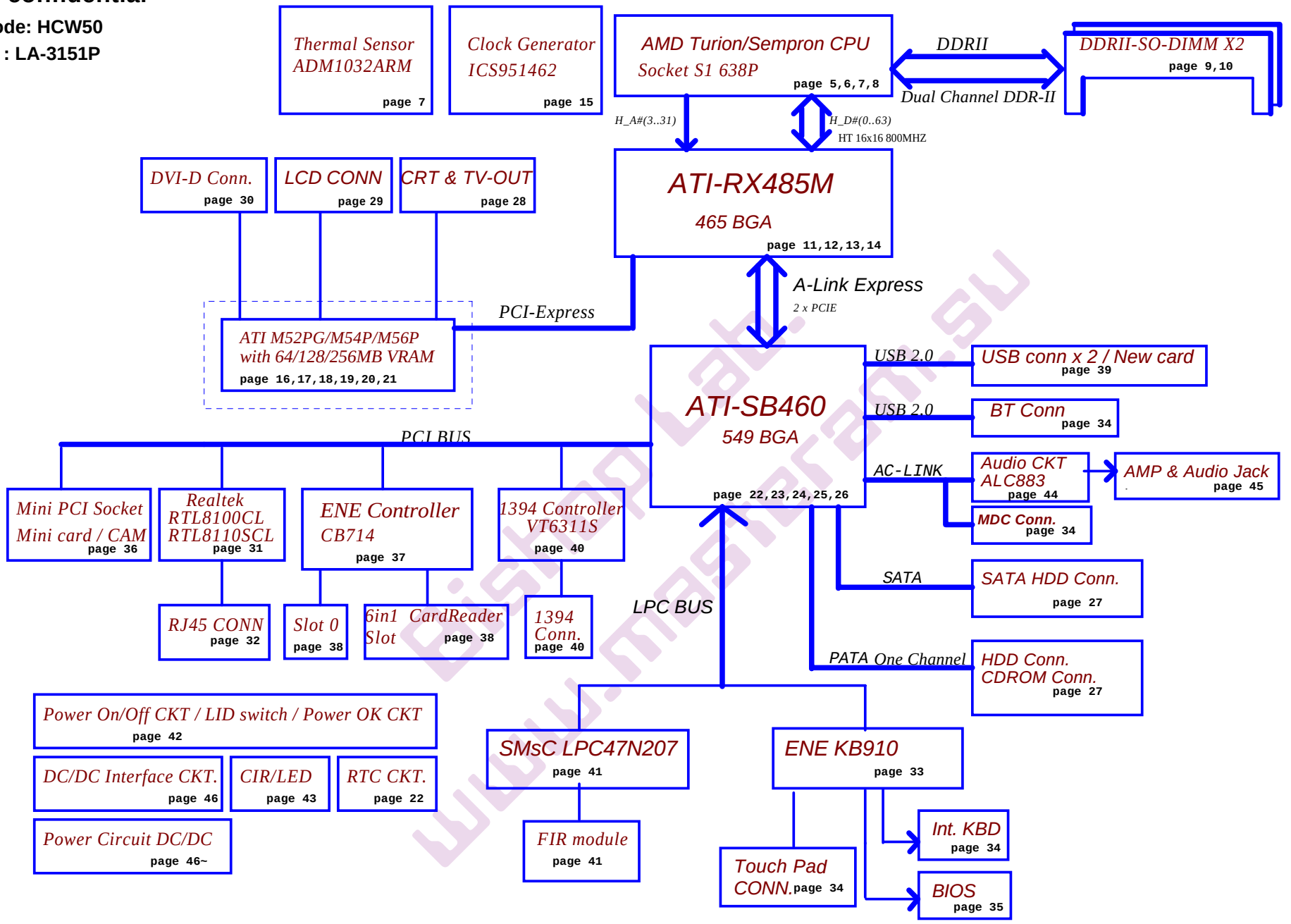
Project Code: HCW50

File Name : LA-3151P



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0~1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

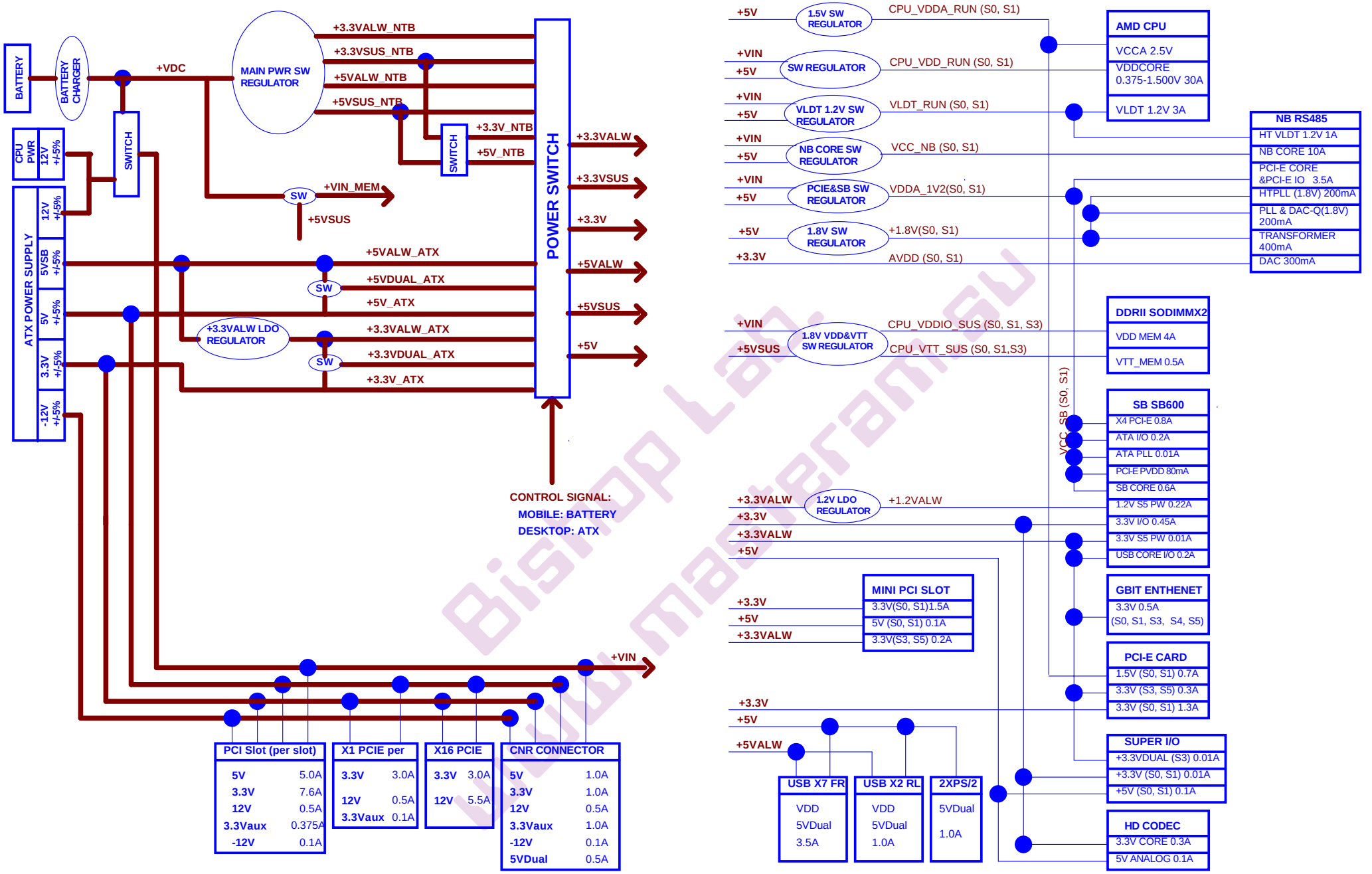
Device	Address
Fintek F75383M	1001 100X b

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	



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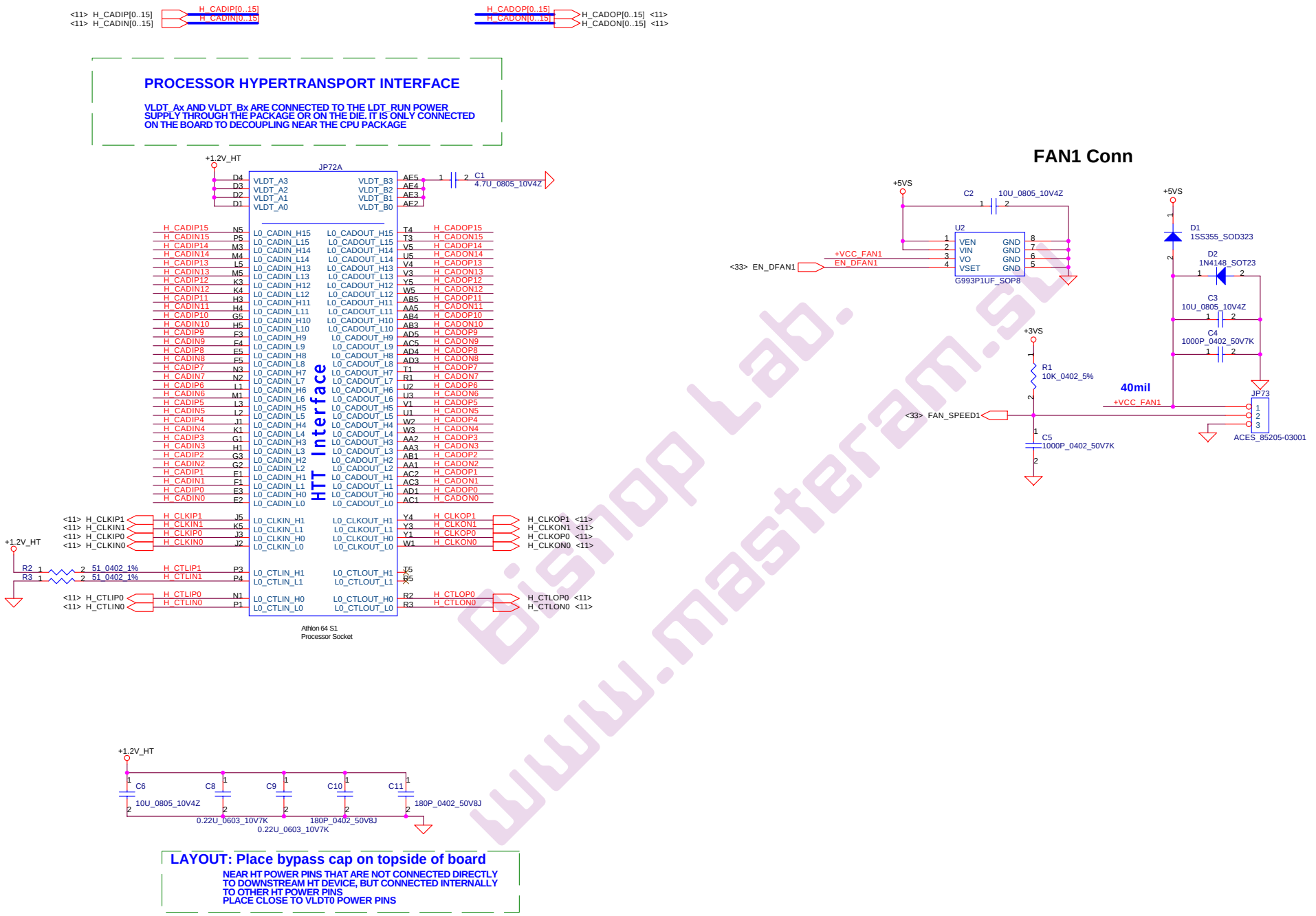

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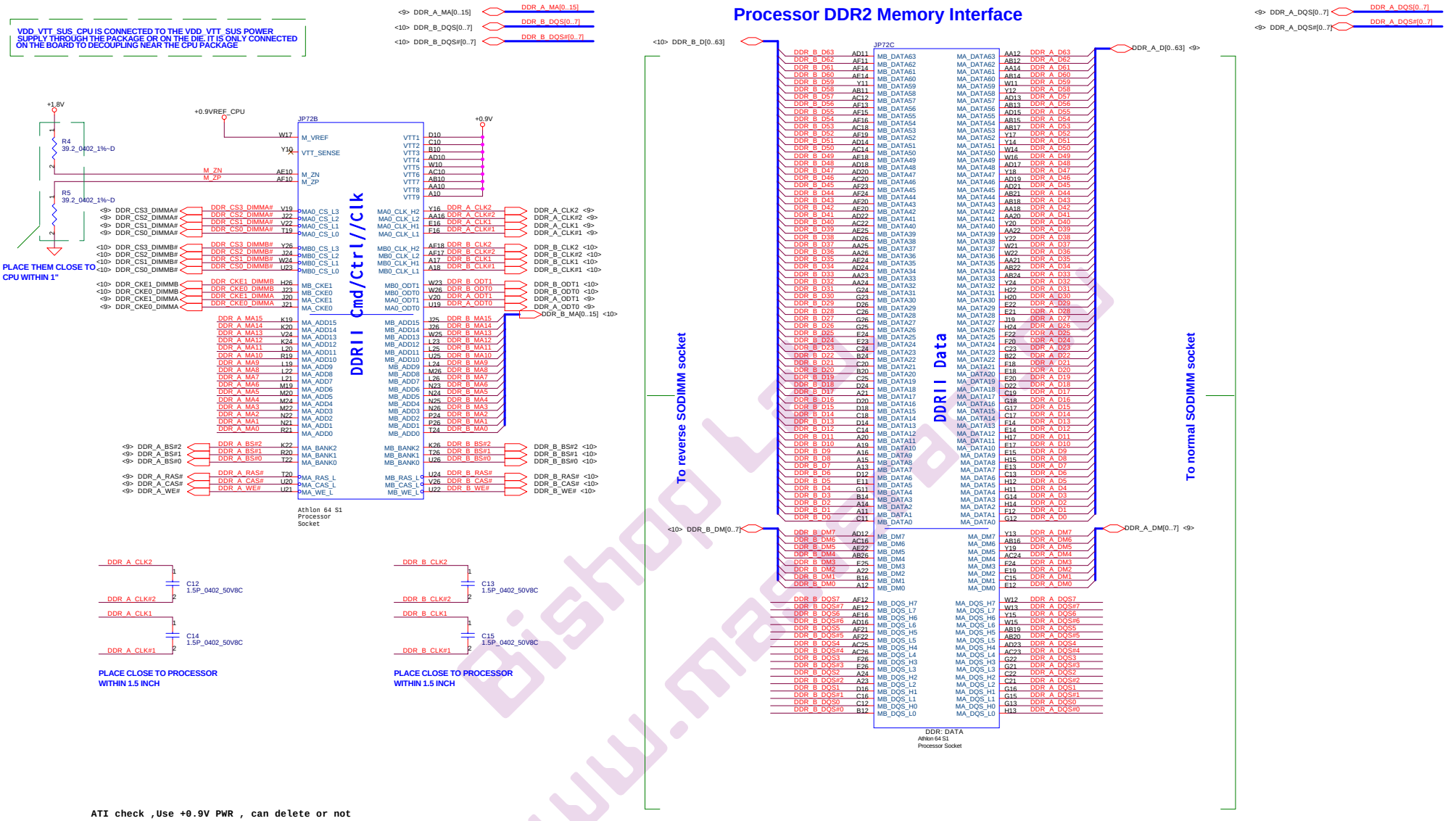
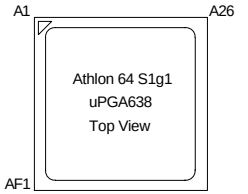
Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





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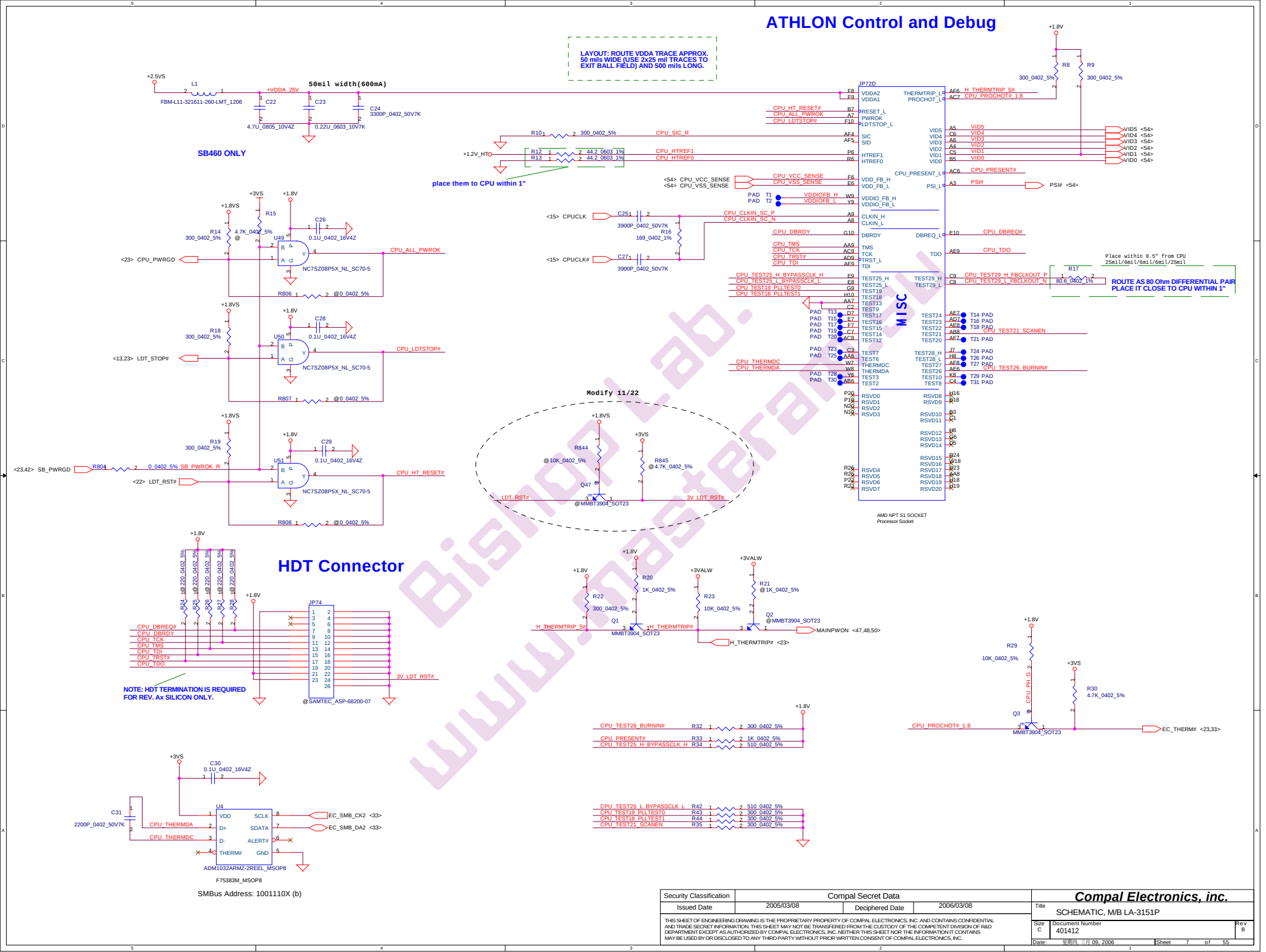
ATHLON Control and Debug



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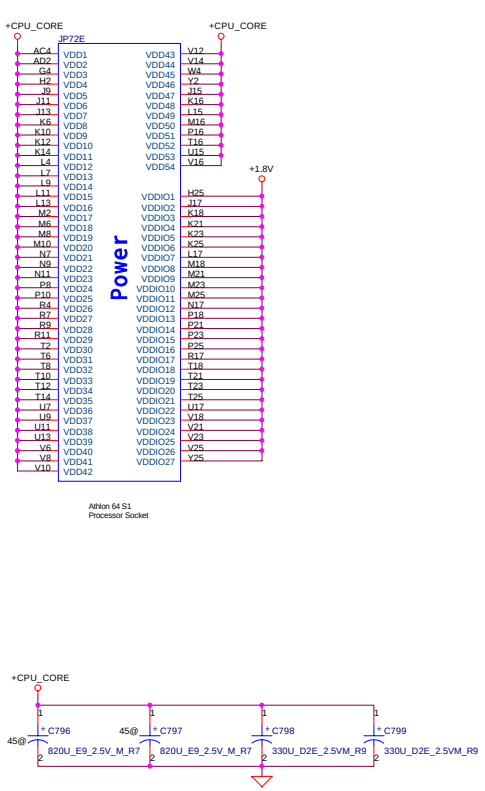
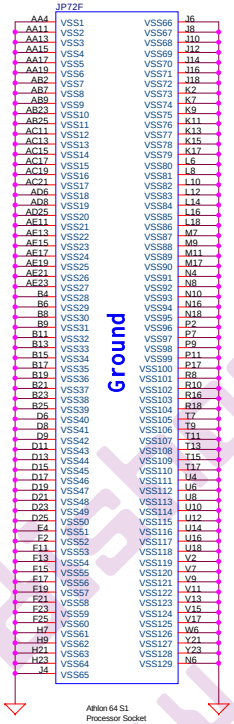
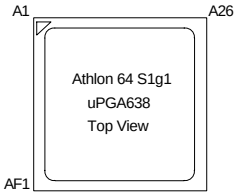
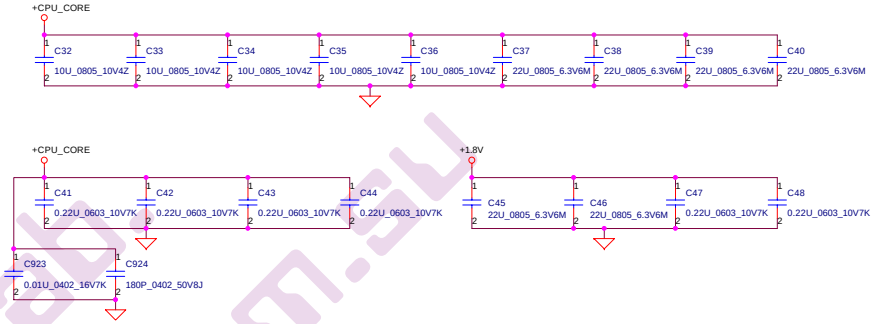


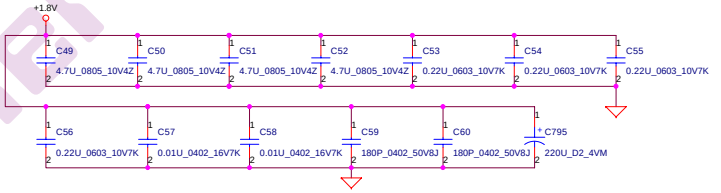




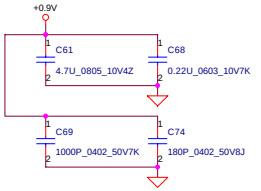
BOTTOMSIDE DECOUPLING



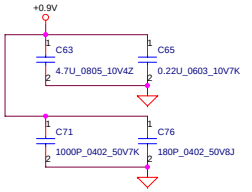
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



CPU left-hand side



CPU right-hand side



PROCESSOR POWER AND GROUND

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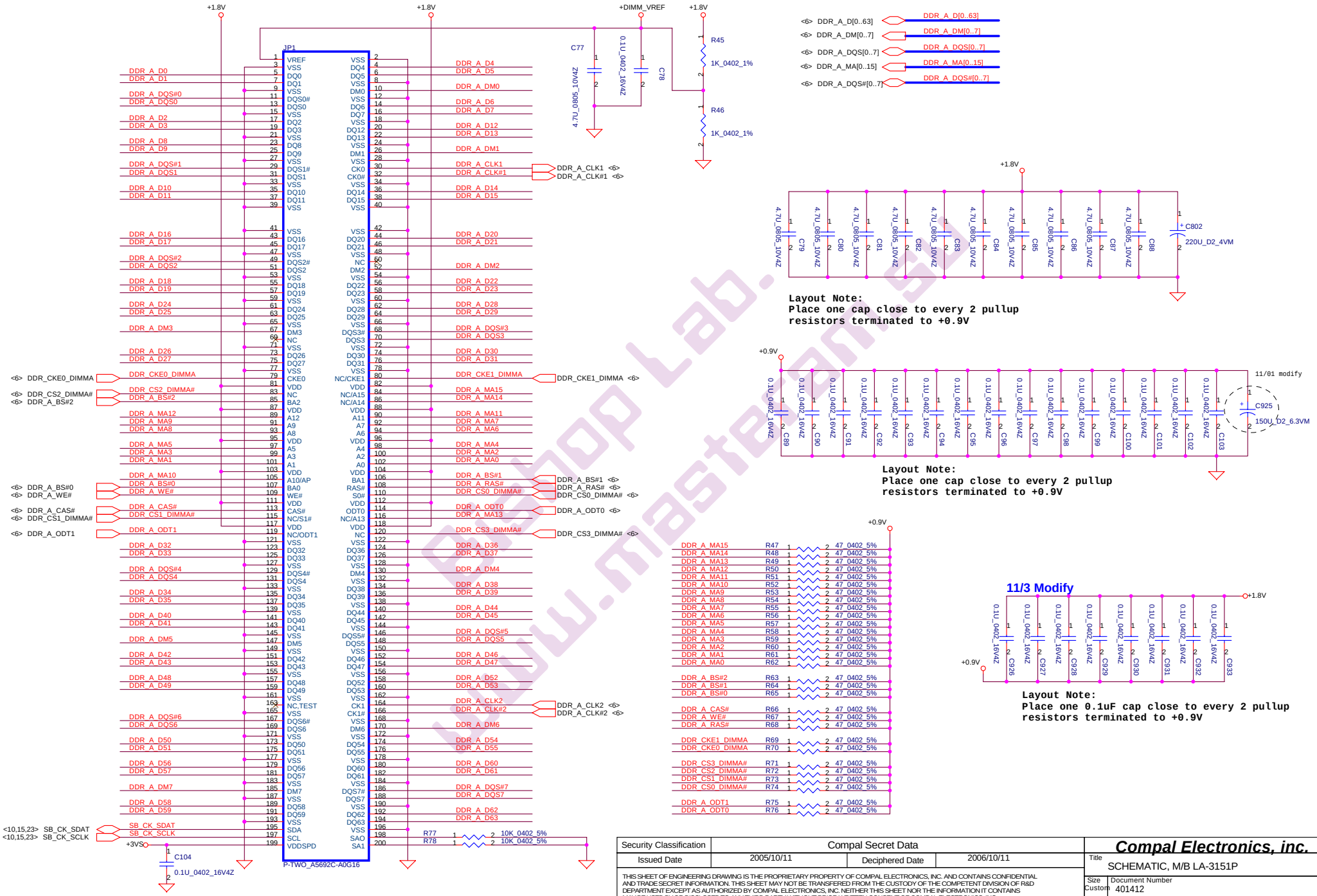

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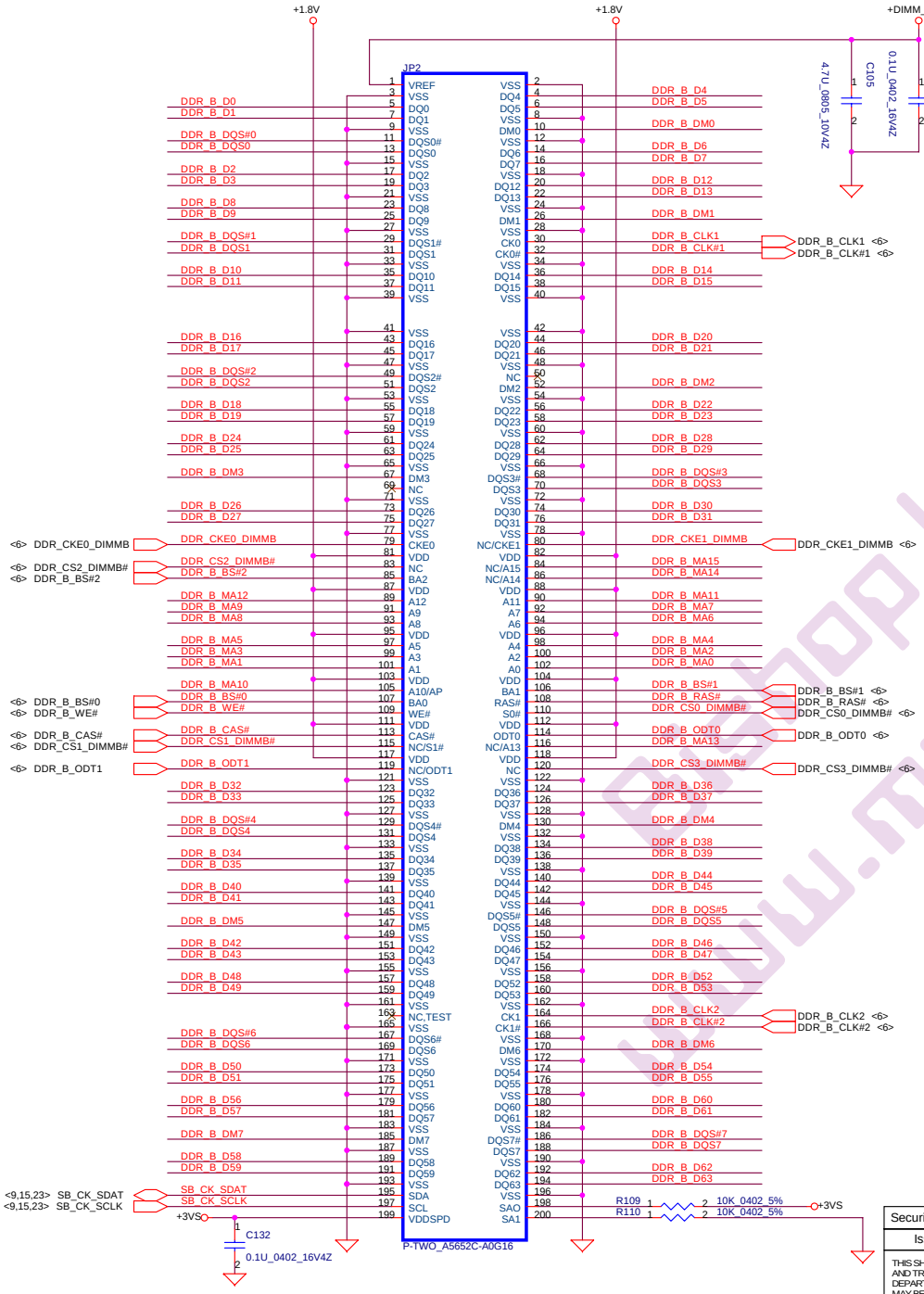
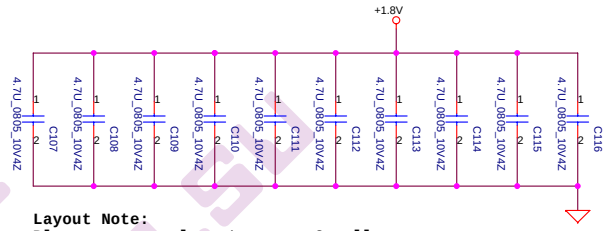
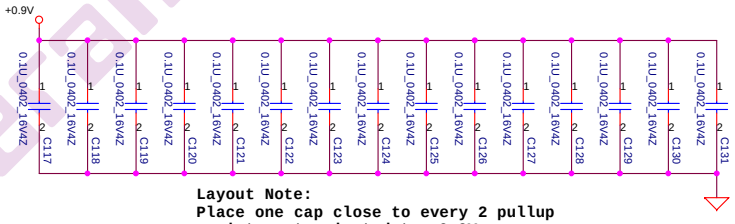
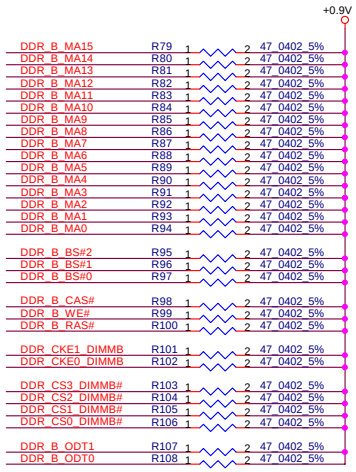




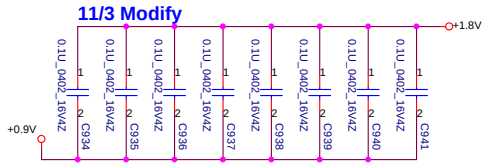
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



11/3 Modify



Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

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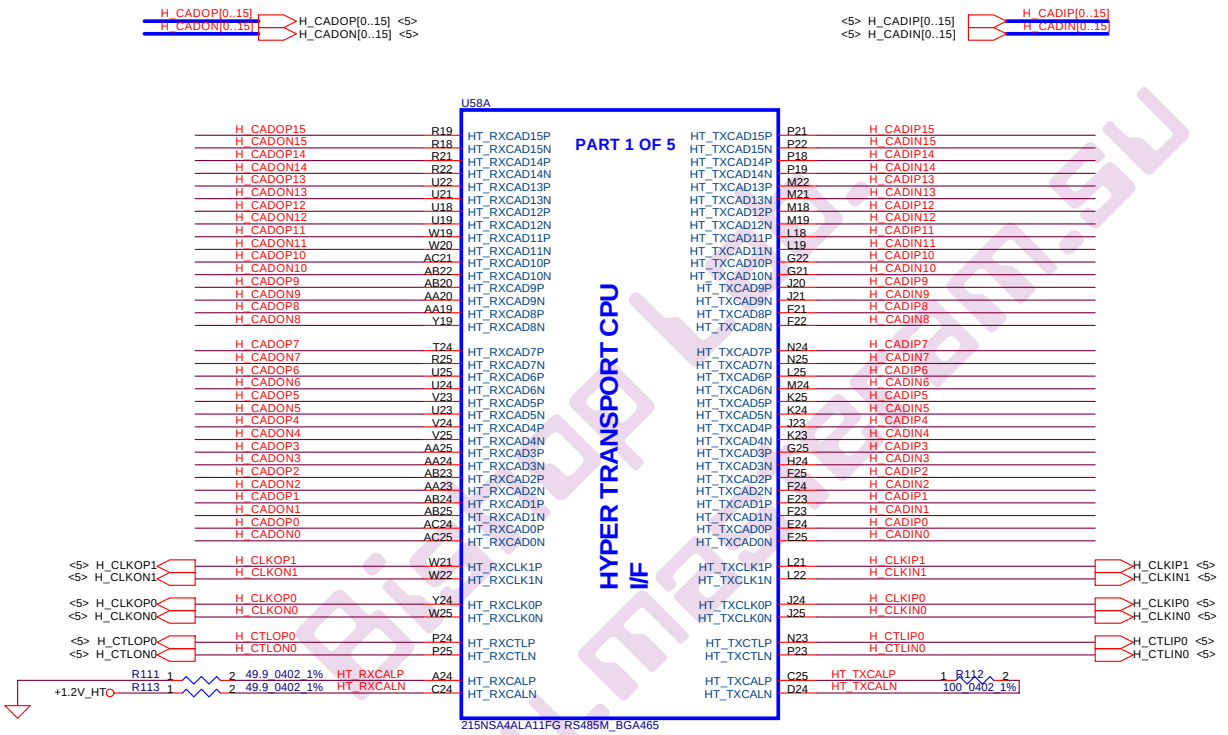

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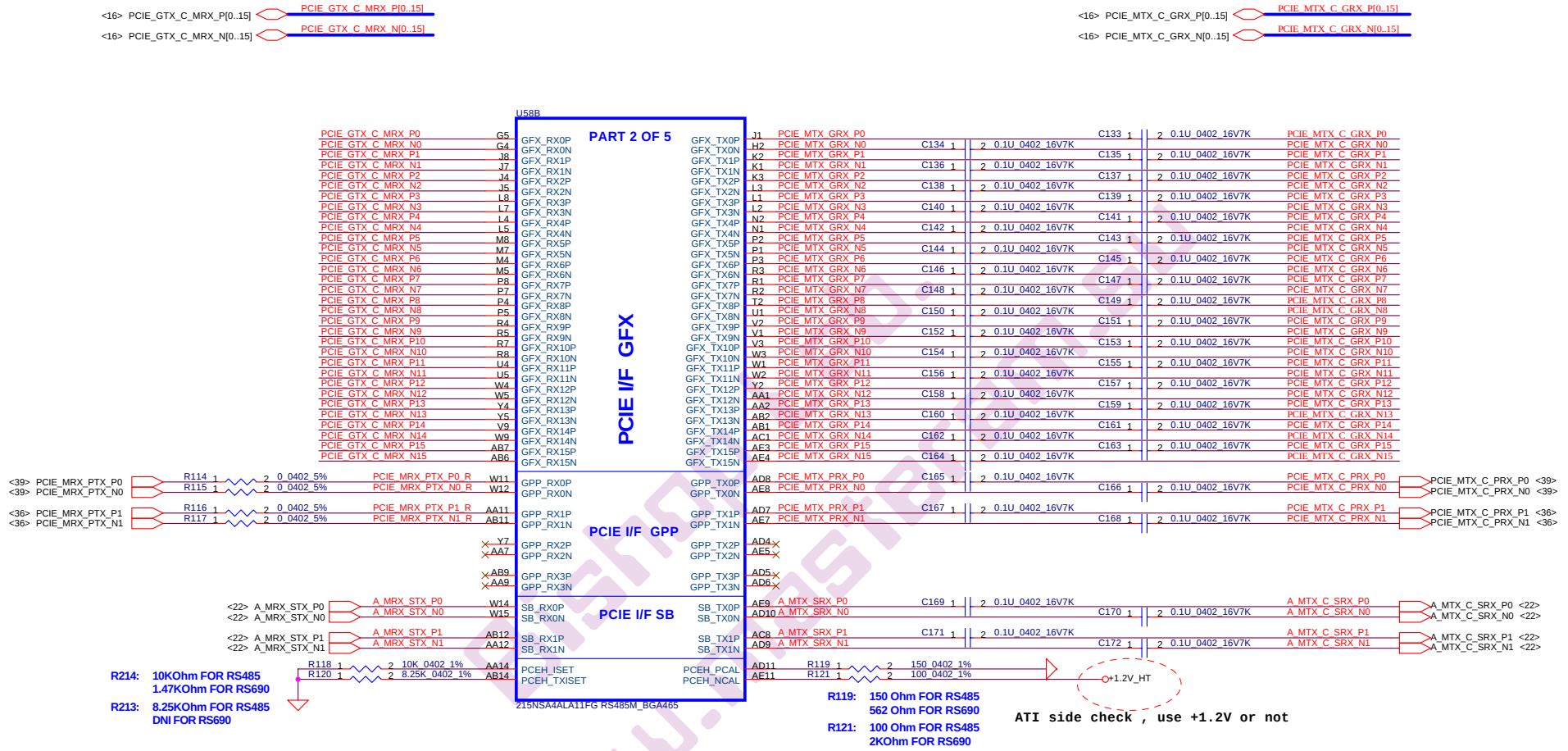

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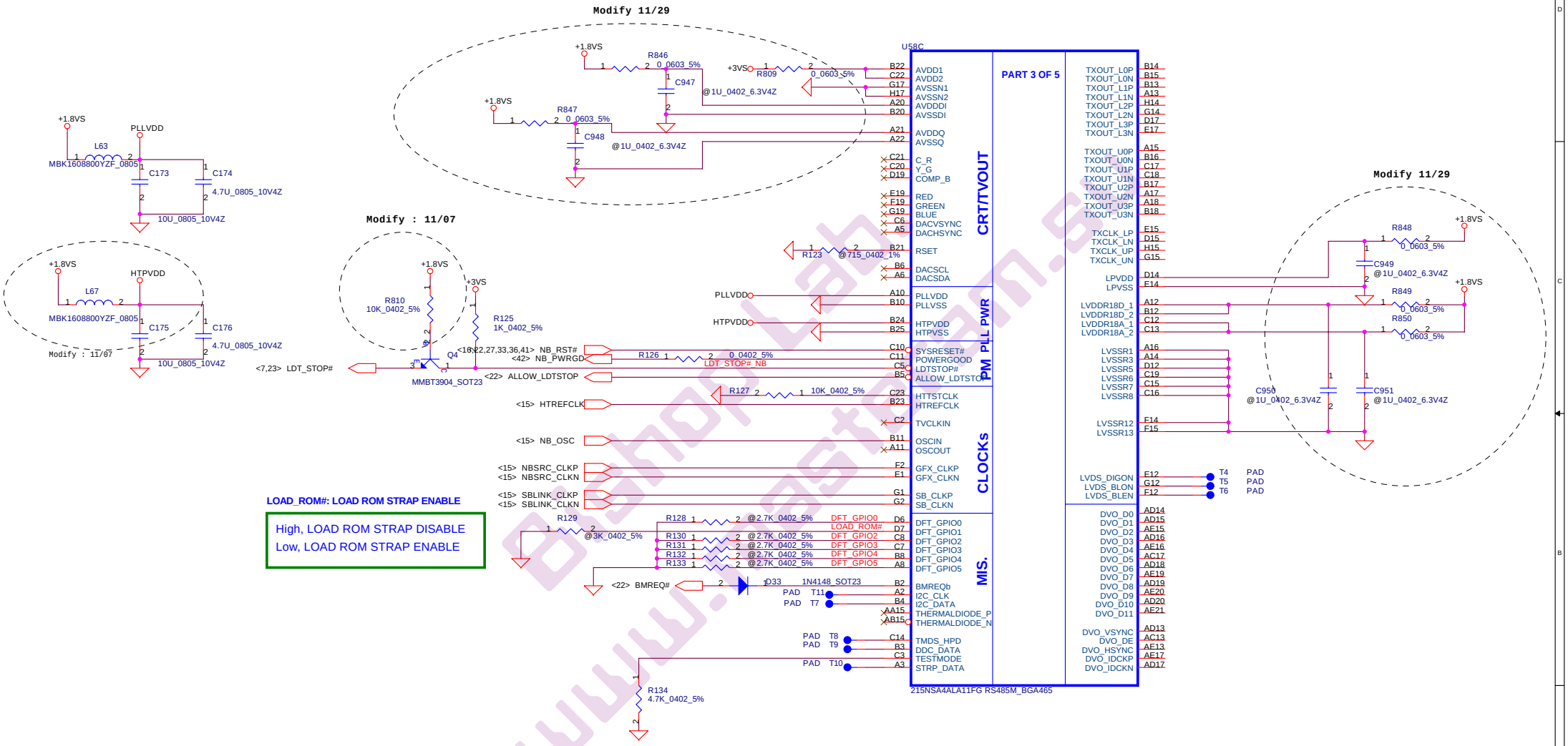
ATI check , CRT / TV/ LVDS can delete or not when I use RX485



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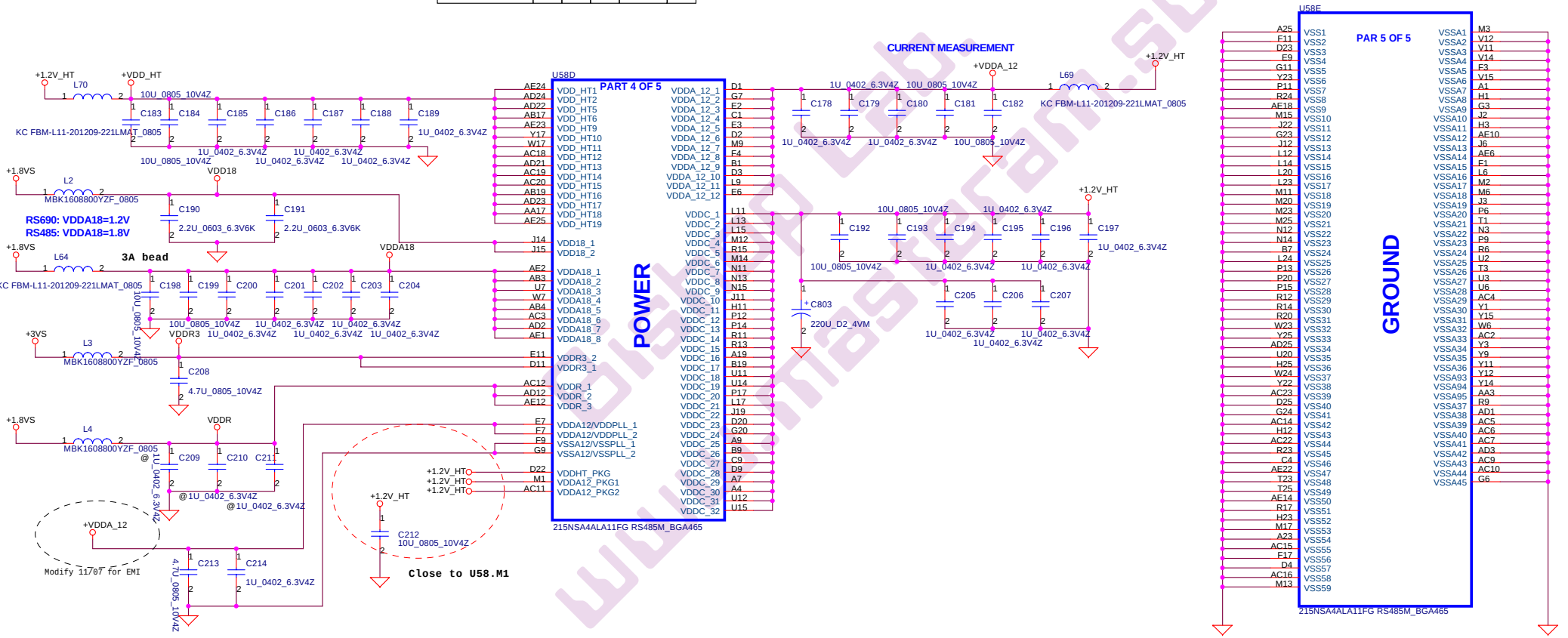
NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



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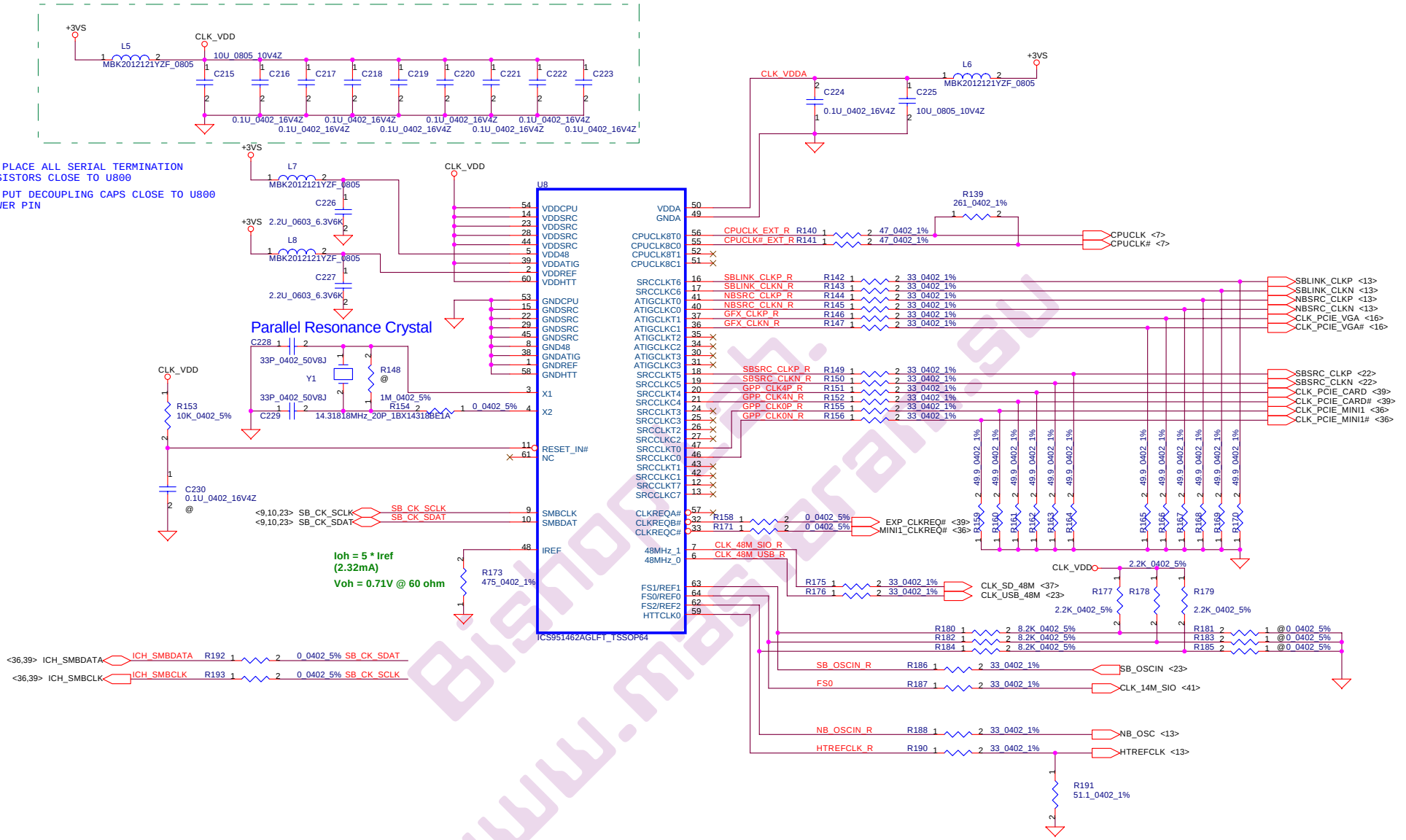

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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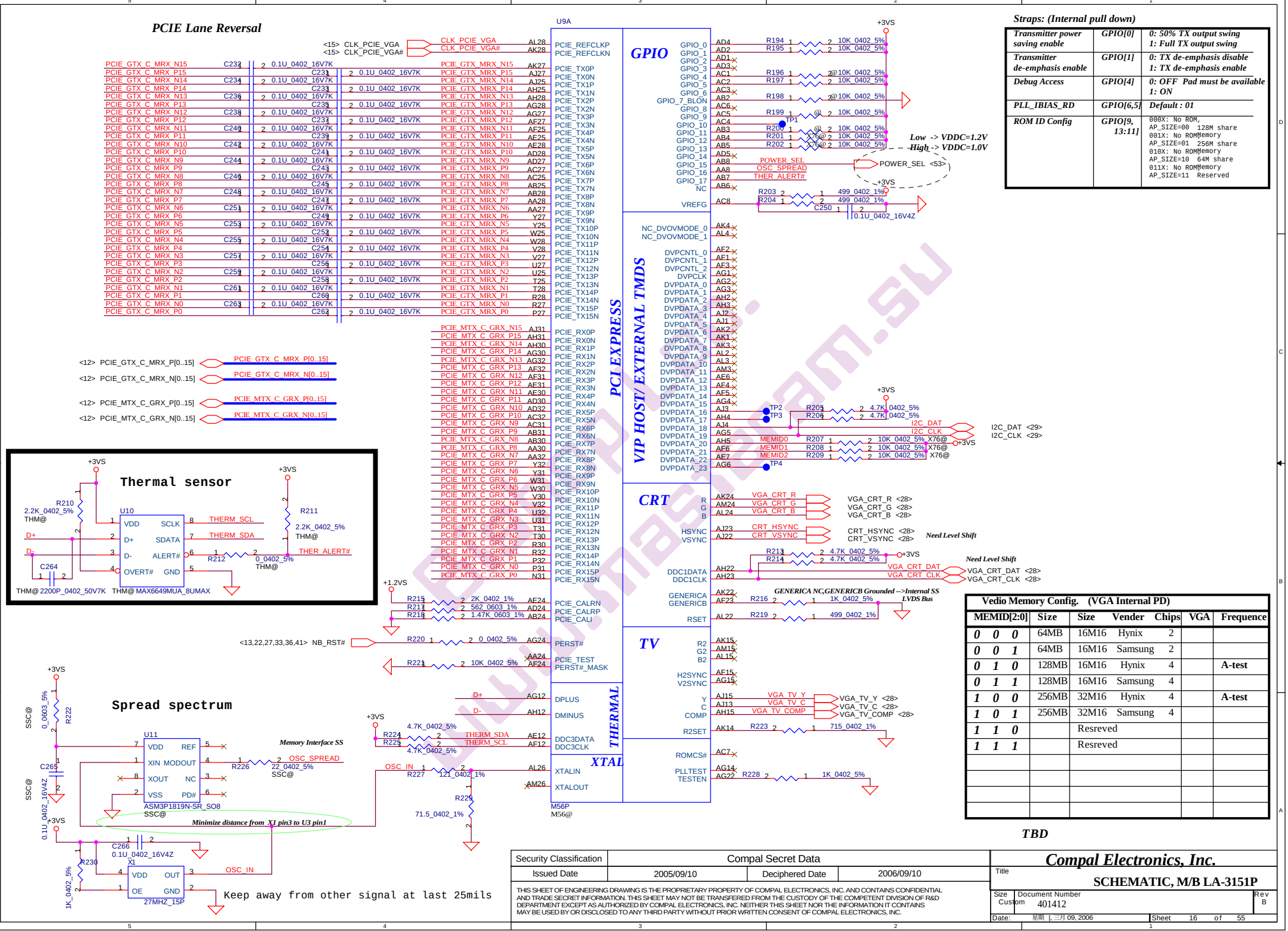
PCIE Lane Reversal
U9A
GPIO
PCI EXPRESS
VIP HOST/ EXTERNAL TMDS
CRT
TV
THERMAL
XTAL
M56P
M56@
Straps: (Internal pull down)
Transmitter power saving enable | GPIO[0] | 0: 50% TX output swing 1: Full TX output swing
Transmitter de-emphasis enable | GPIO[1] | 0: TX de-emphasis disable 1: TX de-emphasis enable
Debug Access | GPIO[4] | 0: OFF Pad must be available 1: ON
PLL_IBIAS_RD | GPIO[6,5] | Default : 01
ROM ID Config | GPIO[9, 13:11] | 000X: No ROM, AP_SIZE=00 128M share 001X: No ROMMemory AP_SIZE=01 256M share 010X: No ROMMemory AP_SIZE=10 64M share 011X: No ROMMemory AP_SIZE=11 Reserved
Low -> VDDC=1.2V
High -> VDDC=1.0V
Thermal sensor
U10
ASM3P1819N-SR_SO8
Spread spectrum
U11
Memory Interface SS
Minimize distance from X1 pin3 to U3 pin1
Keep away from other signal at last 25mils
Need Level Shift
GENERICA NC,GENERICB Grounded -->Internal SS LVDS Bus
Vedio Memory Config. (VGA Internal PD)
MEMID[2:0] | Size | Size | Vender | Chips | VGA | Frequence
0 0 0 | 64MB | 16M16 | Hynix | 2
0 0 1 | 64MB | 16M16 | Samsung | 2
0 1 0 | 128MB | 16M16 | Hynix | 4 | A-test
0 1 1 | 128MB | 16M16 | Samsung | 4
1 0 0 | 256MB | 32M16 | Hynix | 4 | A-test
1 0 1 | 256MB | 32M16 | Samsung | 4
1 1 0 | Resreved
1 1 1 | Resreved
TBD
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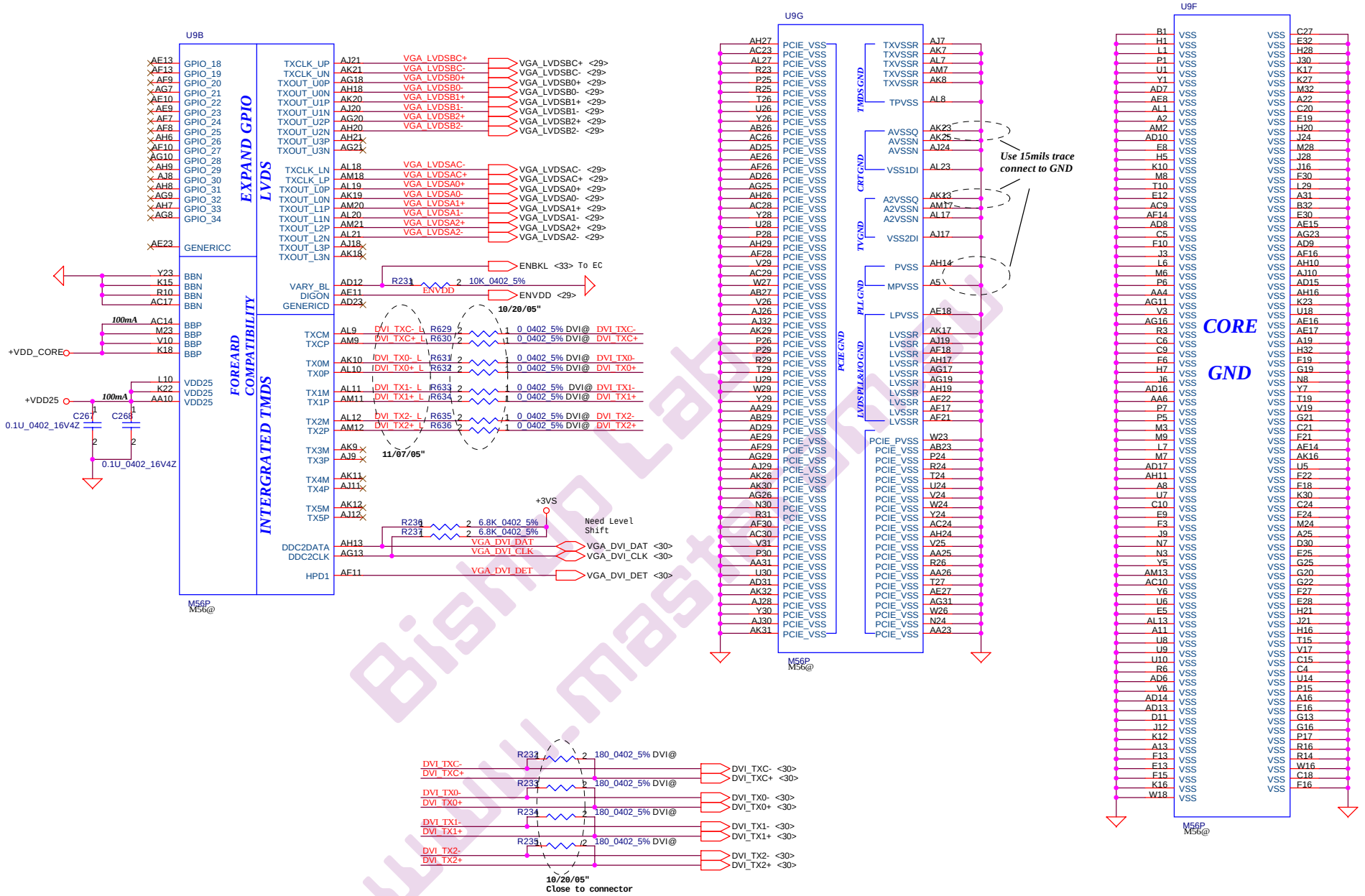

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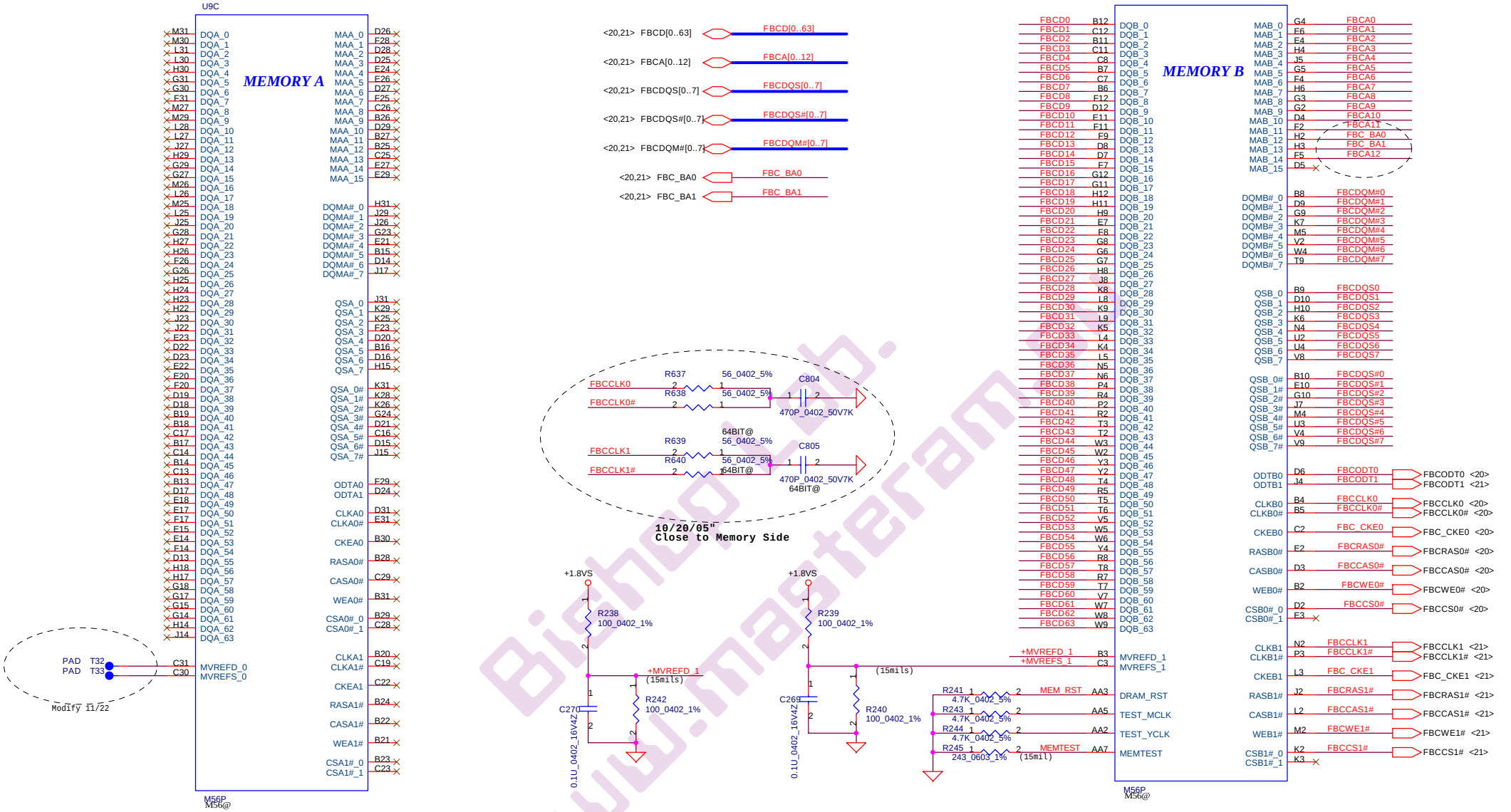

GDDR2

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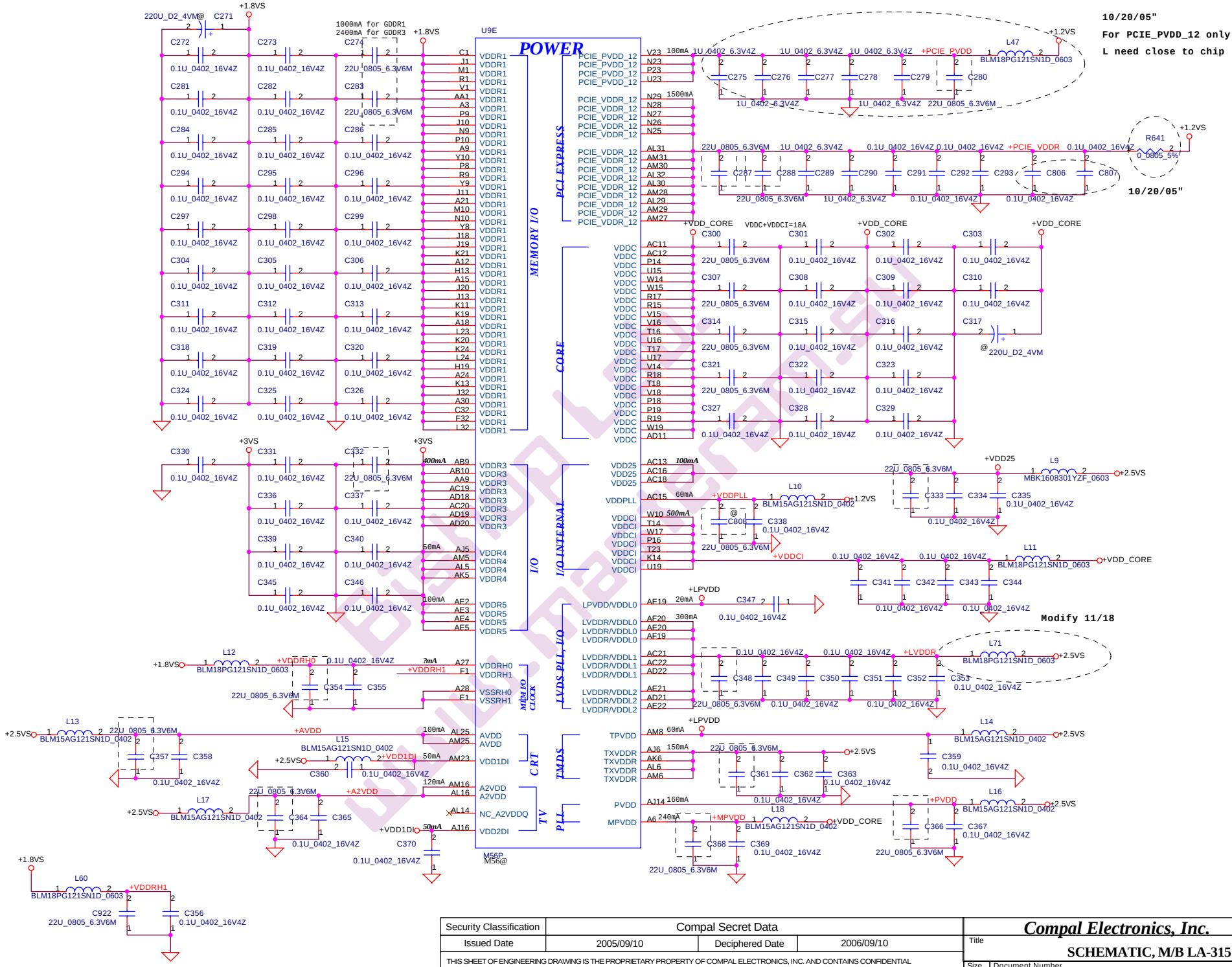

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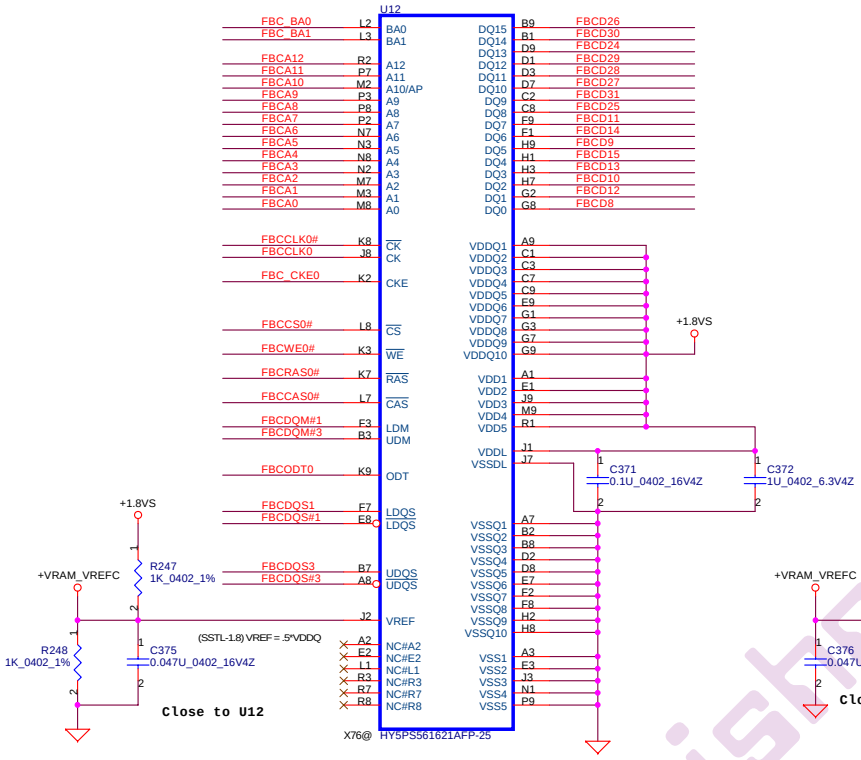
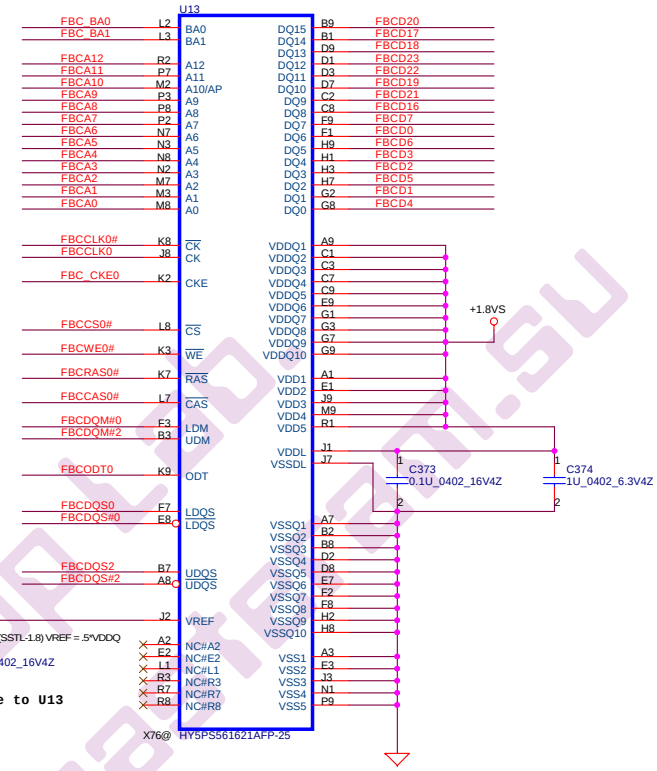
11/03/05' SWAP NET
11/04/05' SWAP NET
11/08/05' SWAP NET

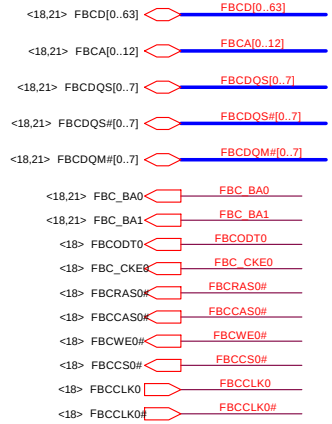


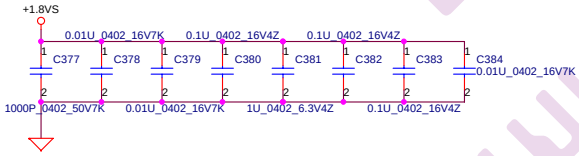
DDR2 BGA MEMORY

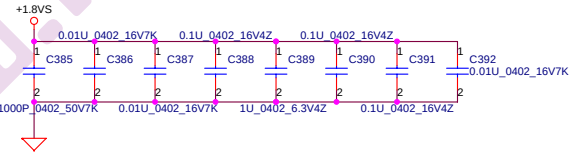
11/03/05' SWAP NET

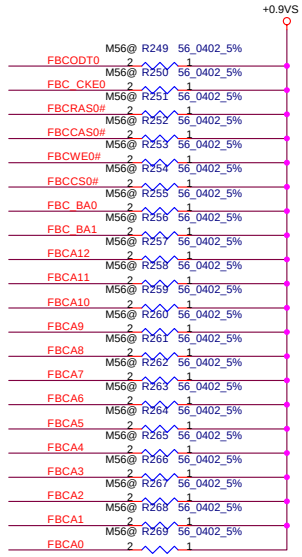


DDR2 BGA MEMORY









M56 Only

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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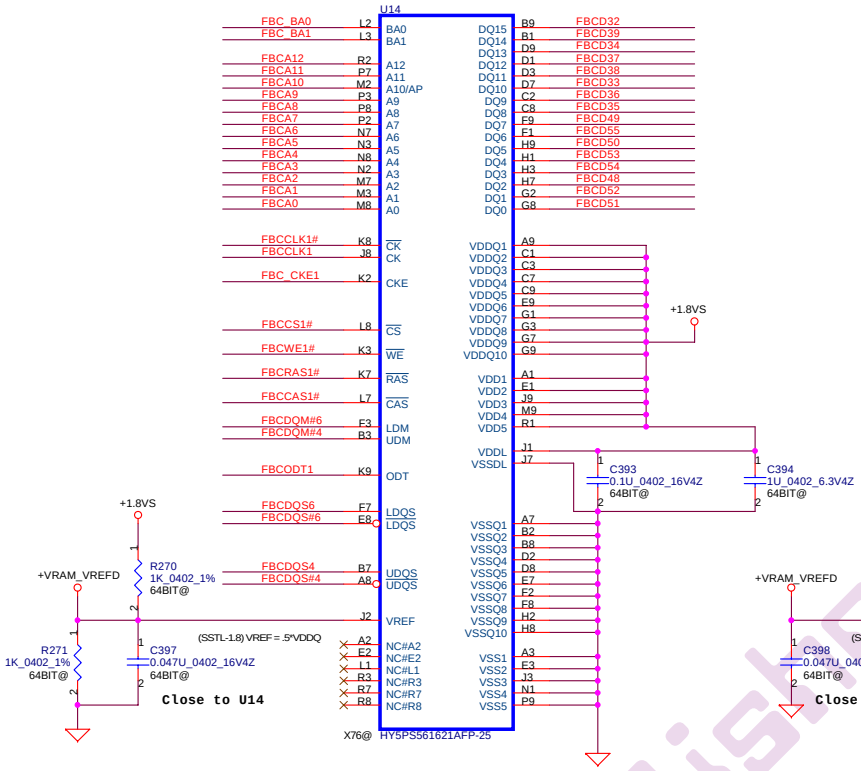
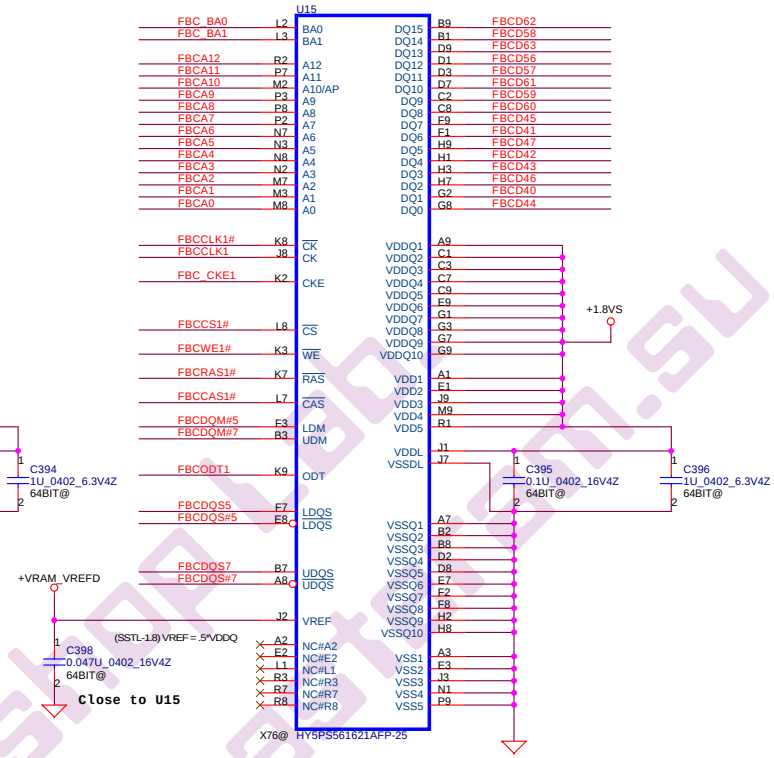
11/03/05' SWAP NET

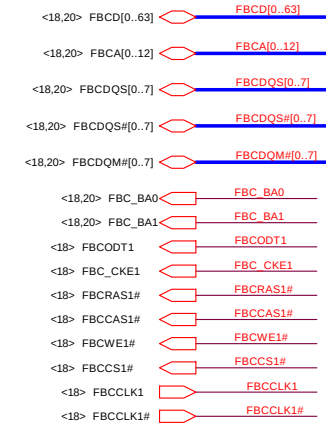


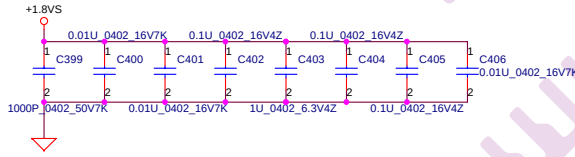
DDR2 BGA MEMORY

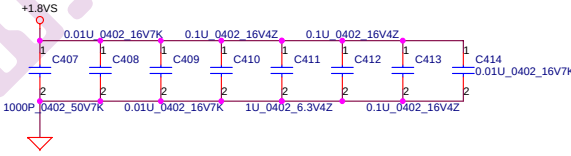
11/03/05' SWAP NET

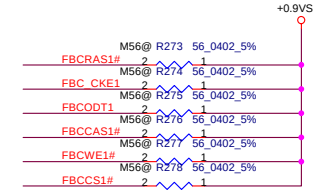


DDR2 BGA MEMORY









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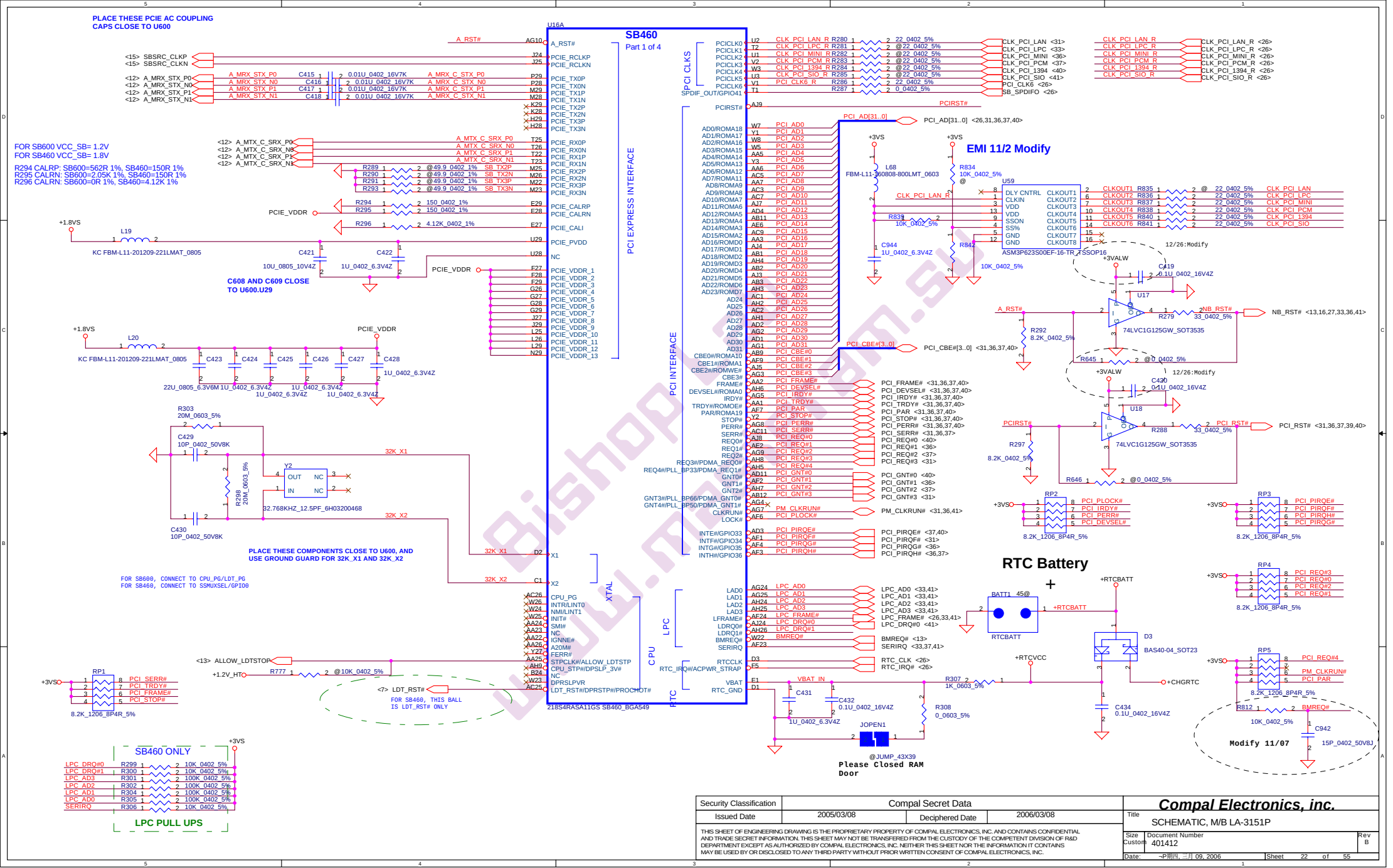

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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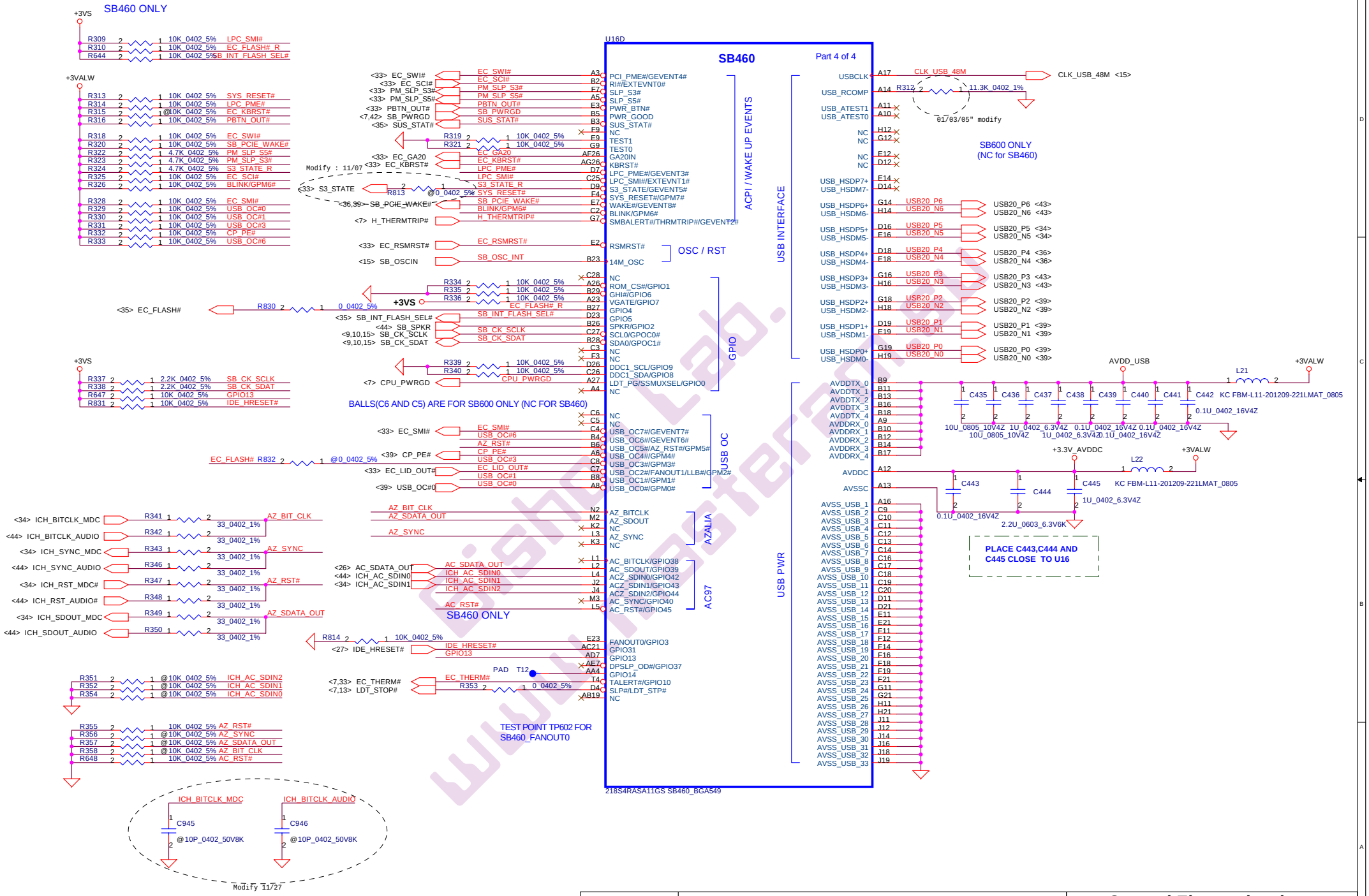

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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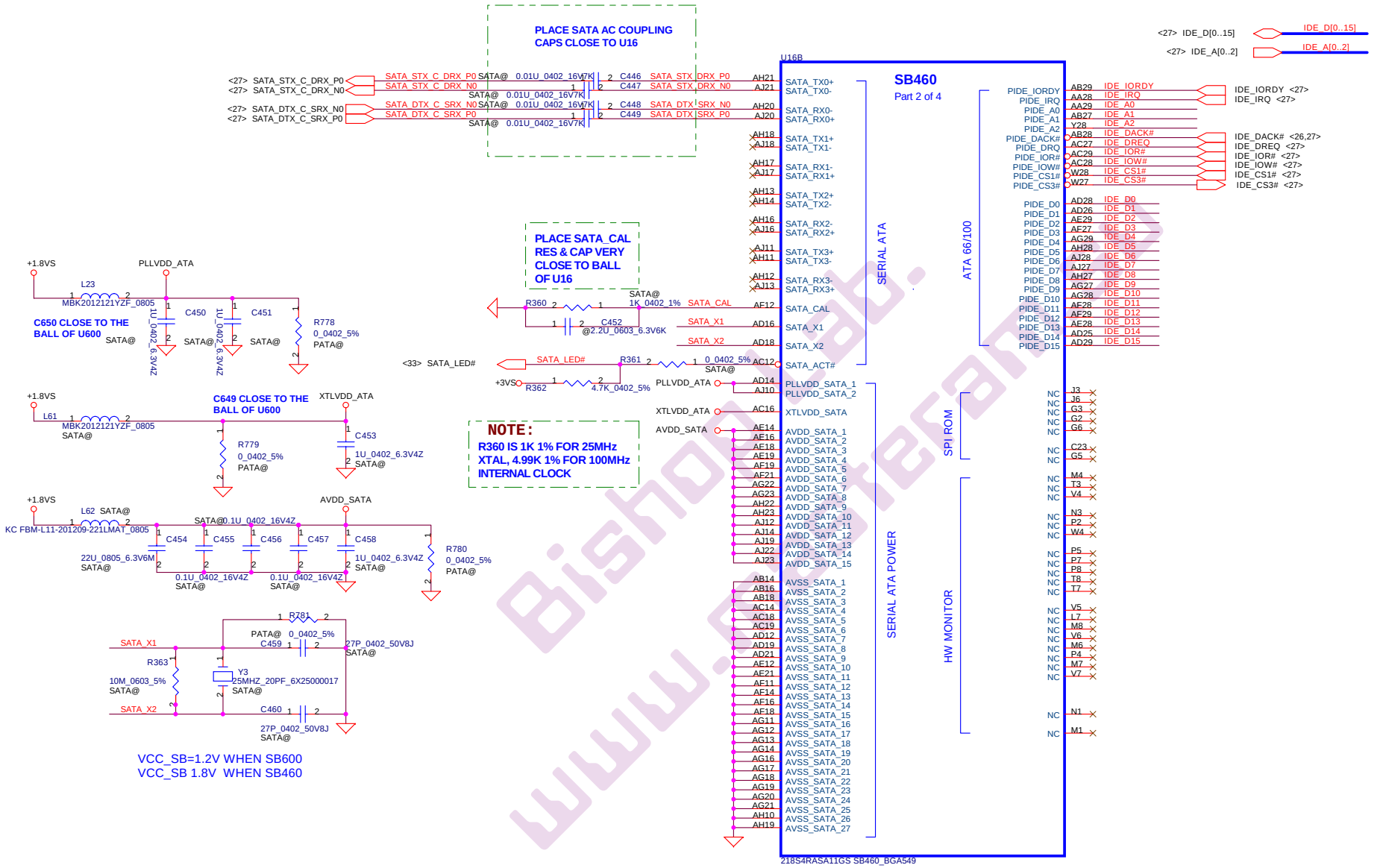

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Issued Date	2005/03/08	Deciphered Date	2006/03/08

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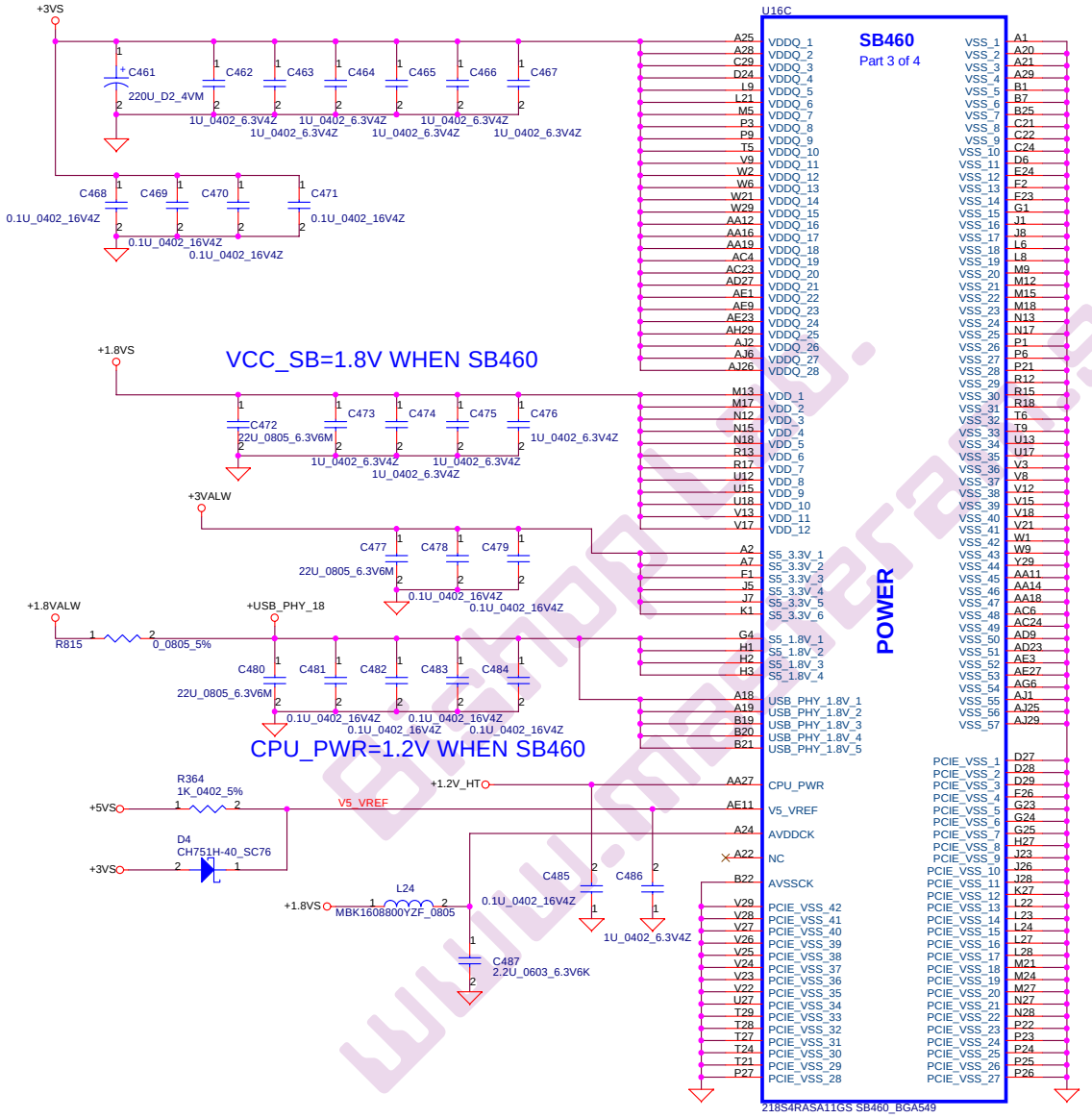

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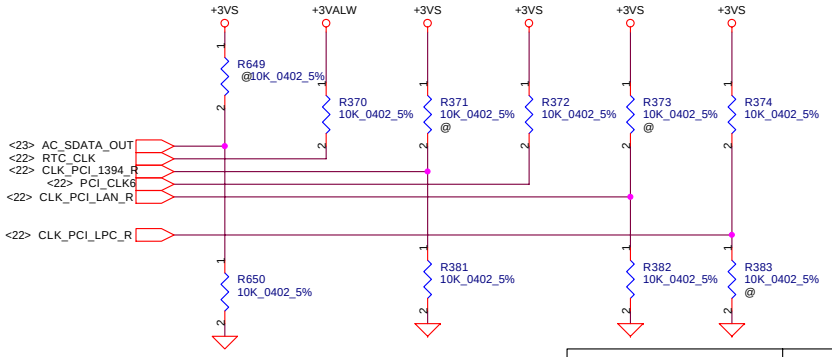
REQUIRED STRAPS

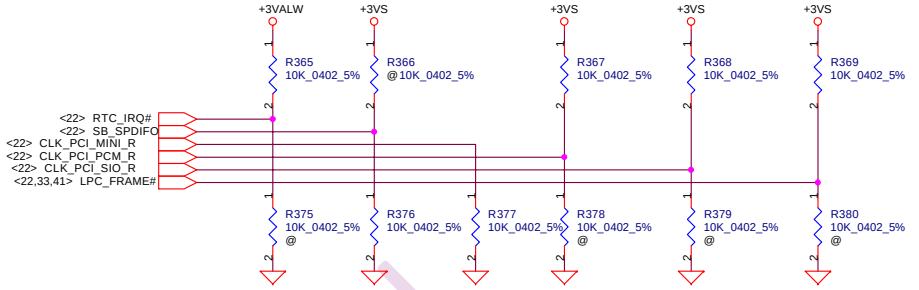
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	SB600 PCI_CLK0 CLK_PCI_LAN	SB600 PCI_CLK1 CLK_PCI_LPC	SB460 PCI_CLK0 CLK_PCI_LAN	SB460 PCI_CLK1 CLK_PCI_LPC
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM		ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM DEFAULT L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4				

NOTE: R365 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB460 TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY

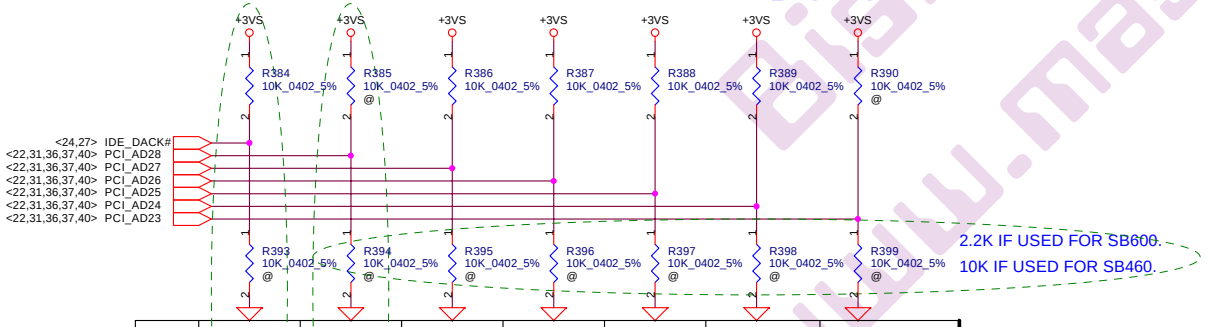


	ACPWRON RTC_IRQ#	SPDIF_OUT SB_SPDIFO	PCI_CLK2 CLK_PCI_MINI	PCI_CLK3 CLK_PCI_PCM	PCI_CLK5 CLK_PCI_SIO	LFRAME# LPC_FRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY — SB600 ONLY

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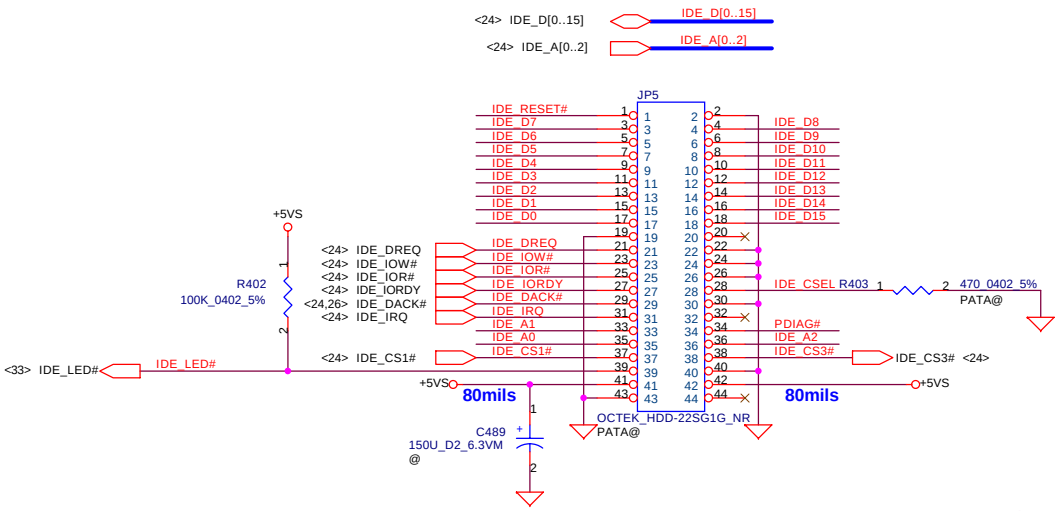
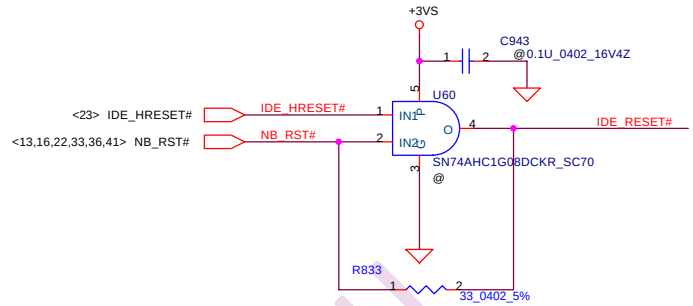
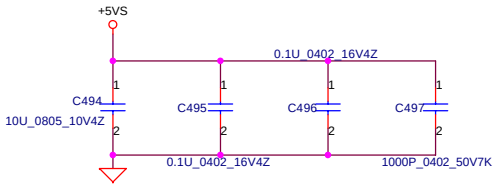
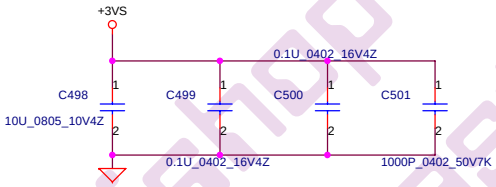
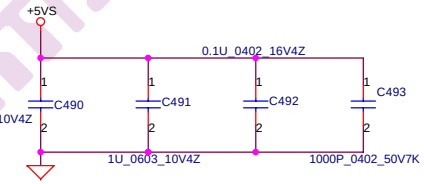
HDD CONN



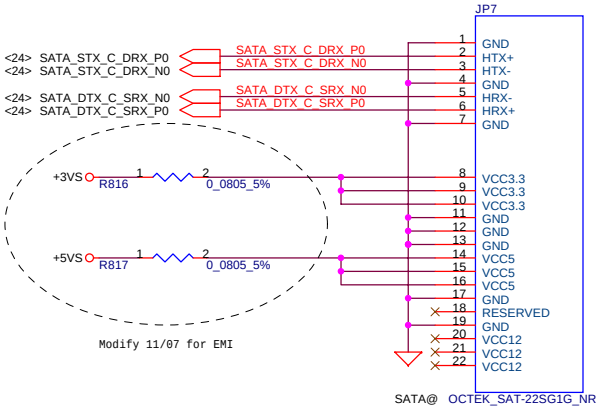






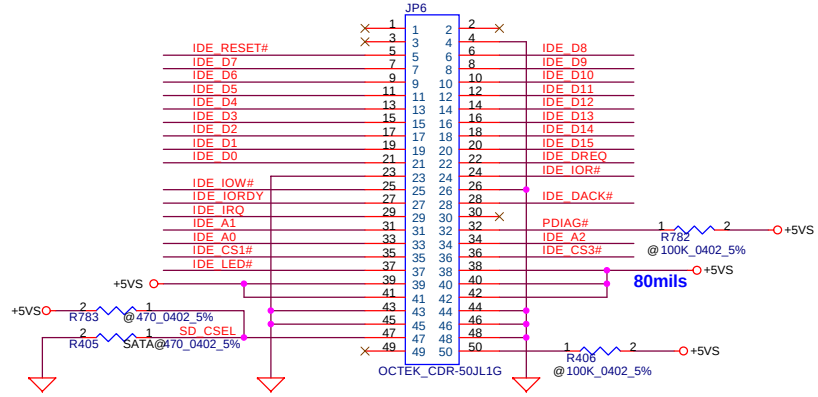


SATA HDD Conn.



(NEW)

CDROM CONN



IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

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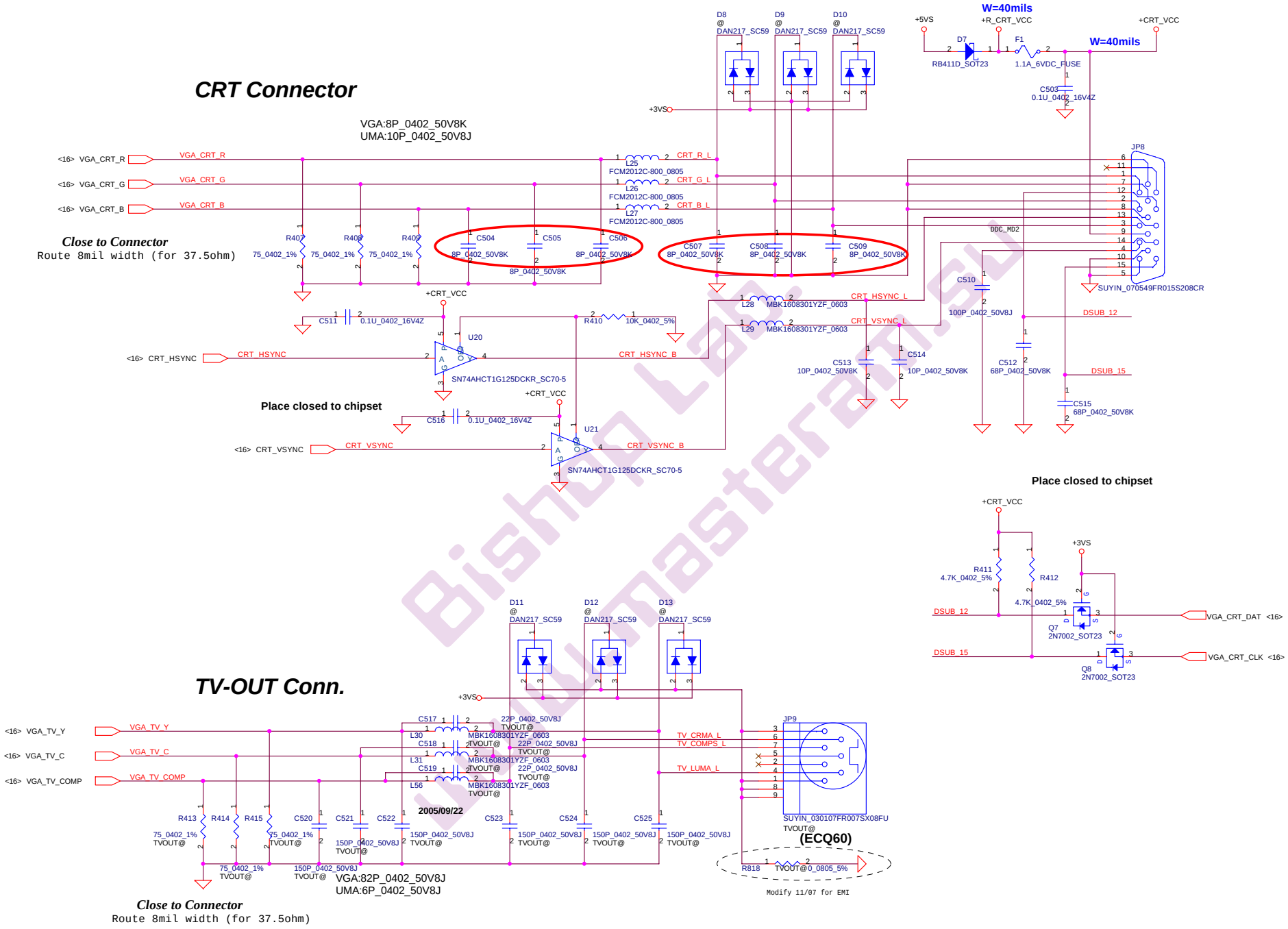

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Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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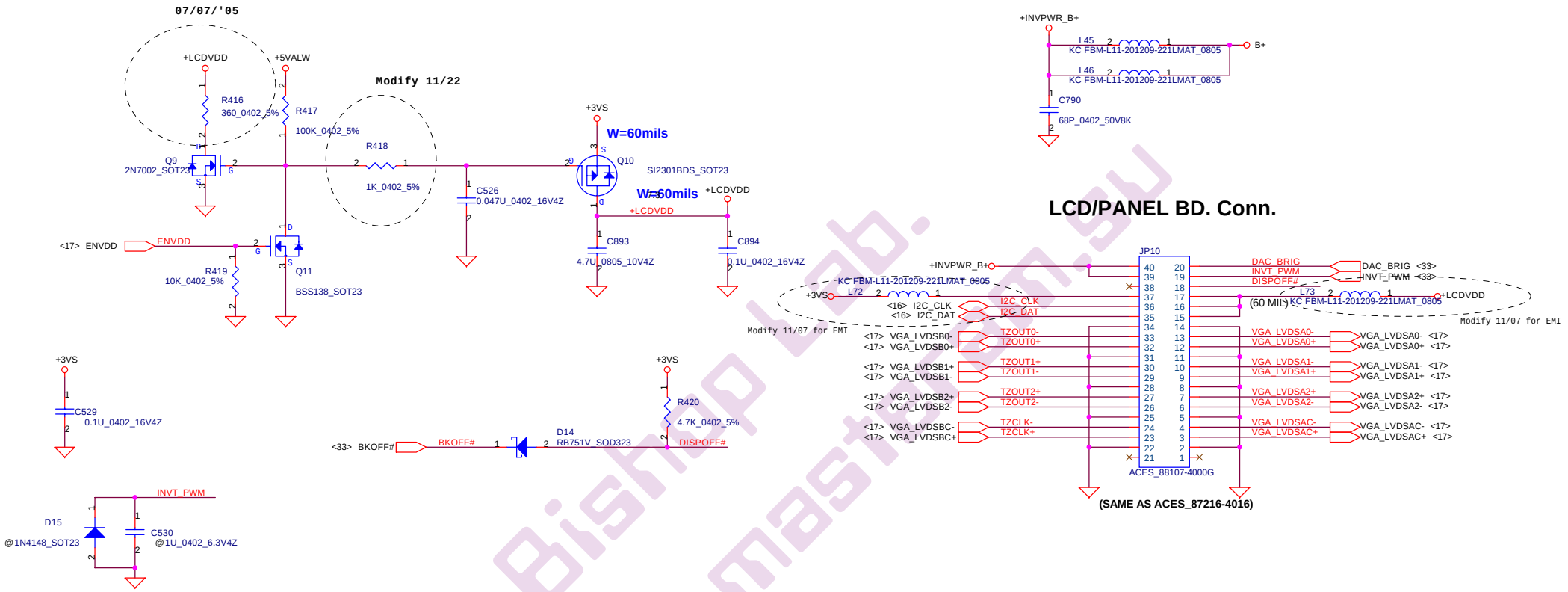
LCD POWER CIRCUIT



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Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

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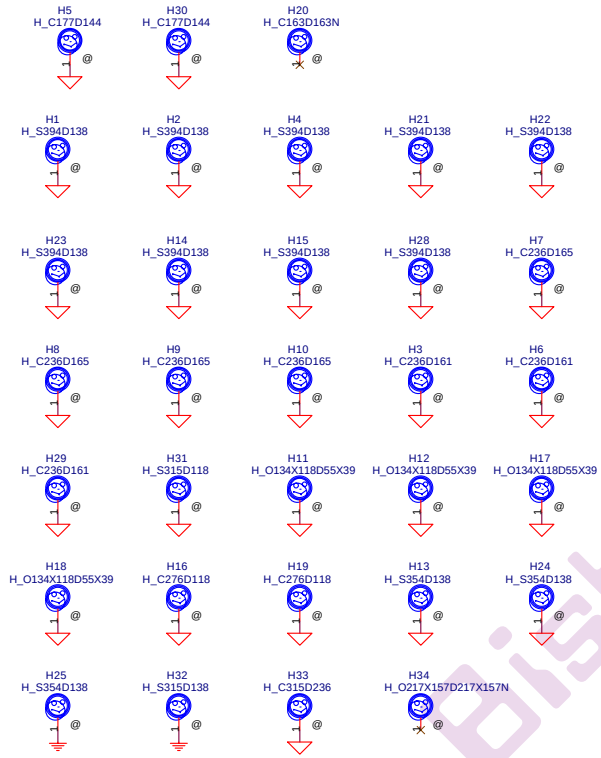
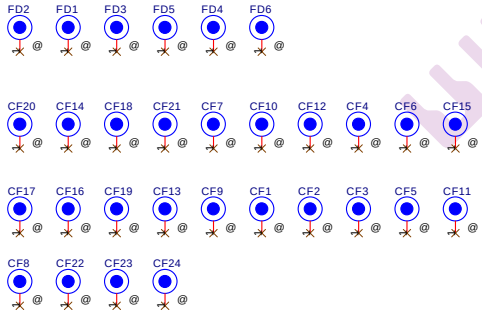
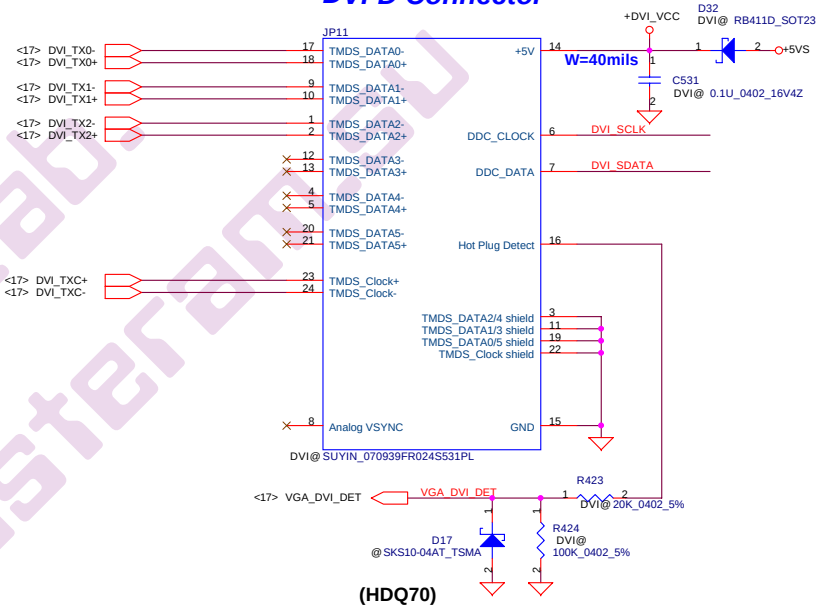
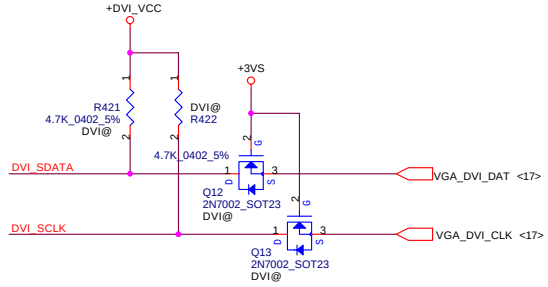




DVI-D Connector





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Issued Date	2005/06/20	Deciphered Date	2006/06/20

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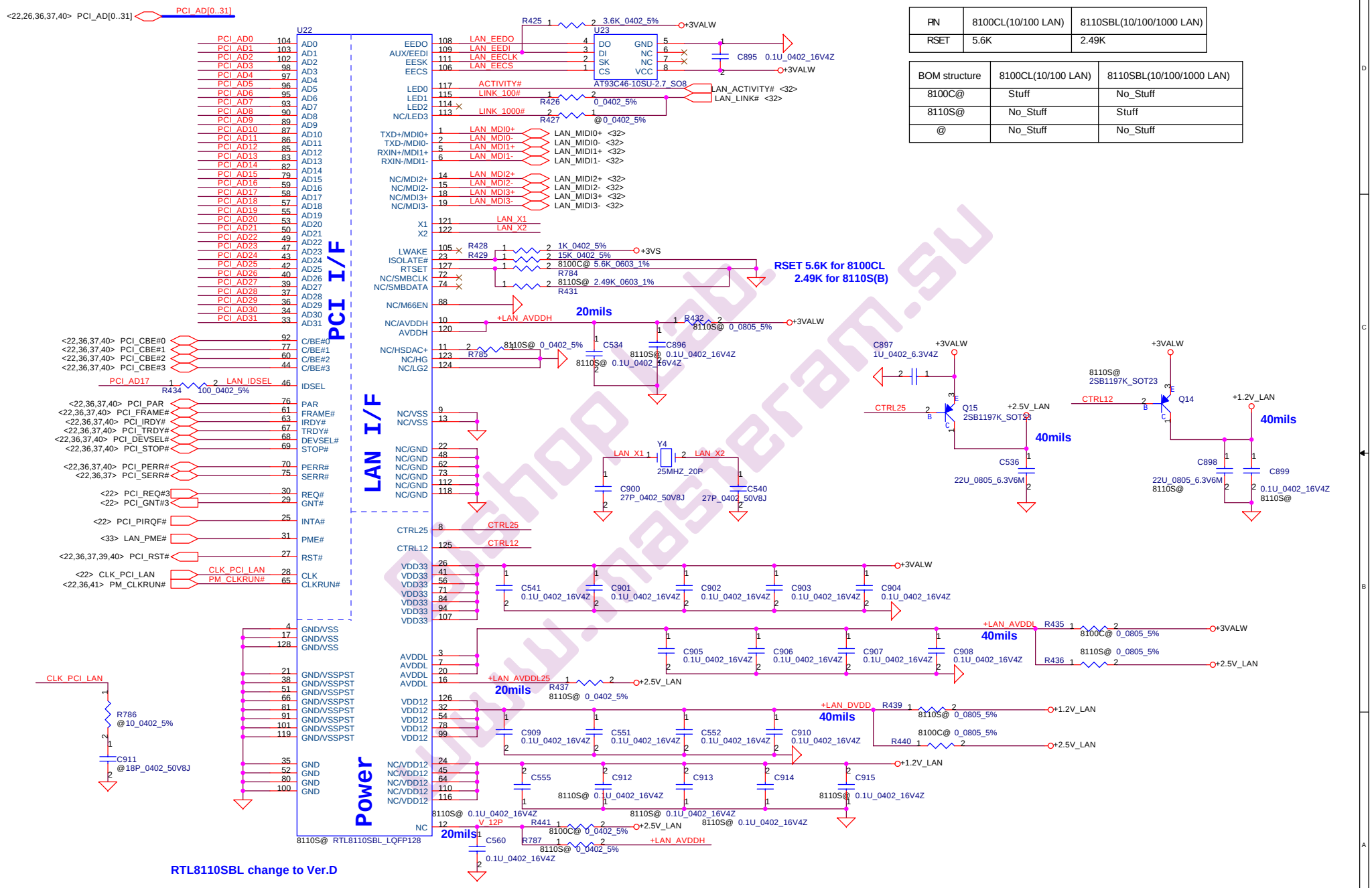

PIN	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
RSET	5.6K	2.49K

BOM structure	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
8100C@	Stuff	No_Stuff
8110S@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

Security Classification	Compal Secret Data		
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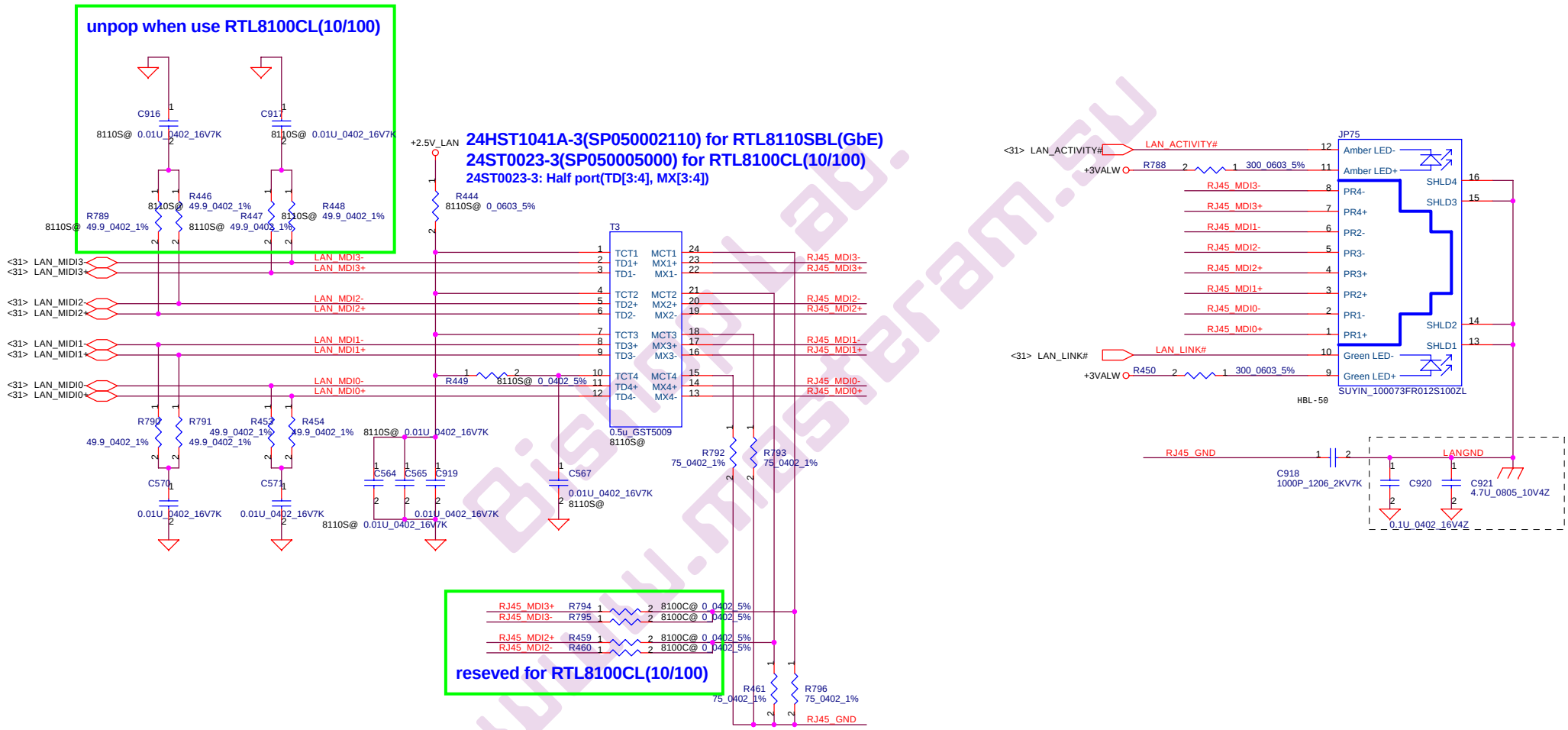
LAN RTL8110SBL/RTL8100CL



Security Classification	Compal Secret Data		
Issued Date	2005/07/29	Deciphered Date	2006/07/29

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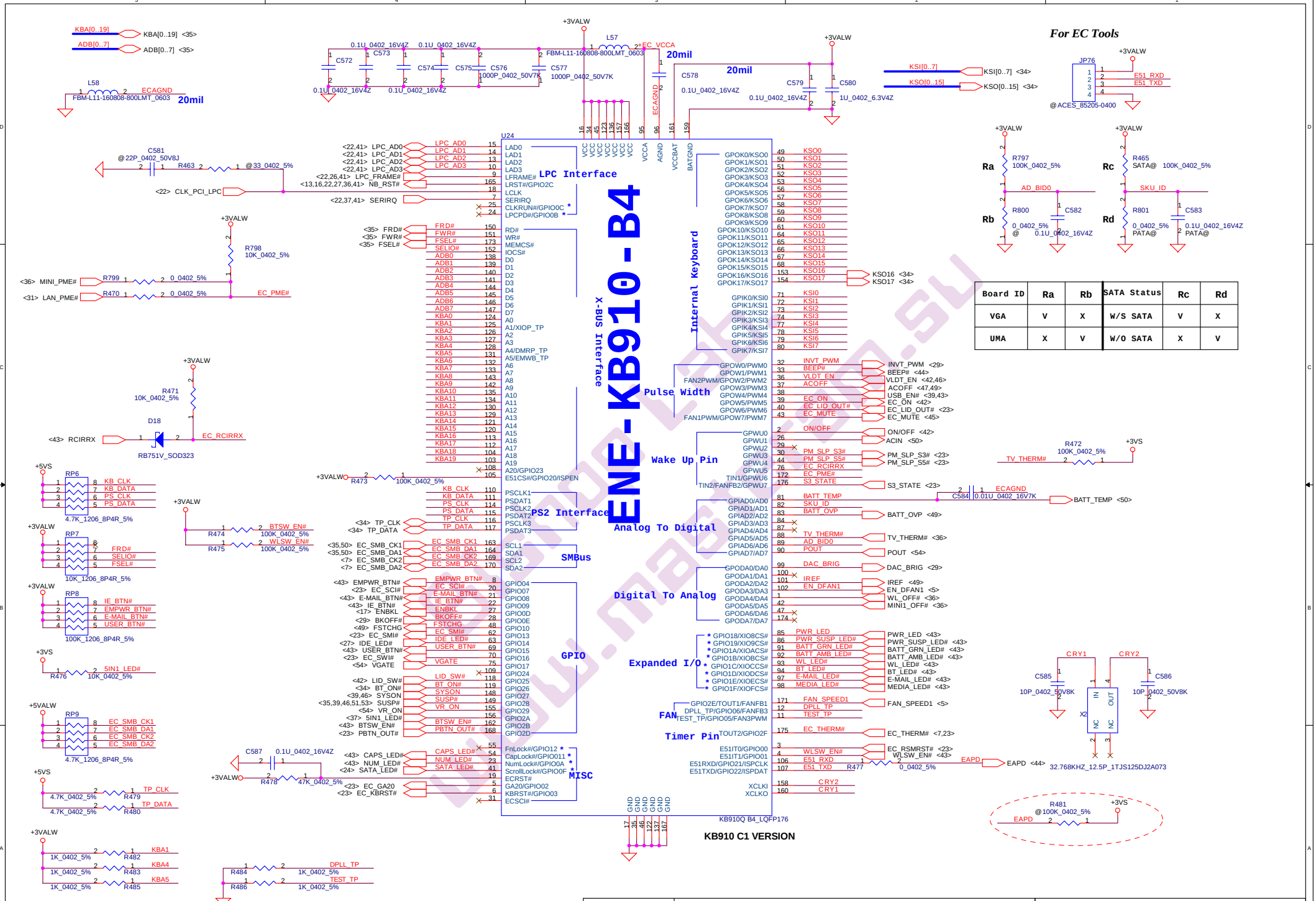
For EC Tools
ENE-KB910-B4
KB910Q B4_LQFP176
KB910 C1 VERSION
LPC Interface
X-BUS Interface
PS2 Interface
SMBus
GPIO
MISC
Internal Keyboard
Pulse Width
Wake Up Pin
Analog To Digital
Digital To Analog
Expanded I/O
FAN
Timer Pin
Board ID | Ra | Rb | SATA Status | Rc | Rd
VGA | V | X | W/S SATA | V | X
UMA | X | V | W/O SATA | X | V
Security Classification | Compal Secret Data
Issued Date | 2005/06/20 | Deciphered Date | 2006/06/20
Compal Electronics, Inc.
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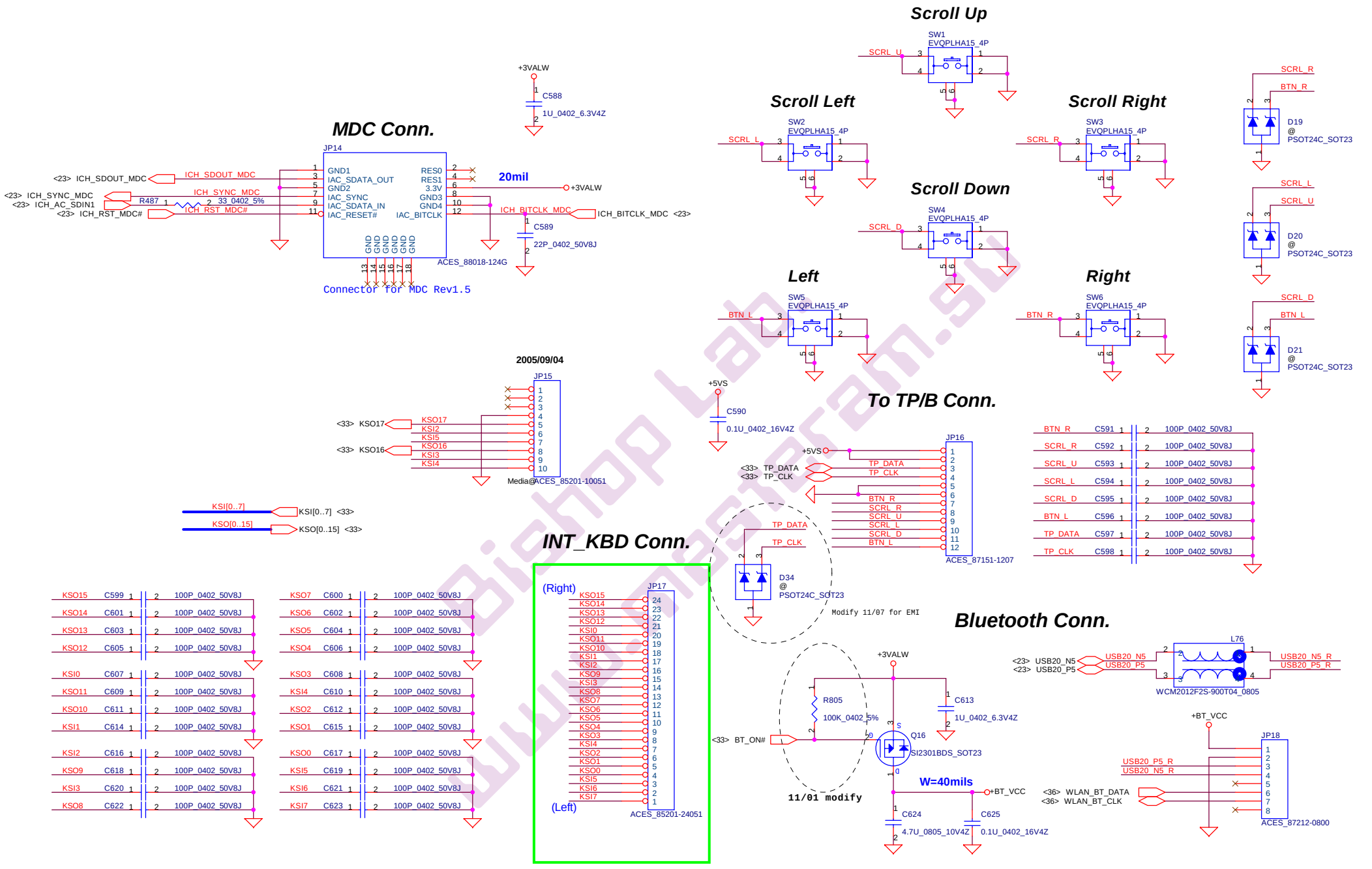

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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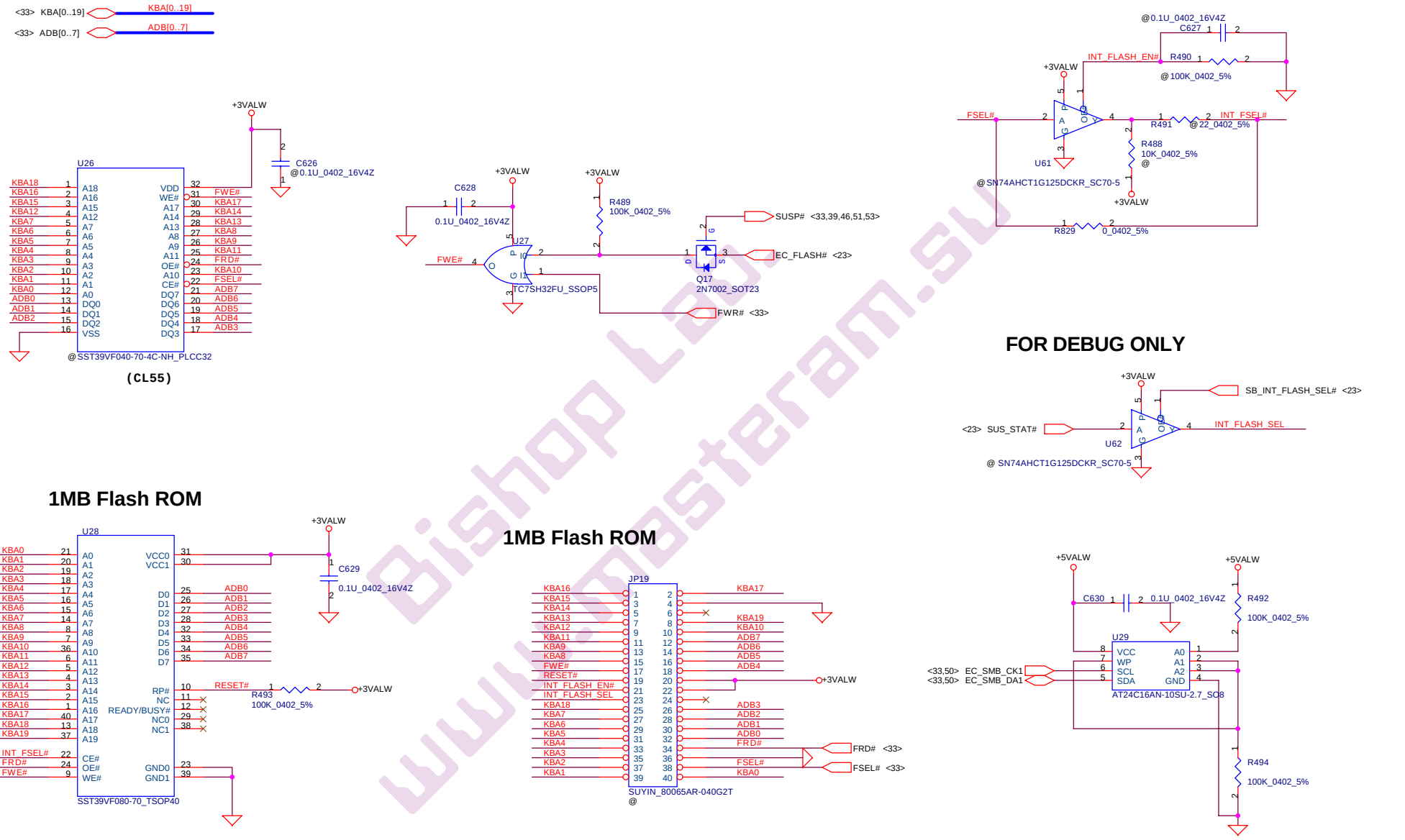

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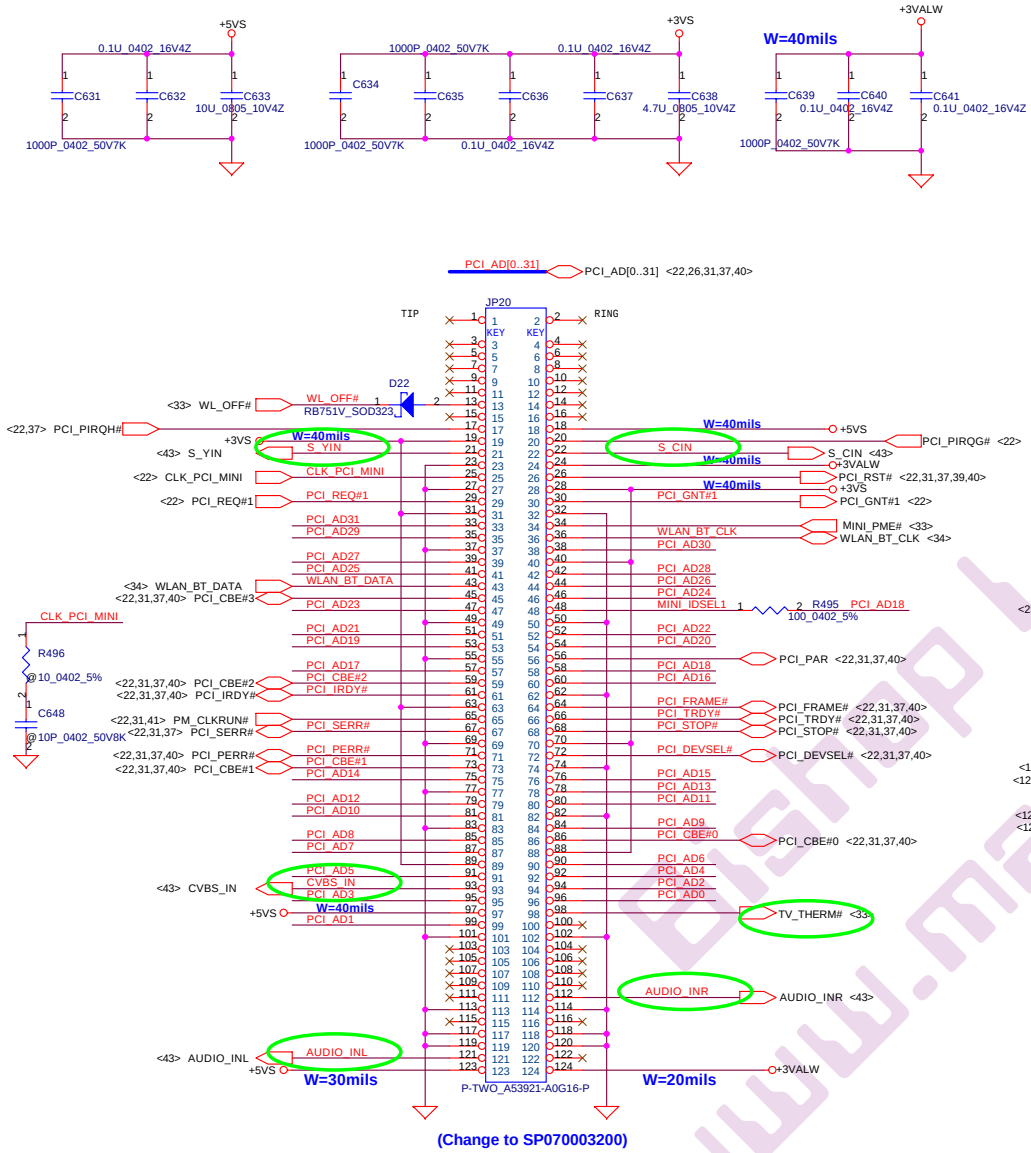

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
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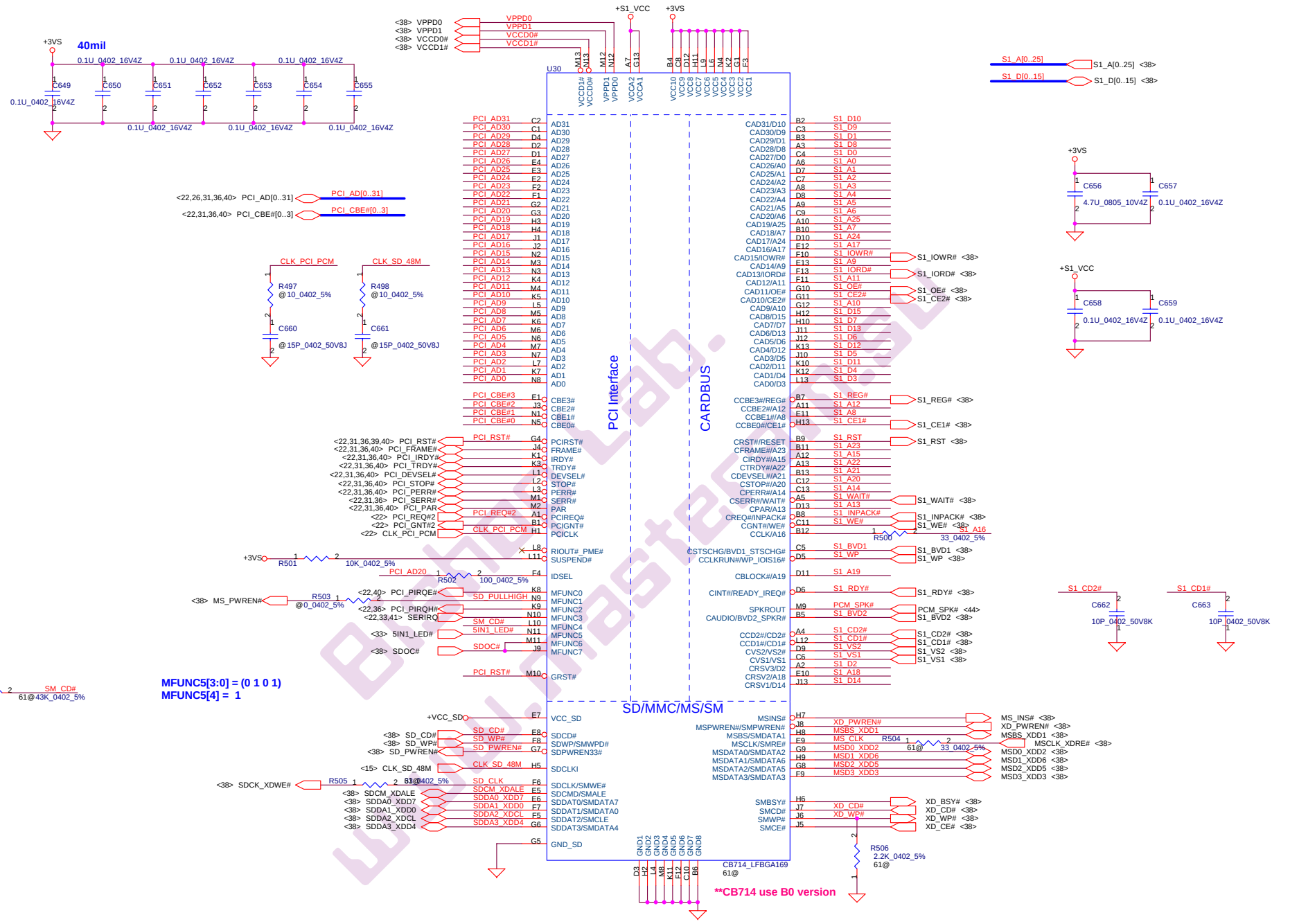

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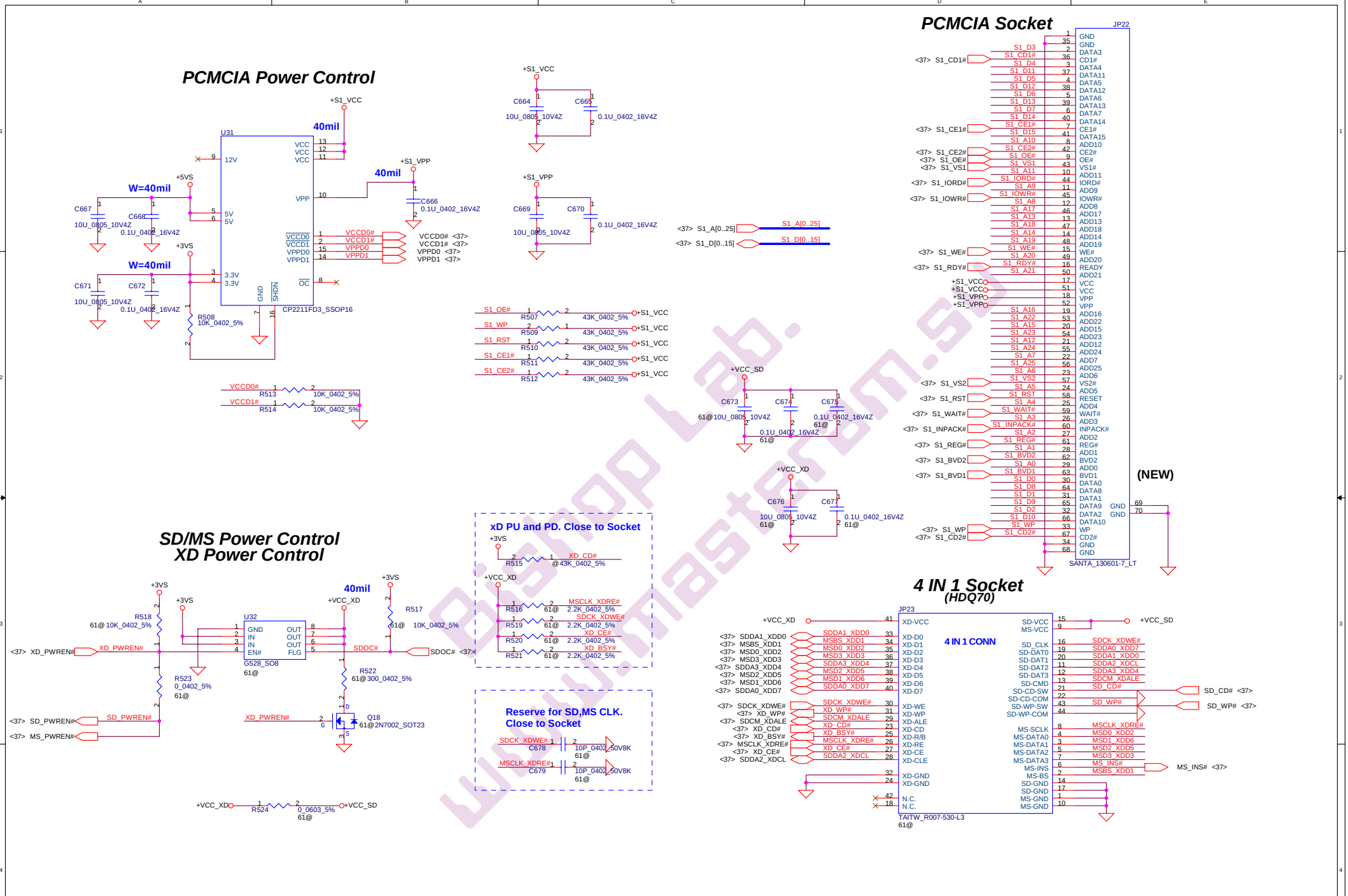

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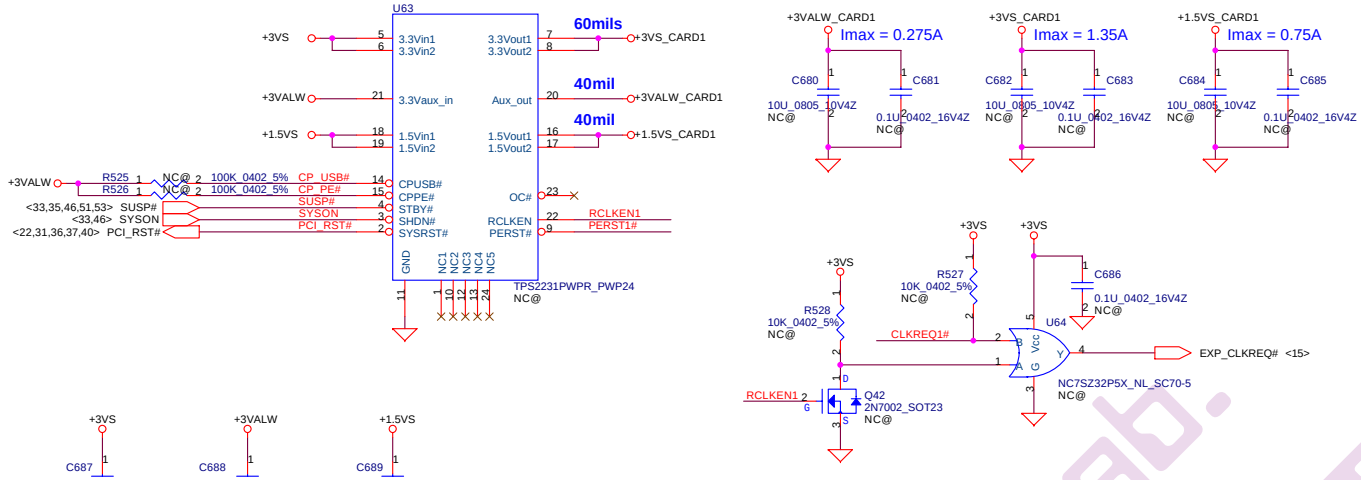
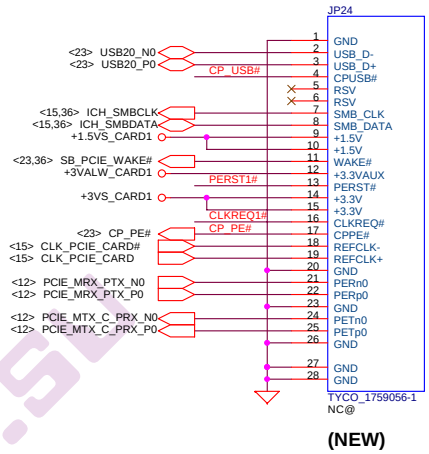
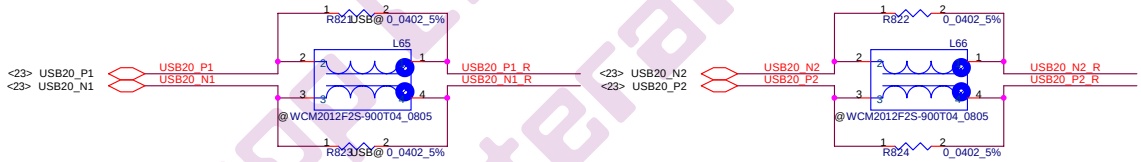
New Card Power Switch



New Card Socket (Left)

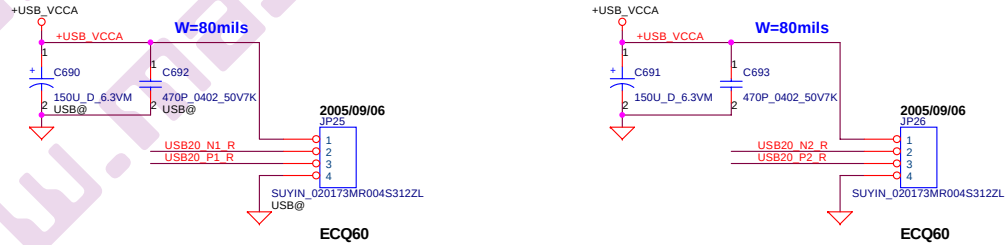


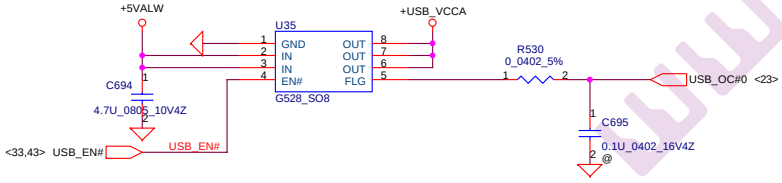
(NEW)



USB Component co-layout

USB CONN. 1 & 2





SUYIN_020173MR004G533ZR_4P

SUYIN_020173MR004G533ZR_4P

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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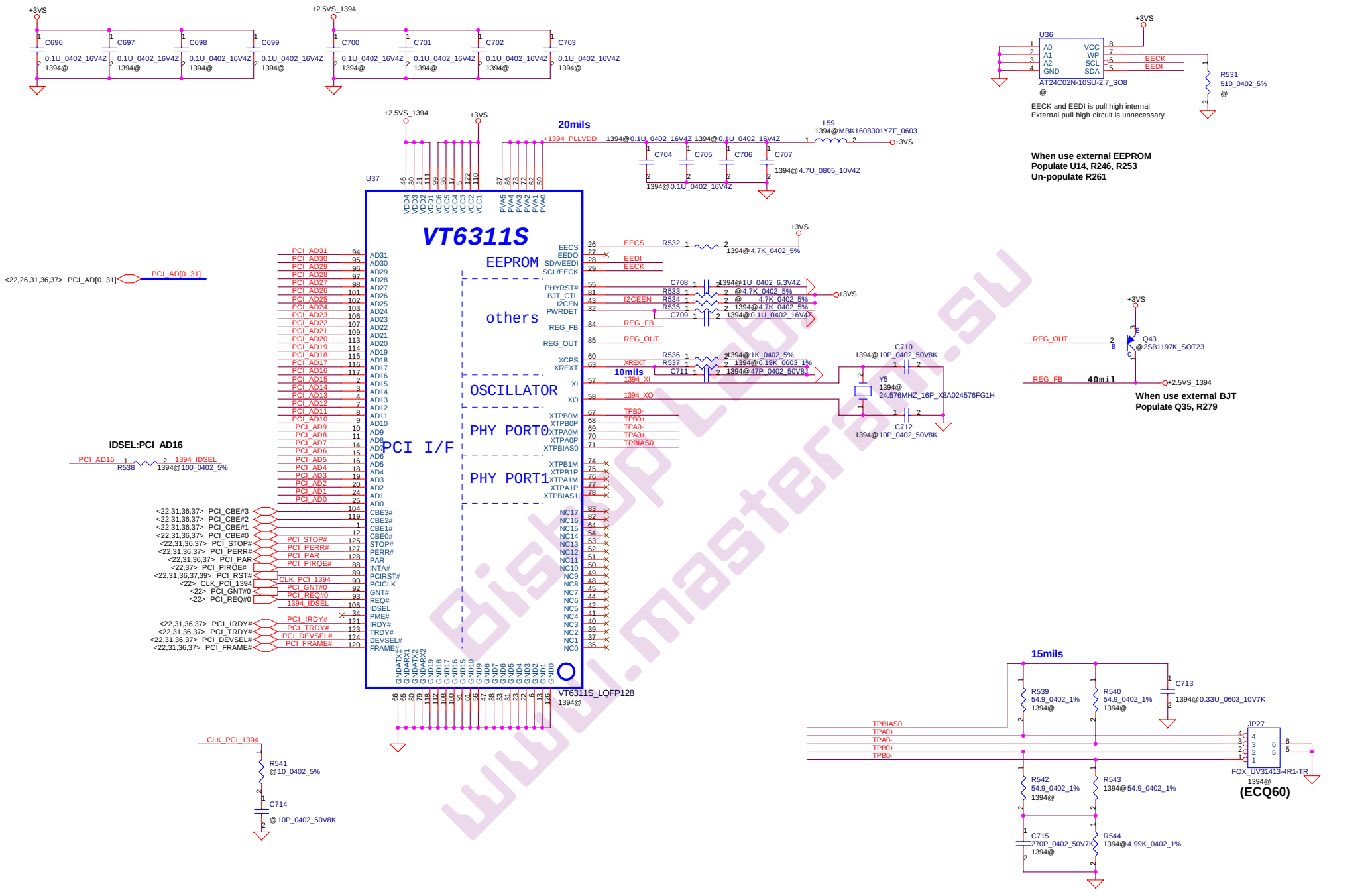

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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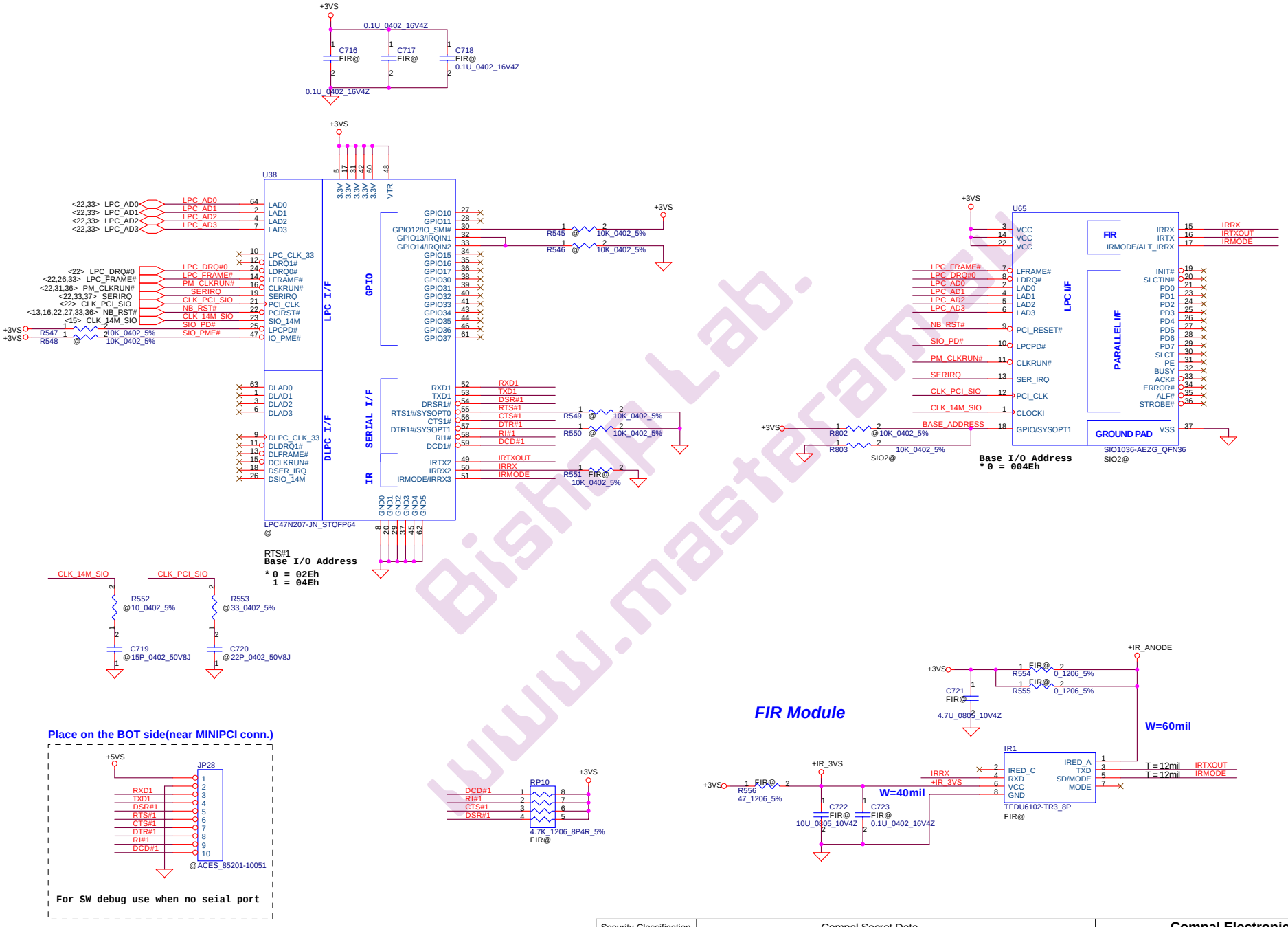
SUPER I/O SMsC LPC47N207



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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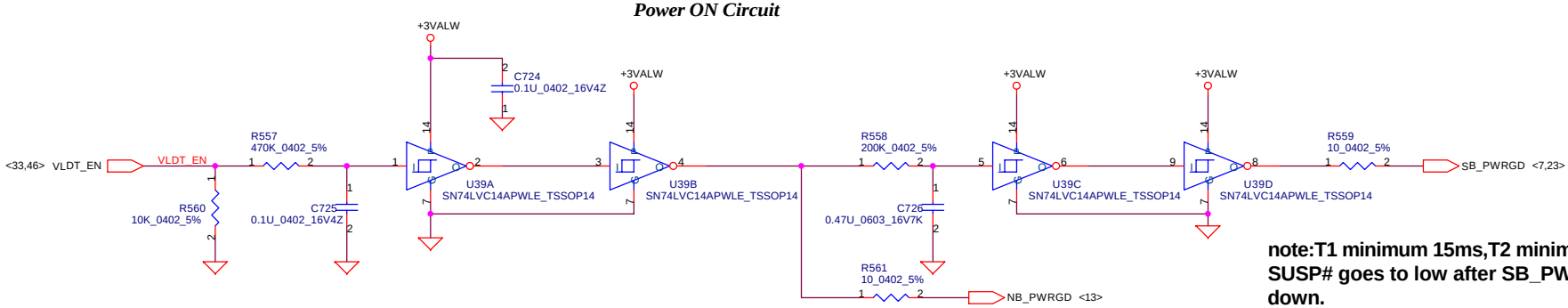
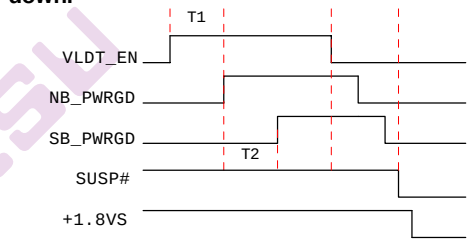
Power ON Circuit

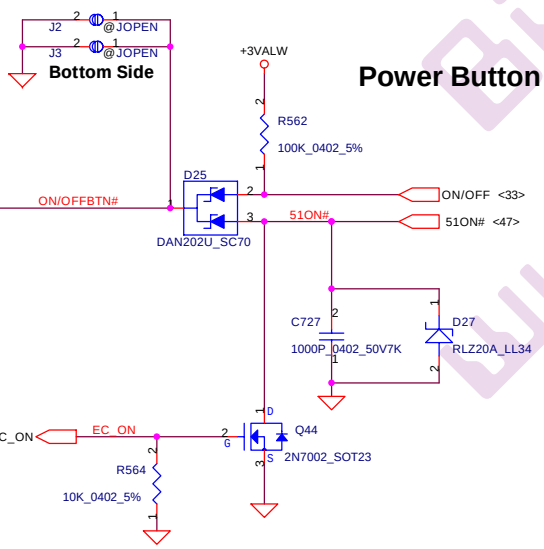


note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



ON/OFF switch

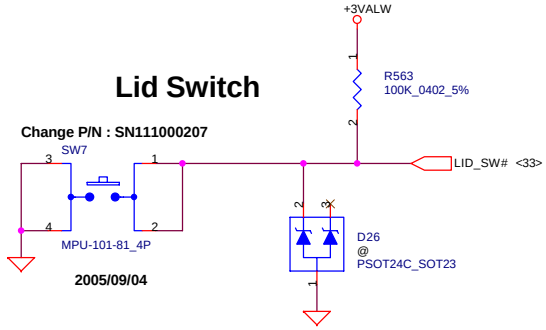
TOP Side



Power Button

Lid Switch

Change P/N : SN111000207



2005/09/04

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

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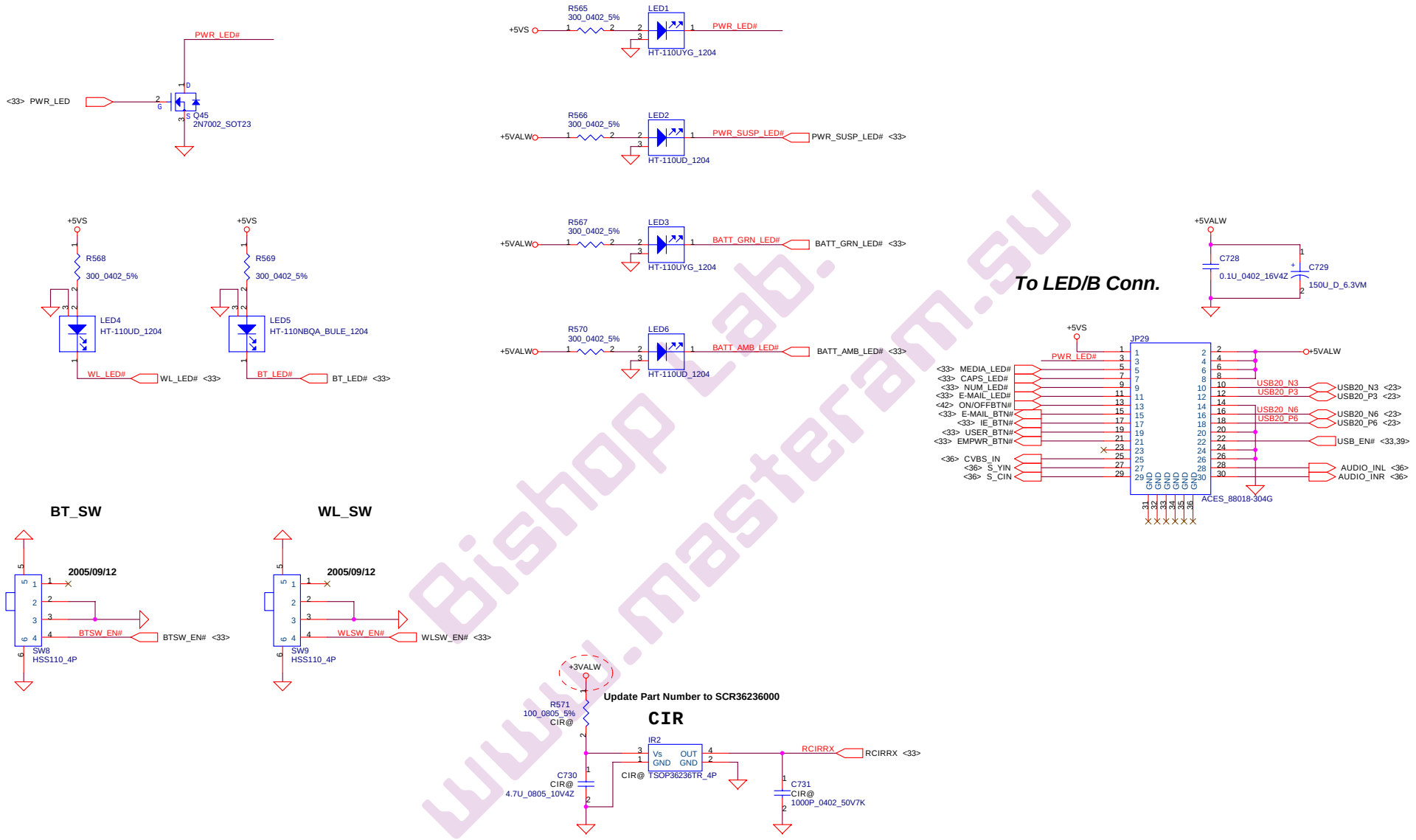

Geneva 2005/09/04 **Grapevine**

	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	
KSI4	NEXT	
KSI5	REV	
KSI6		RECORD

	KSO16	KSO17
KSI2	PLAY	
KSI3	STOP	VOL_UP
KSI4	NEXT	VOL_DOWN
KSI5	REV	ARCADE_TV

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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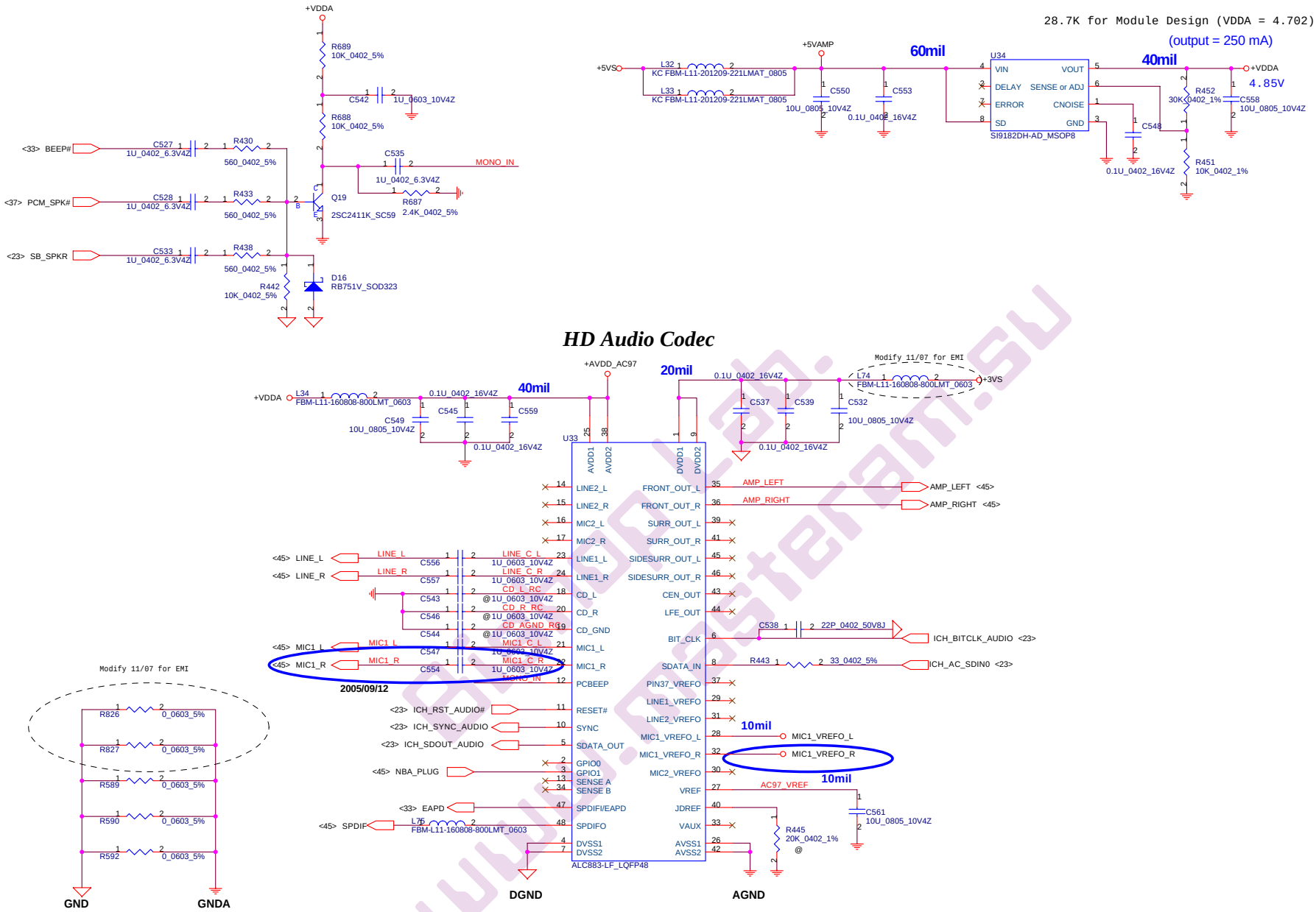

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

Size: Custom | Document Number: 401412 | Rev: B

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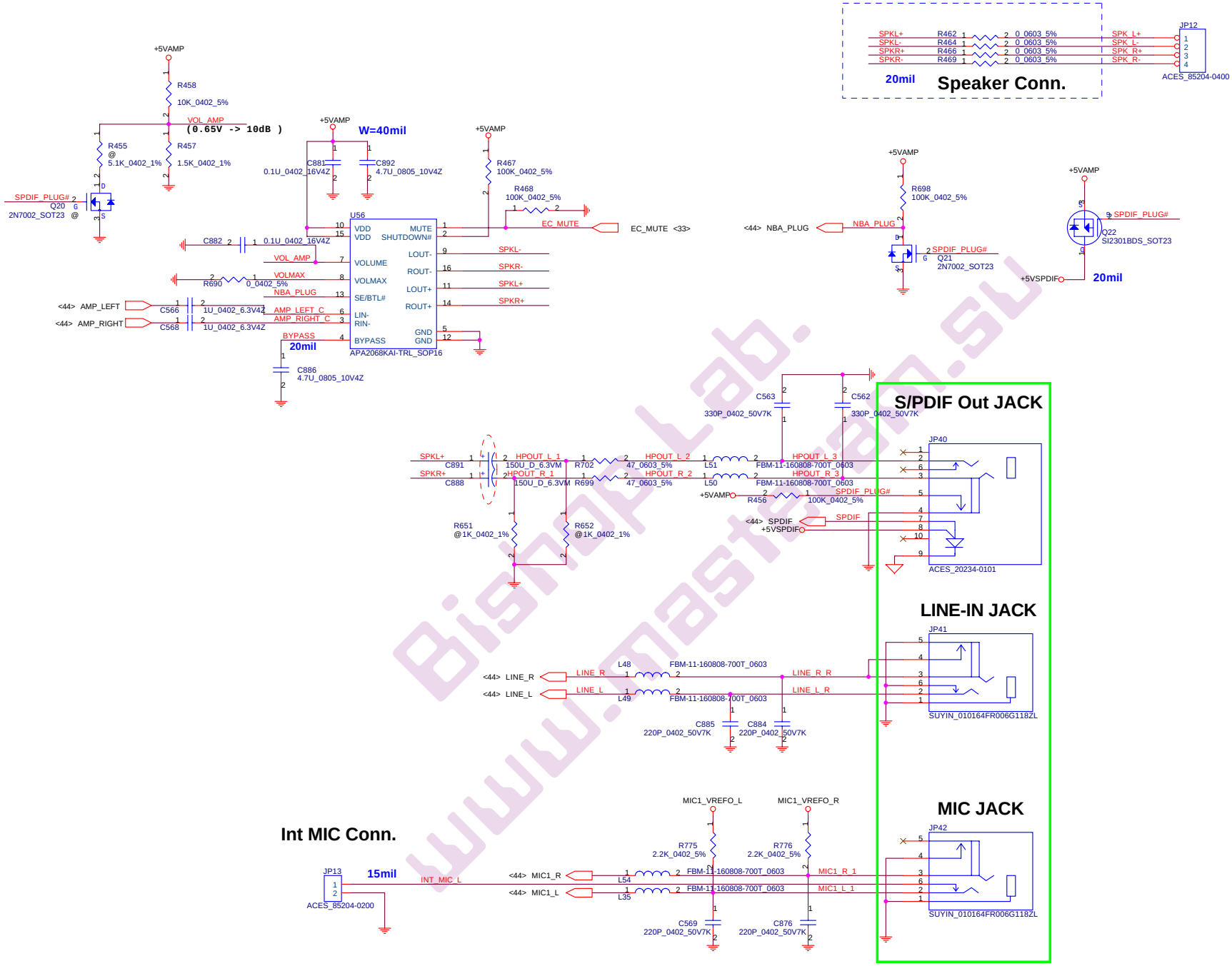

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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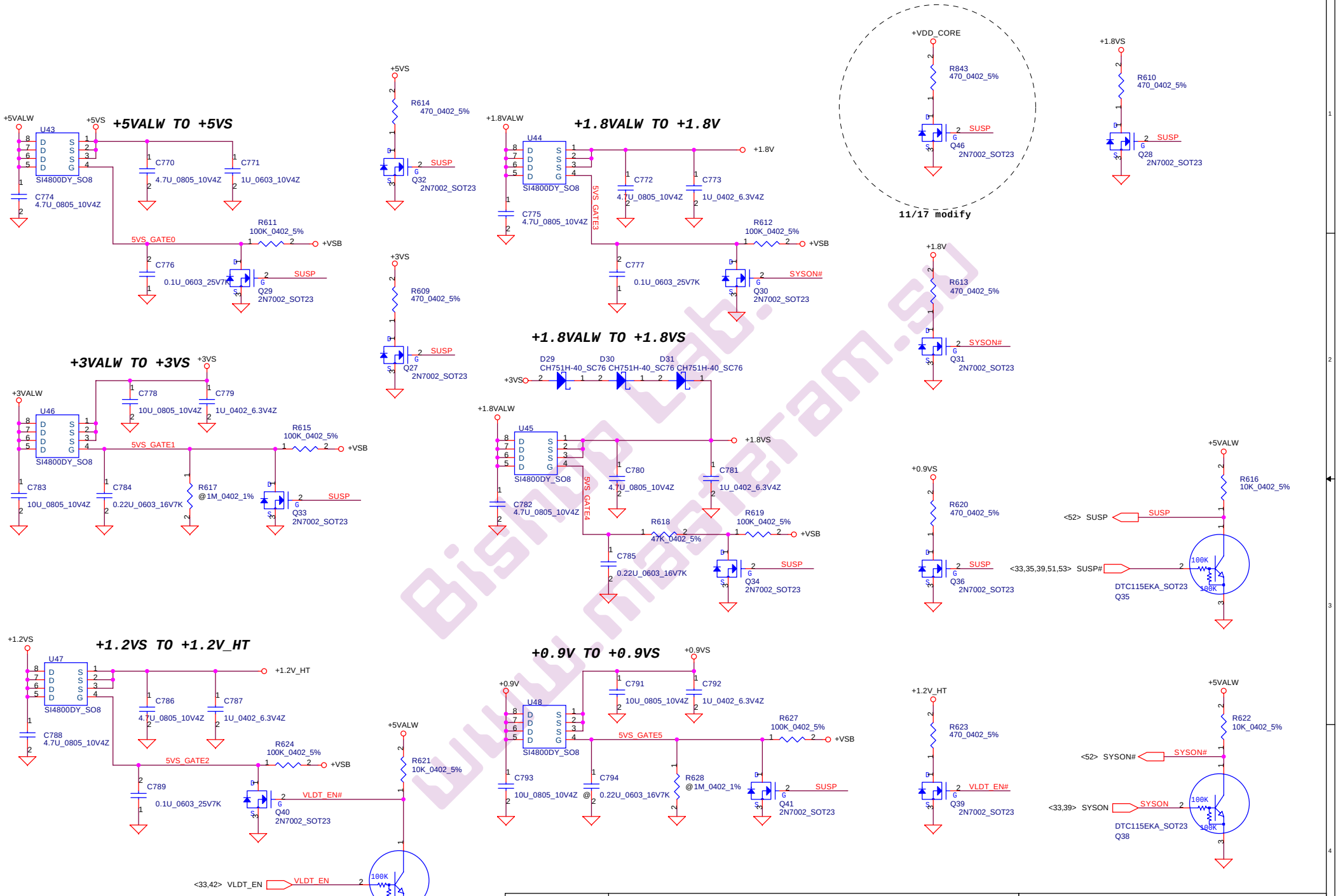

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

Size: Custom | Document Number: 401412 | Rev: B

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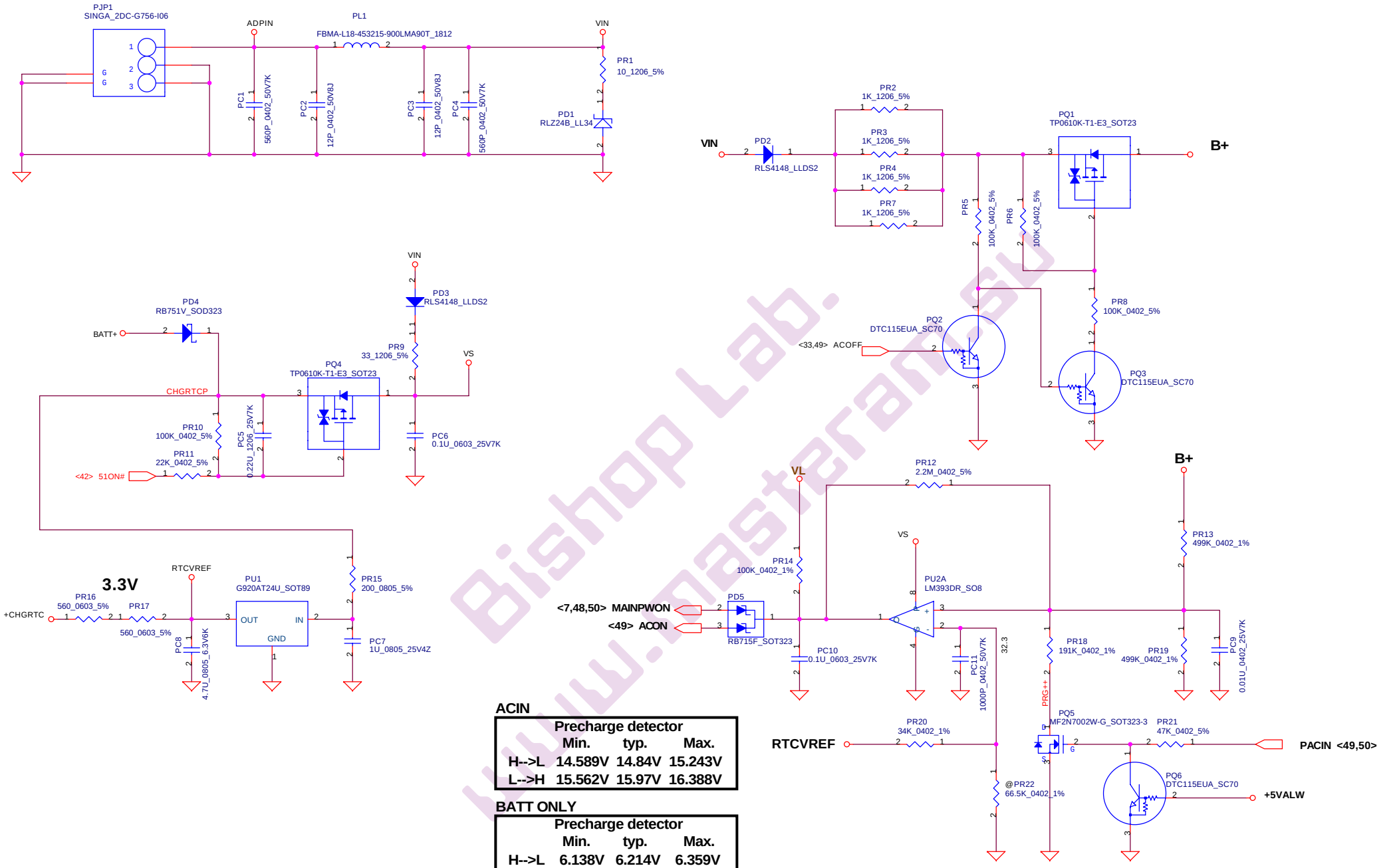

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2005/0926	Deciphered Date	2006/0926

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

Size: B | Document Number: 401412 | Rev: B

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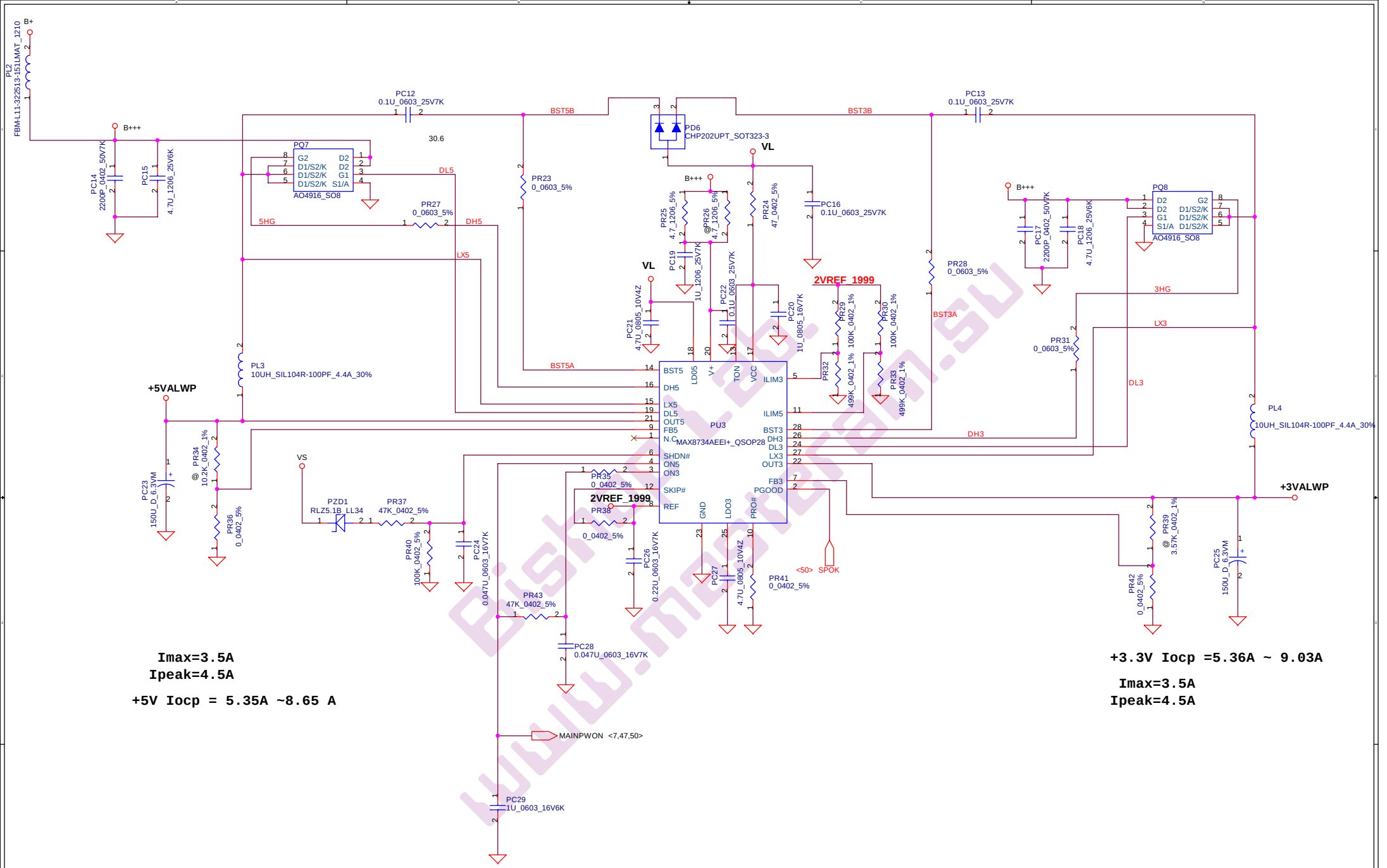

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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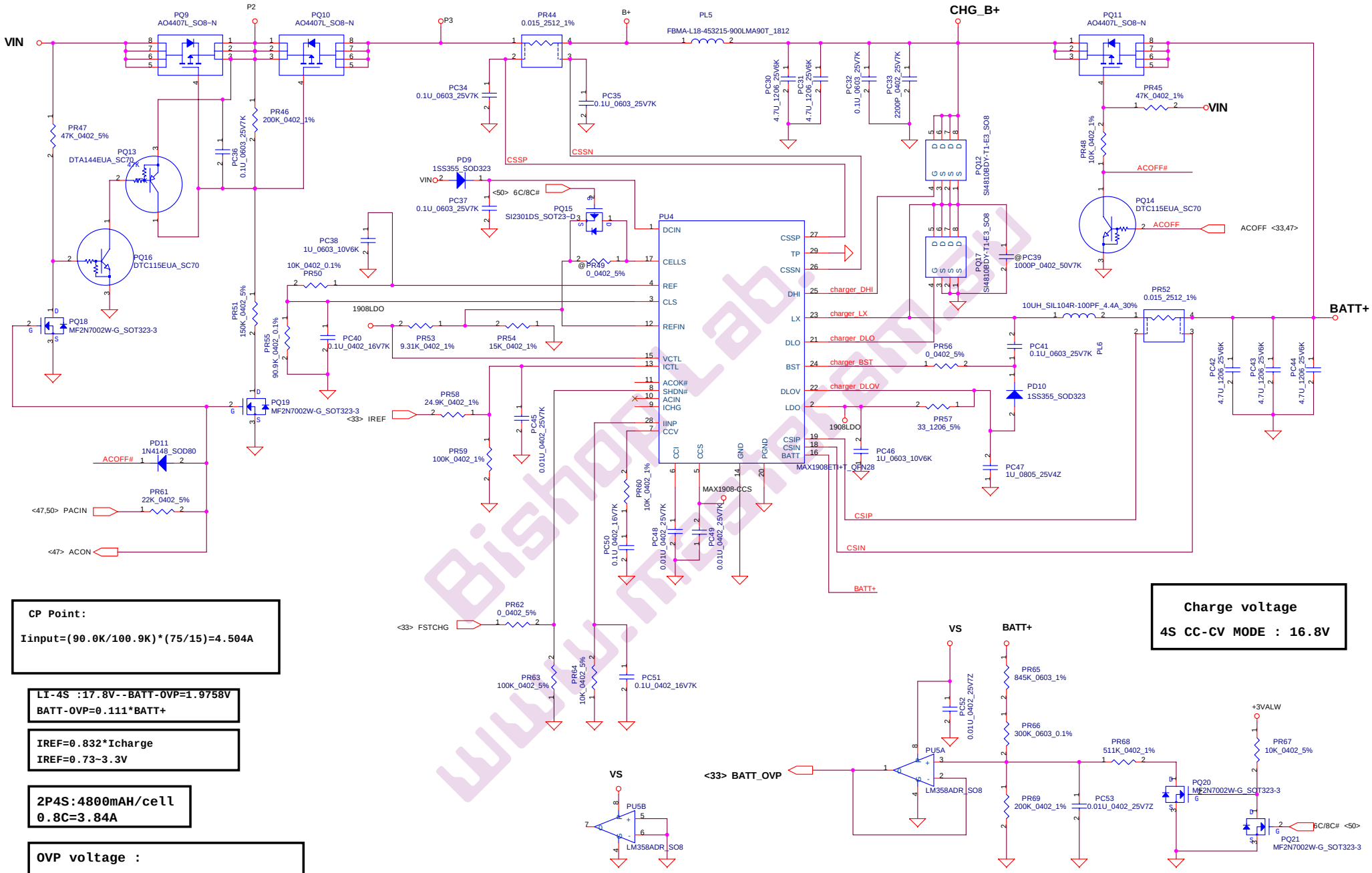
Charger

Iadp=0~4.5A(90W)



CP Point:

Iinput=(90.0K/100.9K)*(75/15)=4.504A

LI-4S :17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

2P4S:4800mAH/cell
0.8C=3.84A

OVP voltage :

LI-3S :17.8V----BATT-OVP=1.9758V

BATT-OVP=0.111*BATT+

Charge voltage

4S CC-CV MODE : 16.8V

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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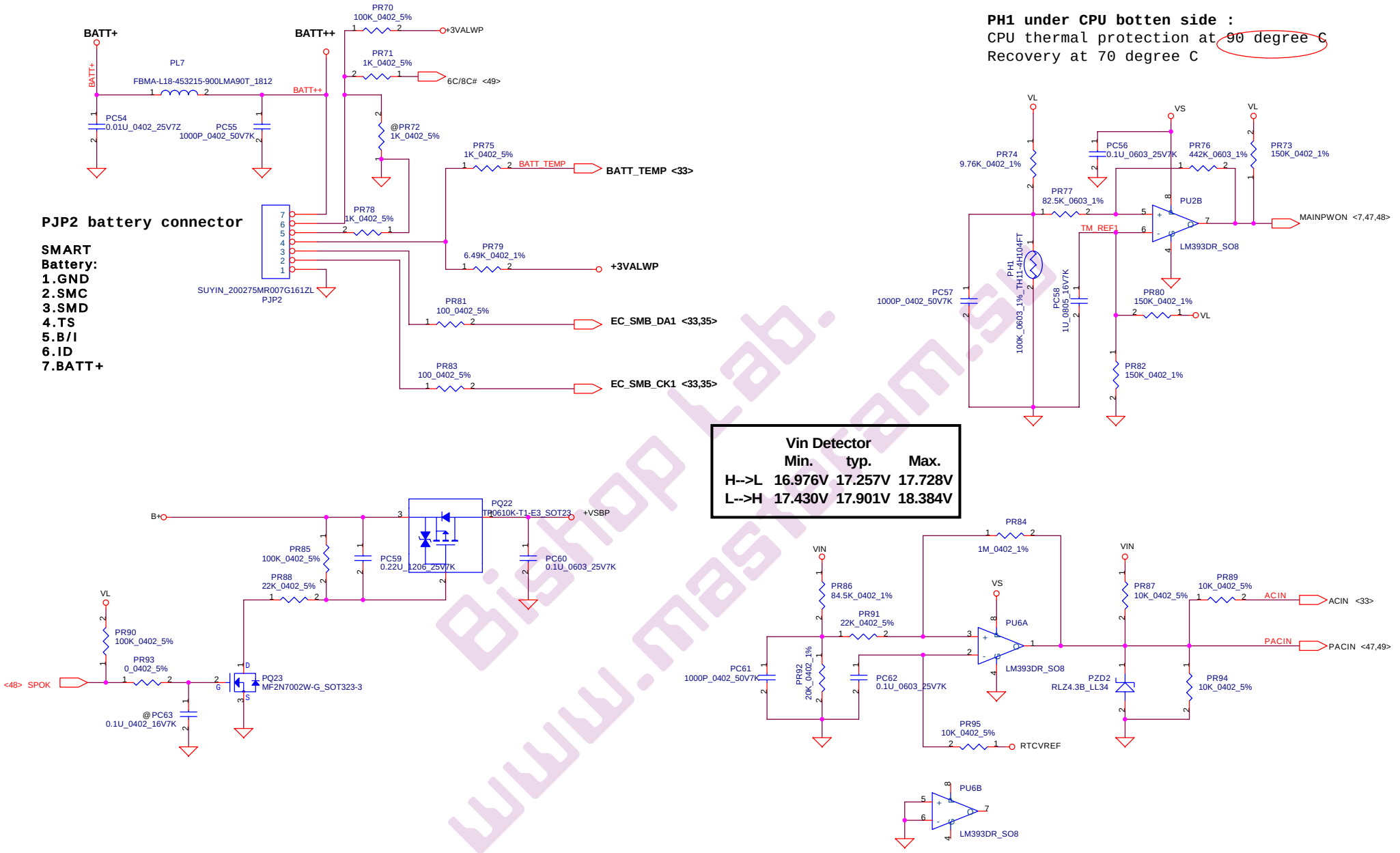

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: **SCHEMATIC, M/B LA-3151P**

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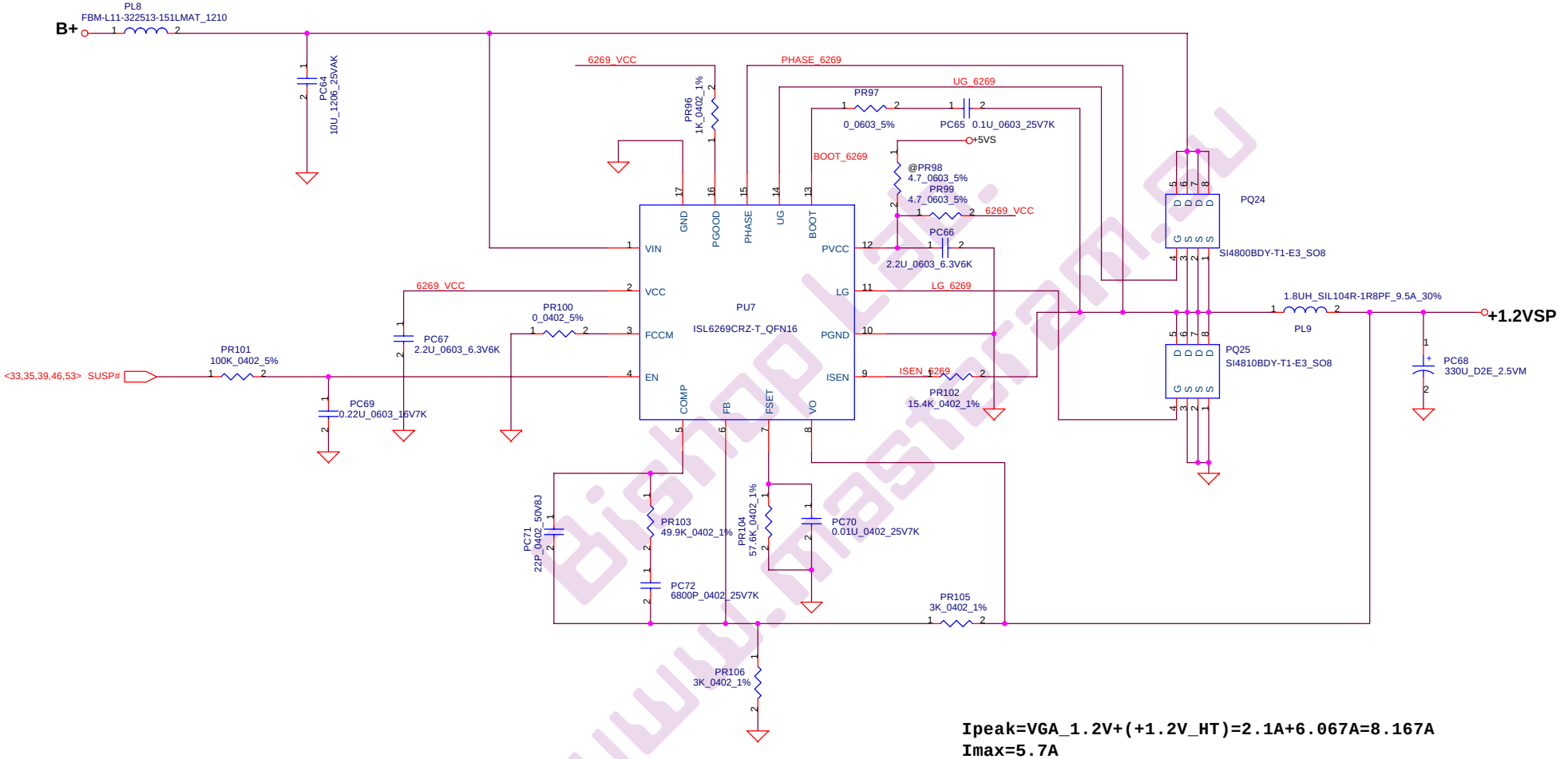

Ipeak=VGA_1.2V+(+1.2V_HT)=2.1A+6.067A=8.167A
Imax=5.7A
Iocmin=9.23A
Iocmax=19.23A

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: **SCHEMATIC, M/B LA-3151P**

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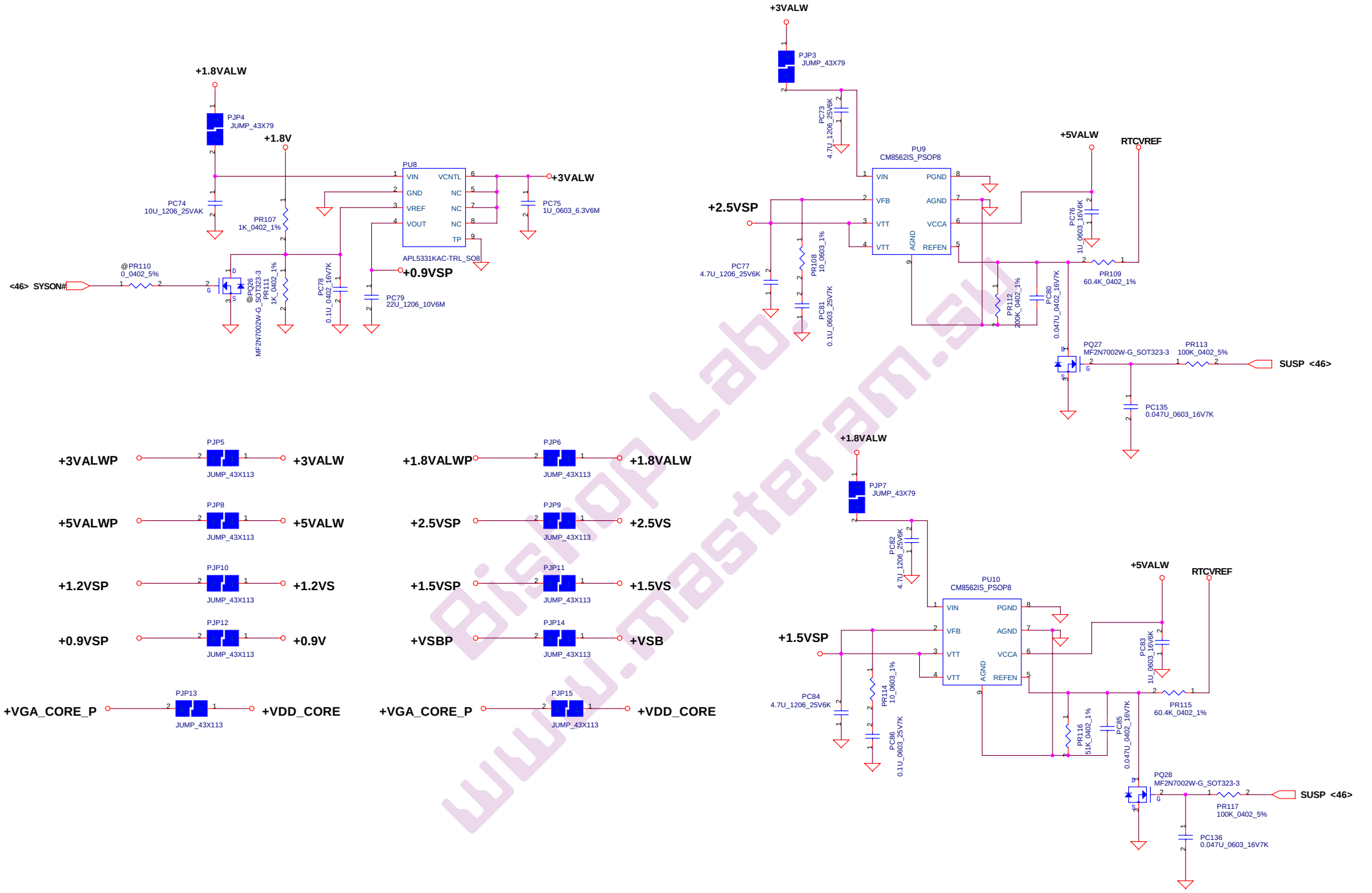

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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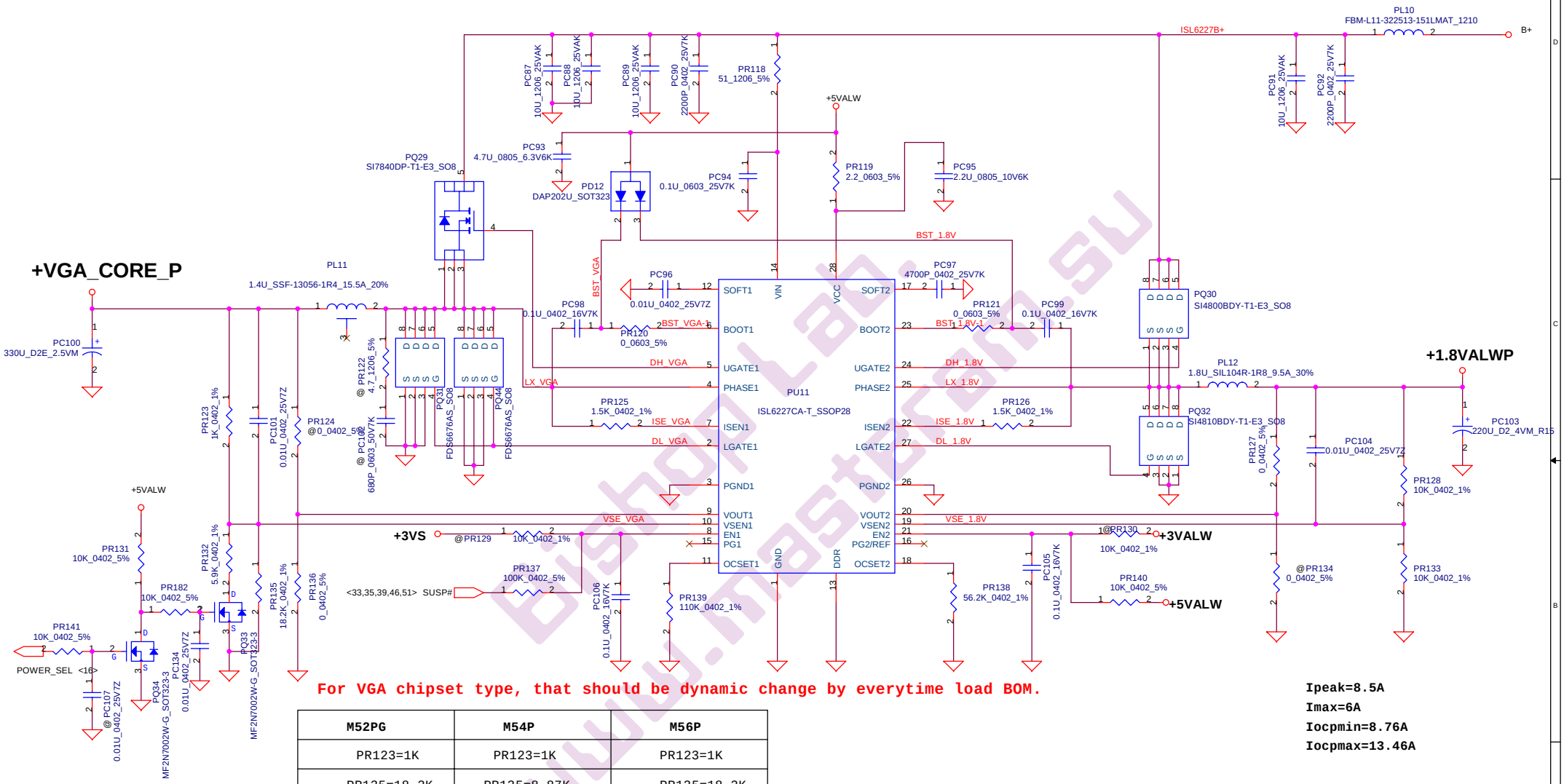

For VGA chipset type, that should be dynamic change by everytime load BOM.

M52PG	M54P	M56P
PR123=1K	PR123=1K	PR123=1K
PR135=18.2K	PR135=8.87K	PR135=18.2K
PR132=17.8K	PR132=8.87K	PR132=5.9K
L=1.000V	**L=1.102V**	**L=1.102V**
H=0.949V	**H=1.001V**	**H=0.949V**

Ipeak=16.40A
Imax=12.25A
Iocpmin=22.07A
Iocpmax=38.67A

Ipeak=8.5A
Imax=6A
Iocpmin=8.76A
Iocpmax=13.46A

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, inc.

Title: **SCHEMATIC, M/B LA-3151P**

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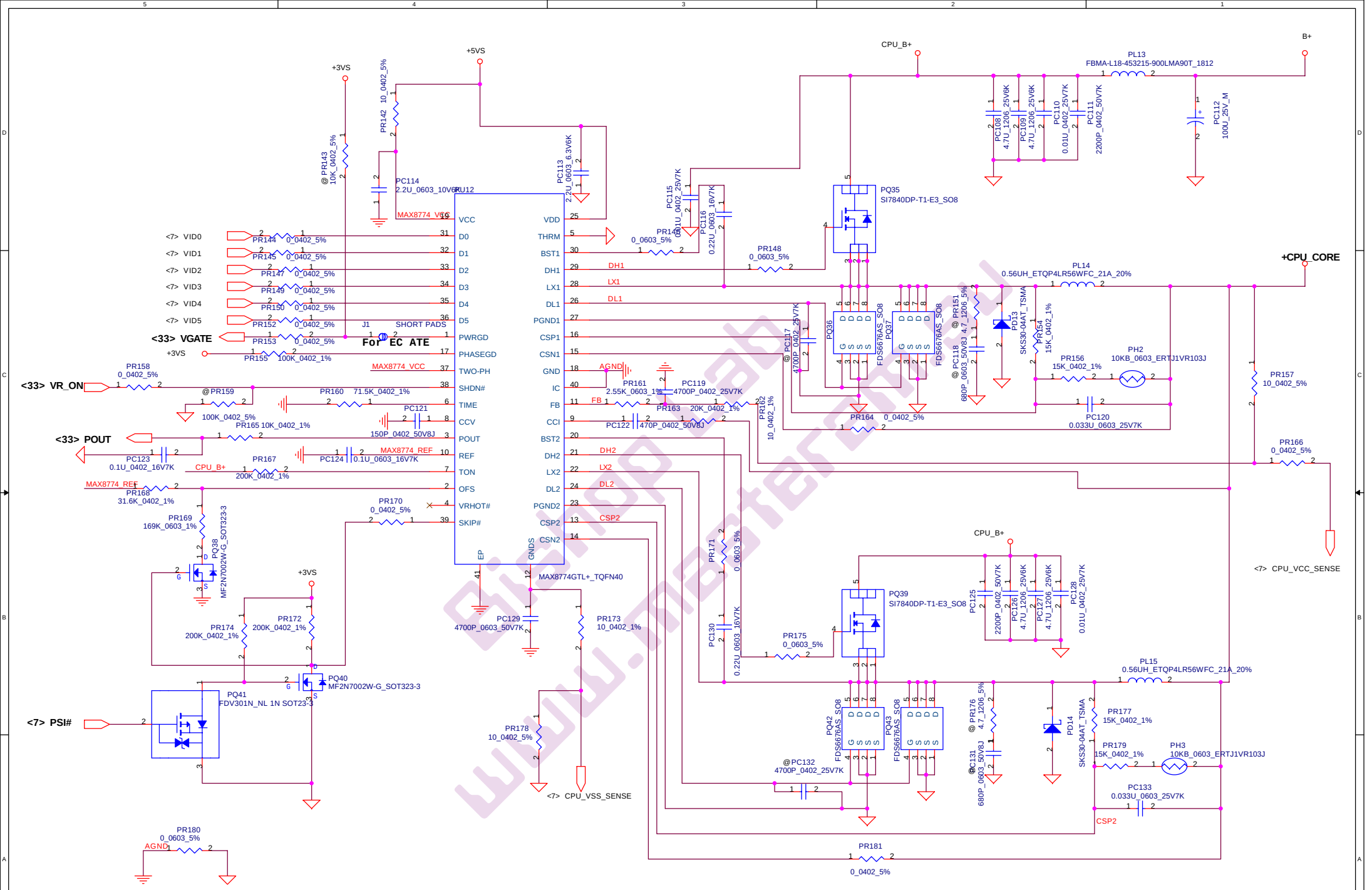

Security Classification	Compal Secret Data		
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Compal Electronics, inc.

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							