KSWAA/KTWAA

Liverpool 10M/10MG

Sunderland 10M/10MG

LA-4982P REV 1.0 Schematic

Intel Penryn/ Cantiga/ ICH9M

2009-07-27 Rev. 1.0

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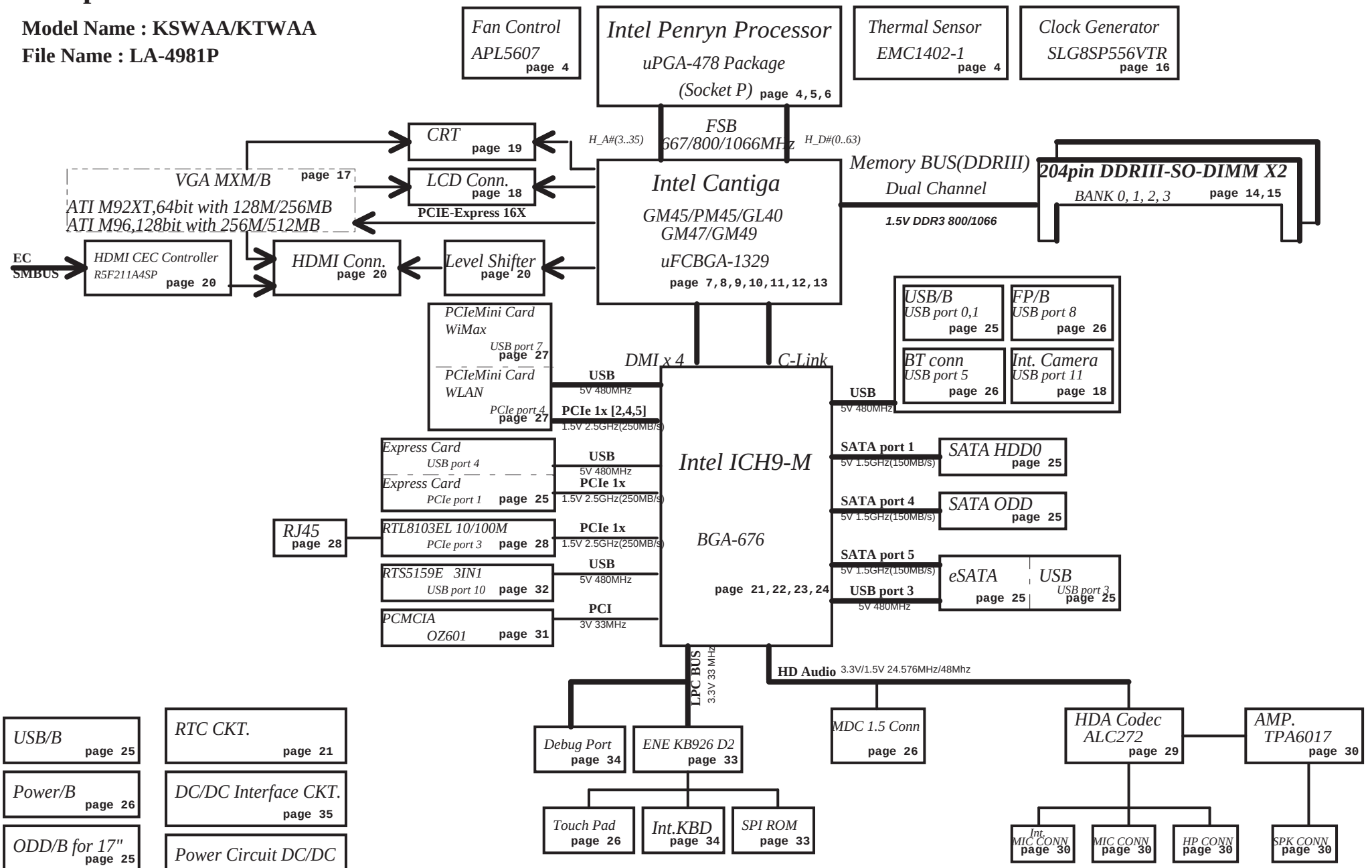
Compal Confidential

Model Name : KSWAA/KTWAA
File Name : LA-4981P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+3VS_HDP	3.3V power rail for G-sensor	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ
CARD BUS	D4	AD20	1	A/B

BTO Option Table

Function	Express Card/ PCMCIA		Bluetooth	RJ11	Camera	3D Sensor
description	(E)	(A)	(B)	(R)	(X)	(S)
explain	Express Card	PCMCIA	Bluetooth	MDC	Camera	3D Sensor
BTO	NEW@	PCM@	BT@	MDC@	CAM@	GSENSOR@

Function	HDMI			
description	(Y)			
explain	Intel(UMA)	ATI VGA/B		COMMON
BTO	IHDMI@	NIHDMI@	HDMI@	H@

EC SM Bus1 address

Power	Device	Address
+5VL	EC KB926 D2	
+5VL	Smart Battery	0001 011X b
+5VL	HDMI-CEC	0011 010x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D2	
+3VS	CPU THM Sen SMSC SMC1402	1001 101Xb
+3VS	VGA THM Sen ADM1032ARMZ	1001 100Xb
	VGA on die thermal sensor	1001 111Xb (No used)

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express Card	

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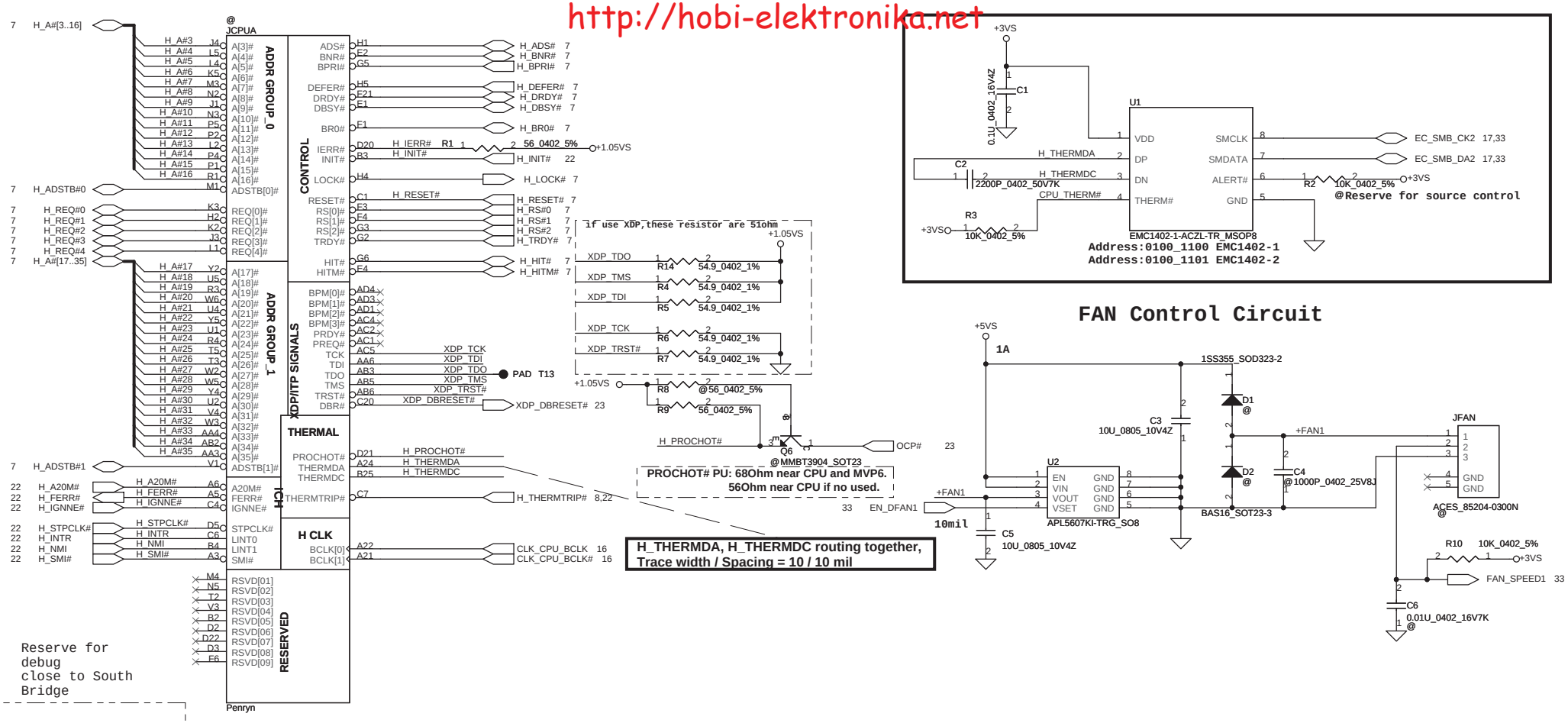

FAN Control Circuit

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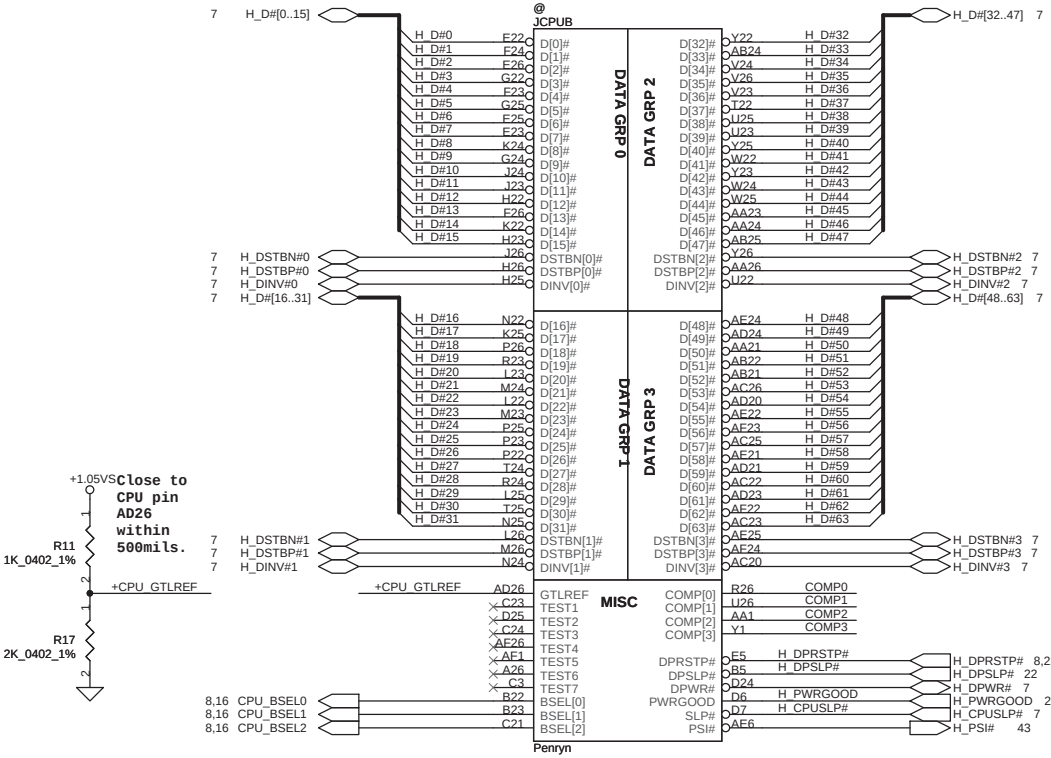
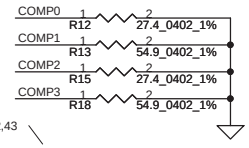


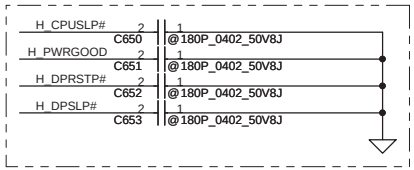


Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

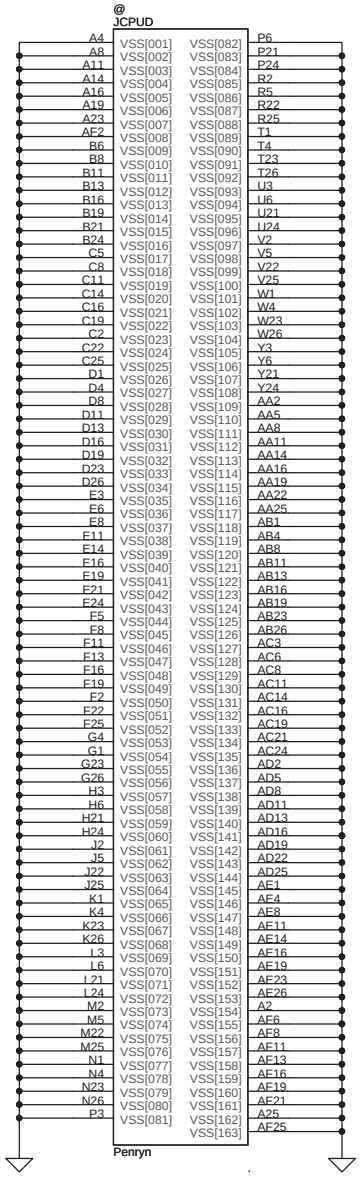
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Reserve for debug close to CPU



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Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

+CPU_CORE
330U_X_2VM_R6M: C7 @, C8 @, C9 @, C10 @

@ JCPUC

reserve for test
please co-layout with C7~C10
330U_6.3V_M_R15: C79, C80, C81, C82

need to change P/N

Penryn

+1.05VS
4.5A
330U_6.3V_M_R15: C43 @, C146
330U_X_2VM_R6M
reserve for test

Near pin B26
C26
C50 0.01U_0402_16V7K
C51 10U_0805_6.3V6M
+1.5VS

CPU_VID0 43
CPU_VID1 43
CPU_VID2 43
CPU_VID3 43
CPU_VID4 43
CPU_VID5 43
CPU_VID6 43
VCCSENSE 43
VSSSENSE 43

+CPU_CORE
VCCSENSE 100_0402_1% R19
VSSSENSE 100_0402_1% R20

Close to CPU pin within 500mils.

Length match within 25 mils. The trace width/space/other is 14/7/25.

+CPU_CORE
Place these capacitors on L8 (North side,Secondary Layer)
C11 C12 C13 C14 C15 C16 C17 C18 — 10U_0805_6.3V6M

+CPU_CORE
Place these capacitors on L8 (North side,Secondary Layer)
C19 C20 C21 C22 C23 C24 C25 C26 — 10U_0805_6.3V6M

+CPU_CORE
Place these capacitors on L8 (Sorth side,Secondary Layer)
C27 C28 C29 C30 C31 C32 C33 C34 — 10U_0805_6.3V6M

+CPU_CORE
Place these capacitors on L8 (Sorth side,Secondary Layer)
C35 C36 C37 C38 C39 C40 C41 C42 — 10U_0805_6.3V6M

Mid Frequence Decoupling

+1.05VS
Place these inside socket cavity on L8 (North side Secondary)
C44 C45 C46 C47 C48 C49 — 0.1U_0402_10V6K

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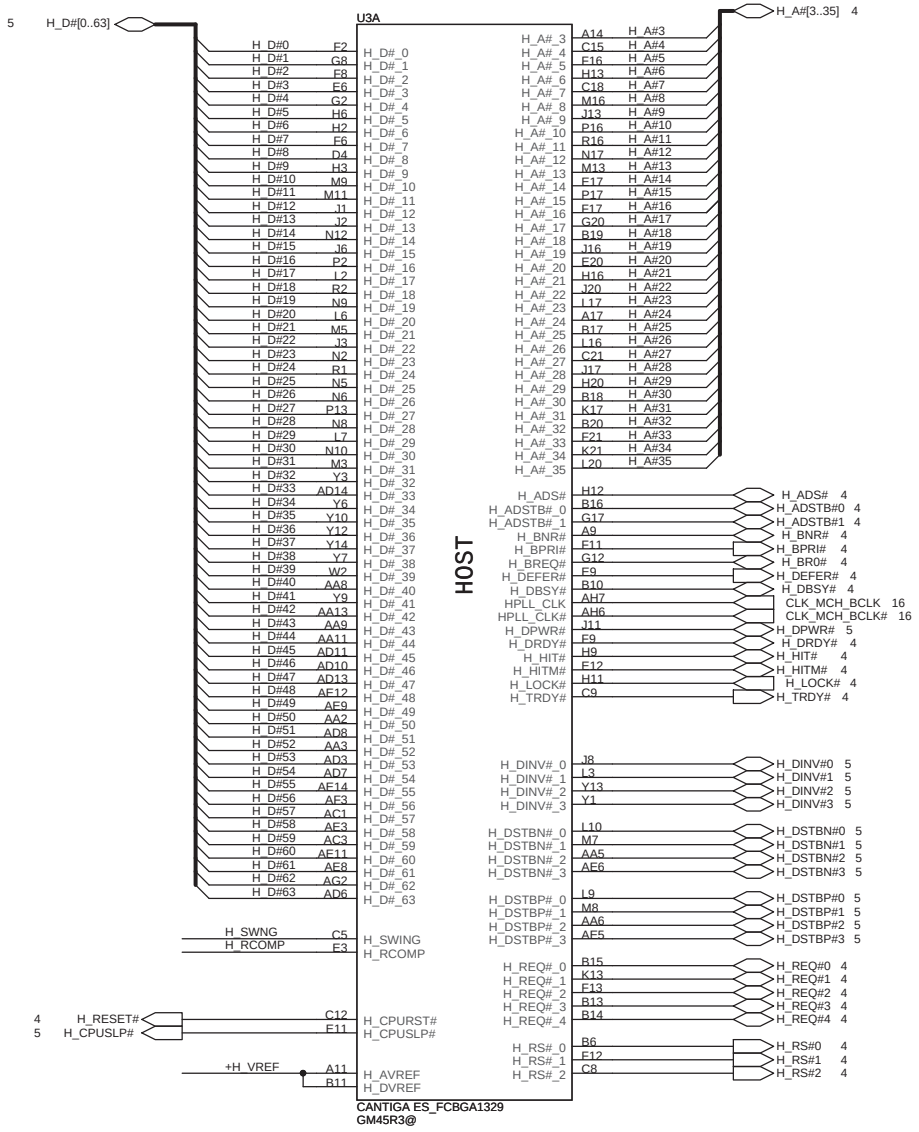
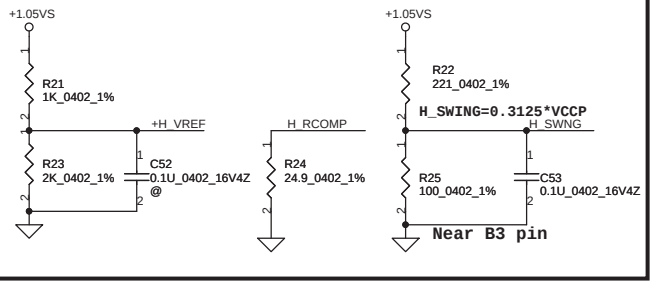


Layout Note:
H_RCOMP / +H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB



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Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled 1 = Digital display (iHDMI/DP) interface enabled *(Default)

Use VGATE for GMCH_PWROK

23,33,43 VGATE — R58 @0_0402_5% — GMCH_PWROK

23,33 ICH_PWROK — R59 0_0402_5%

Please place these resistors close to related balls

Lane reversal

the strap pin will impact no IHDMI SKU if mount R62

CANTIGA ES_FCBGA1329

GM45R3@

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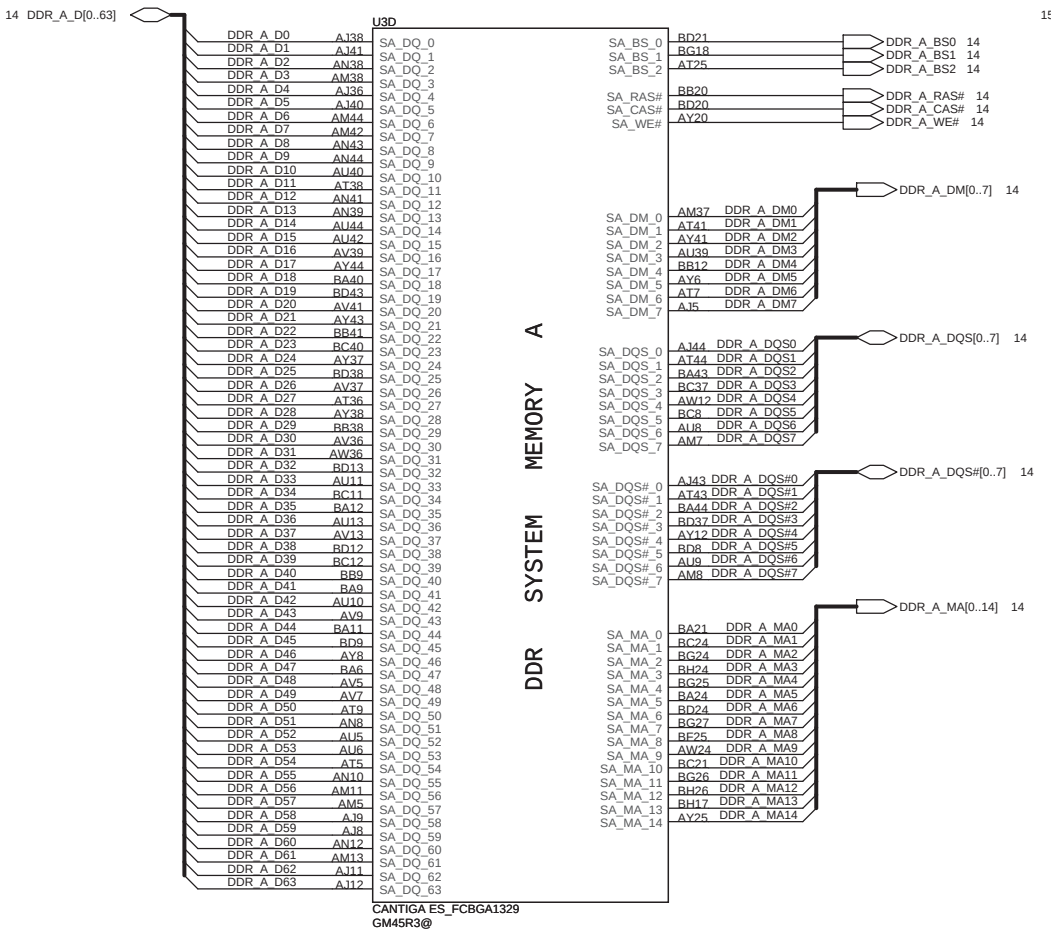

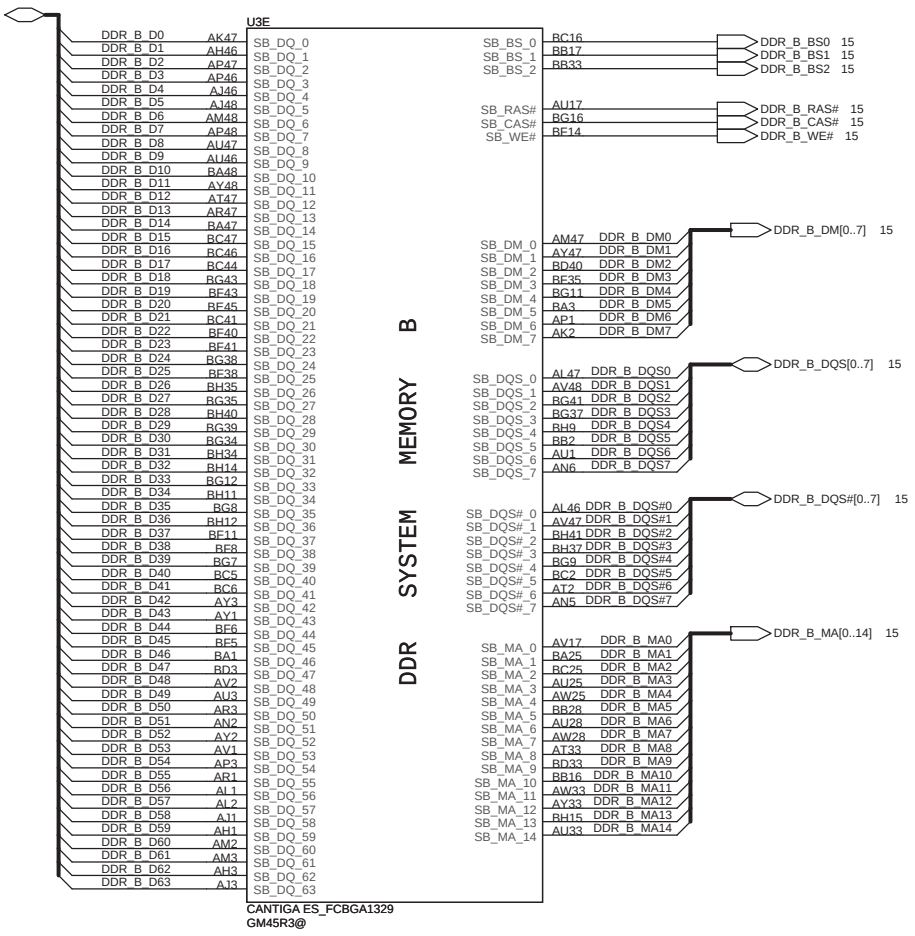

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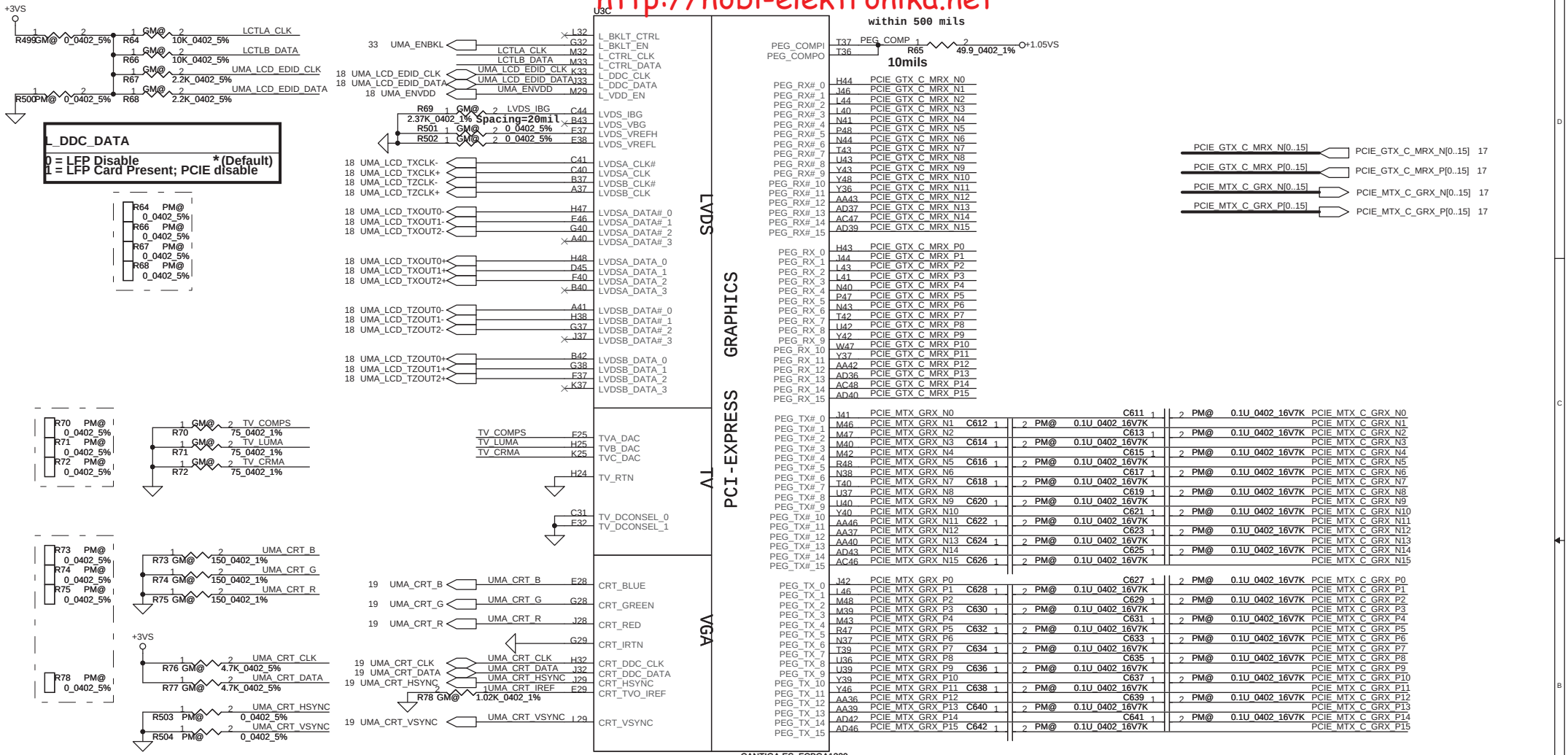

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DDR3,1066MHz,4140mA
DDR3,800MHz,3162.5mA

DDR PWR

VCC CORE (Core+IMEL+HSIO)
W/Ext GFX: 3060mA
W/Int GFX: 2400mA

NB Core,Intel Management Engine Link

Intel: VCC -- 220U*2, ESR 12mOhm

9600mA

For layout placement un-mound C123 and mound C84

Int. Graphic

Intel:AXG and AXG_NCTF -- 220U*2, ESR 15mOhm

For layout issue to separate 220u*1 to +1.05VS

CANTIGA ES_FCBGA1329
GM45R3@

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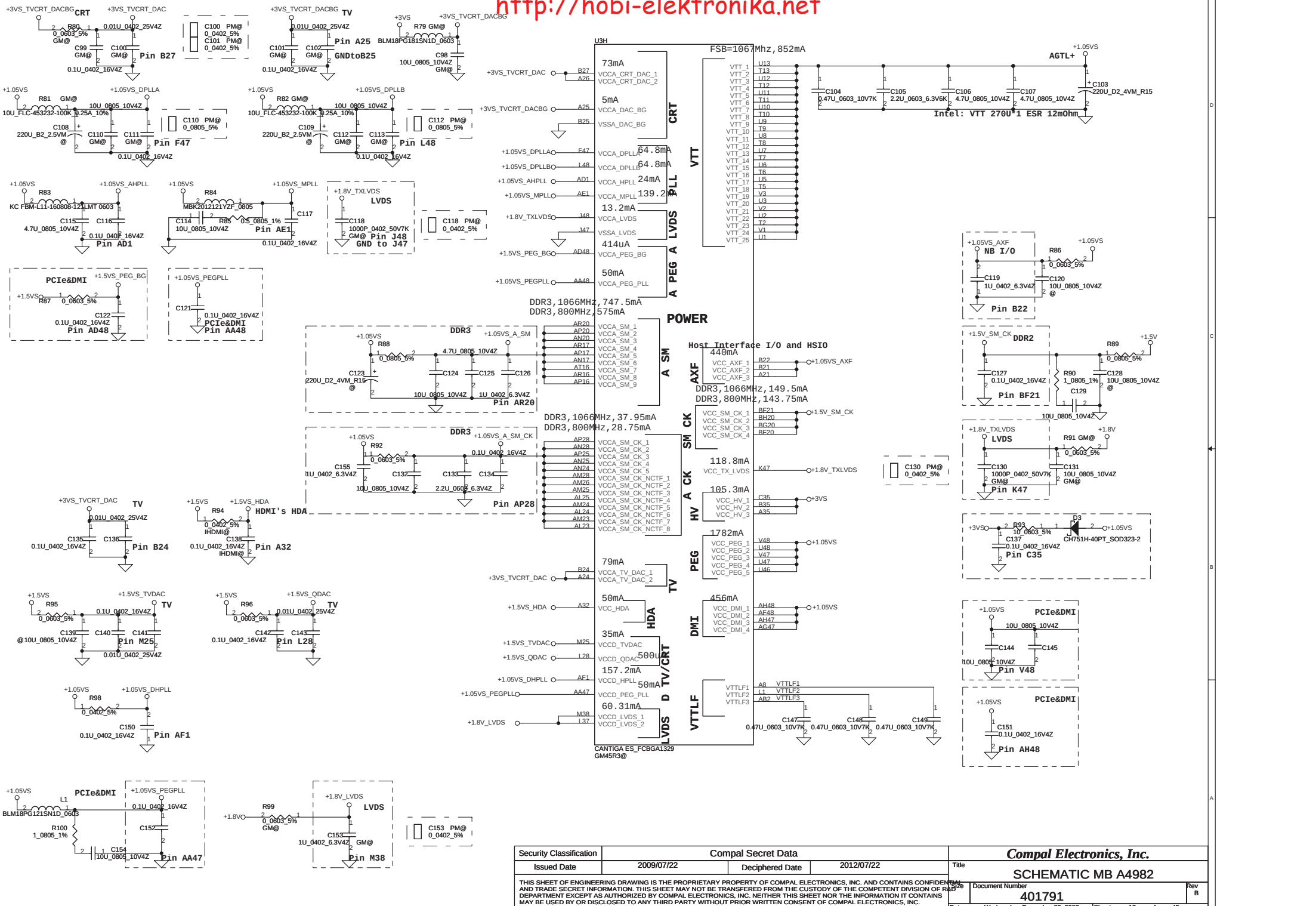

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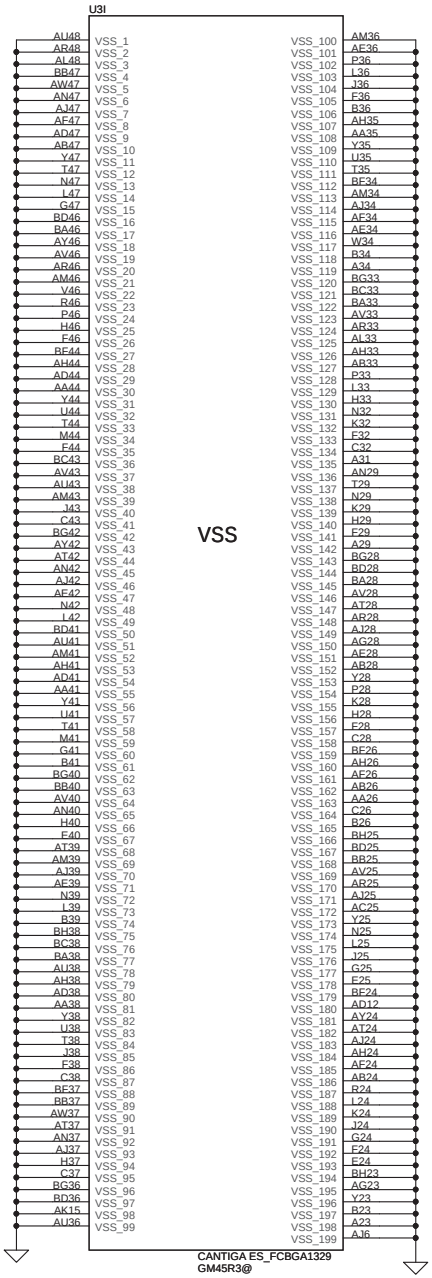

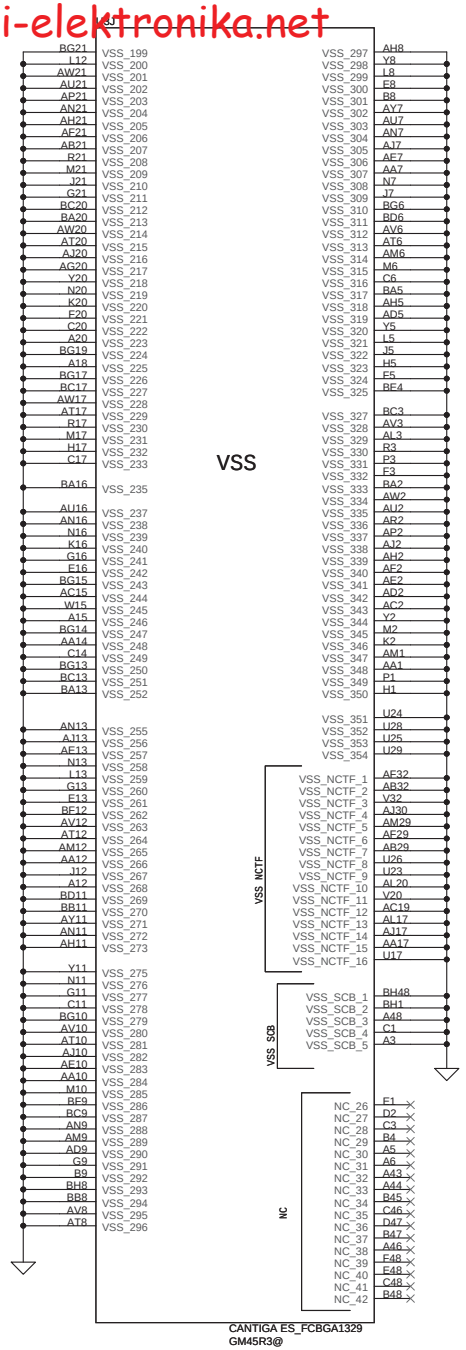

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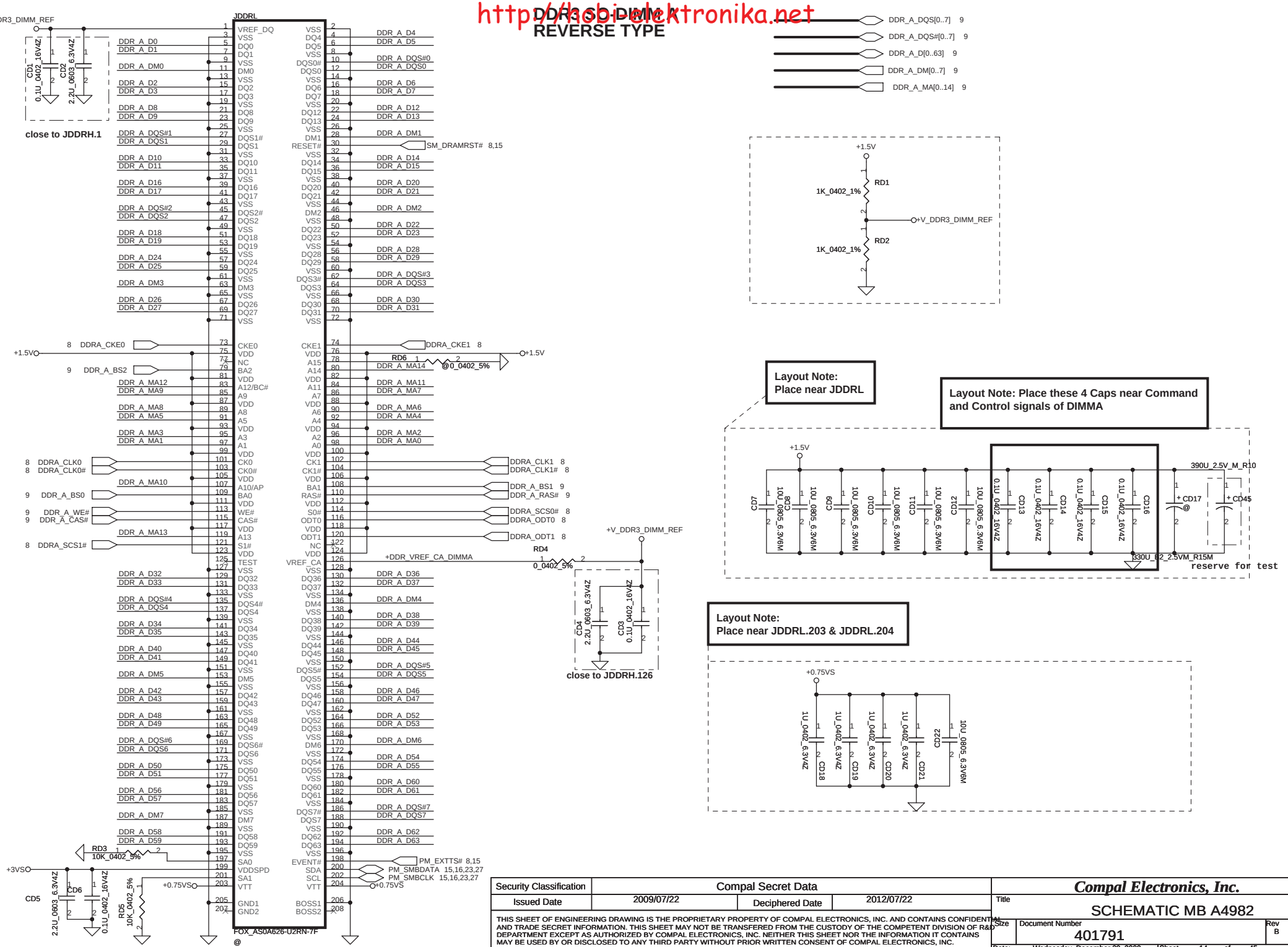
DDR3 SO-DIMM X REVERSE TYPE



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DDR3 SO-DIMM 3
REVERSE TYPE

DDR_B_DQS[0..7] 9
DDR_B_DQS#[0..7] 9
DDR_B_D[0..63] 9
DDR_B_DM[0..7] 9
DDR_B_MA[0..14] 9

+V_DDR3_DIMM_REF

JDDRH

close to JDDRL.1

+1.5V

RD10 1 2 DDR_B_MA14 @0_0402_5%

RD7 1 2 0_0402_5%

+DDR_VREF_CA_DIMMB

close to JDDRL.126

RD8 1 2 10K_0402_5%

RD9 1 2 10K_0402_5%

+3VS

+0.75VS

FOX_AS0A626-UARN-7F
@

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 & JDDRH.204

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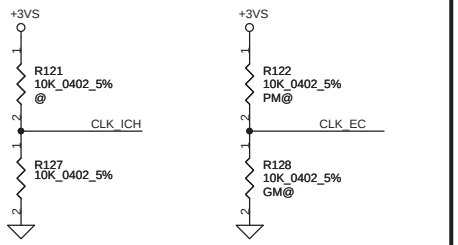
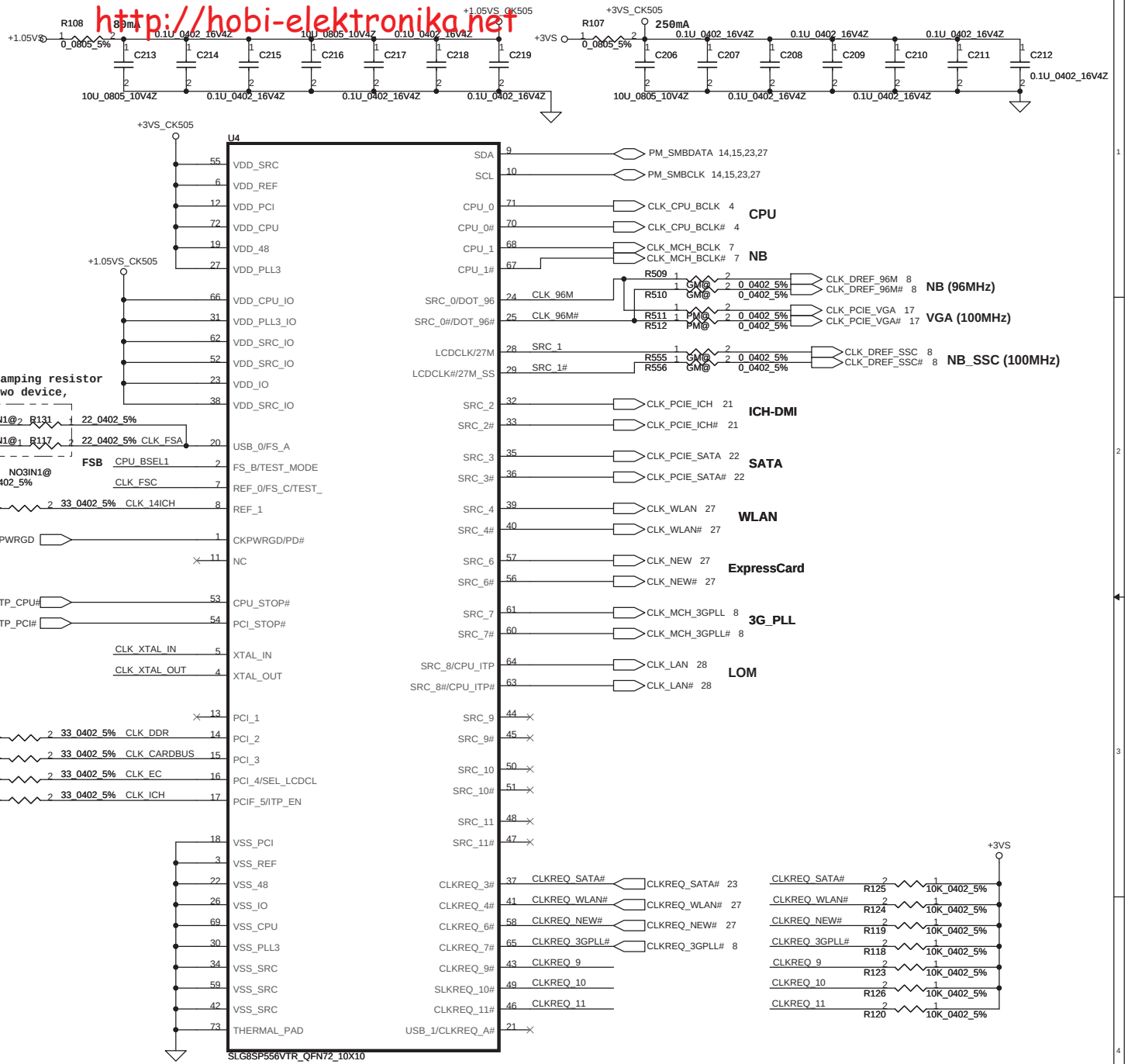
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)





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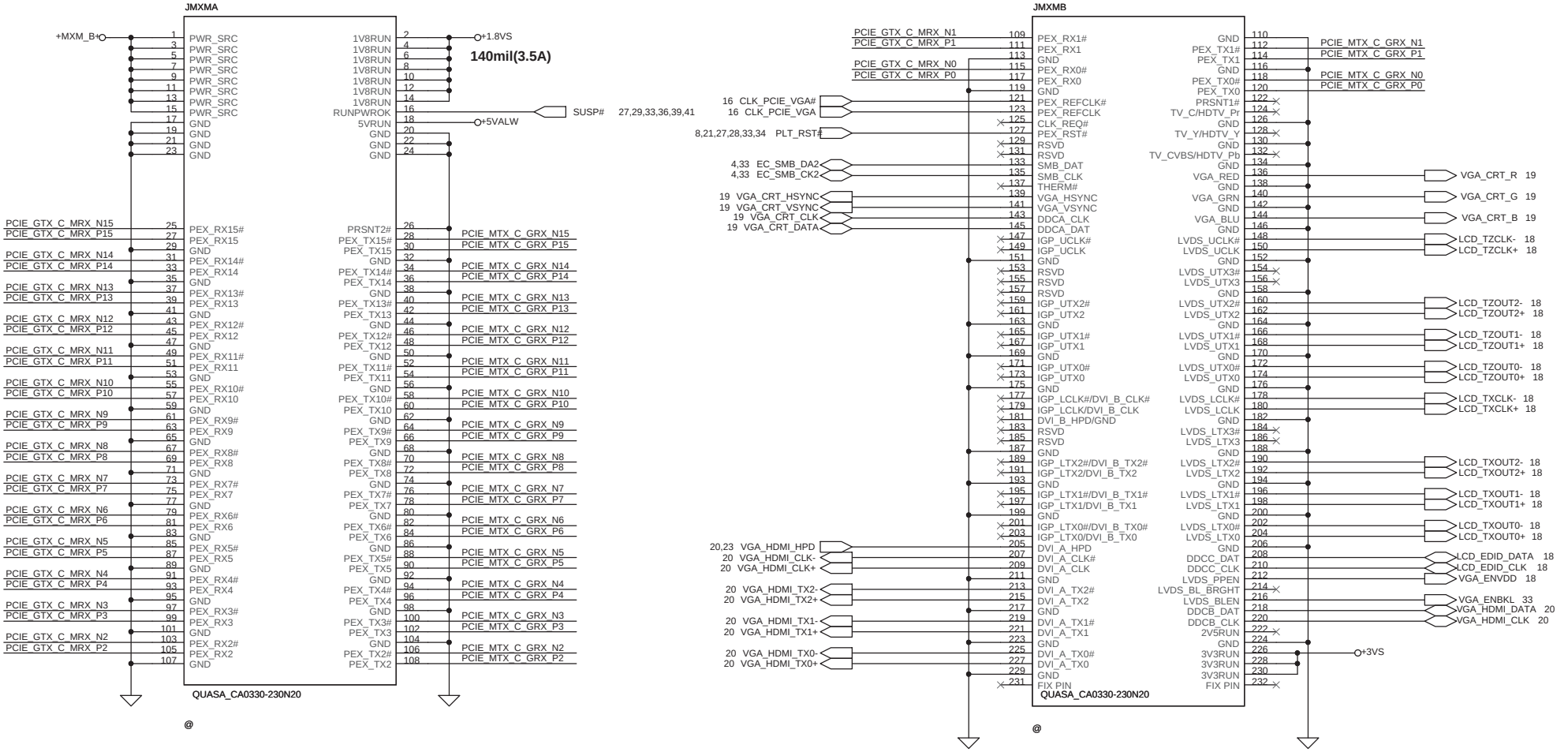
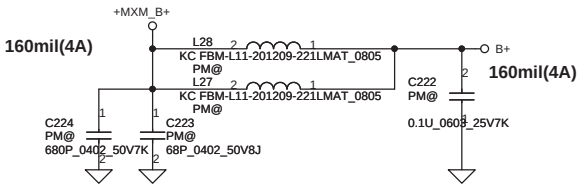
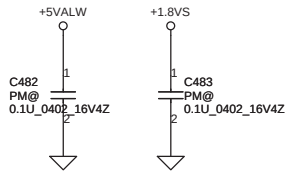
10 PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]
10 PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]







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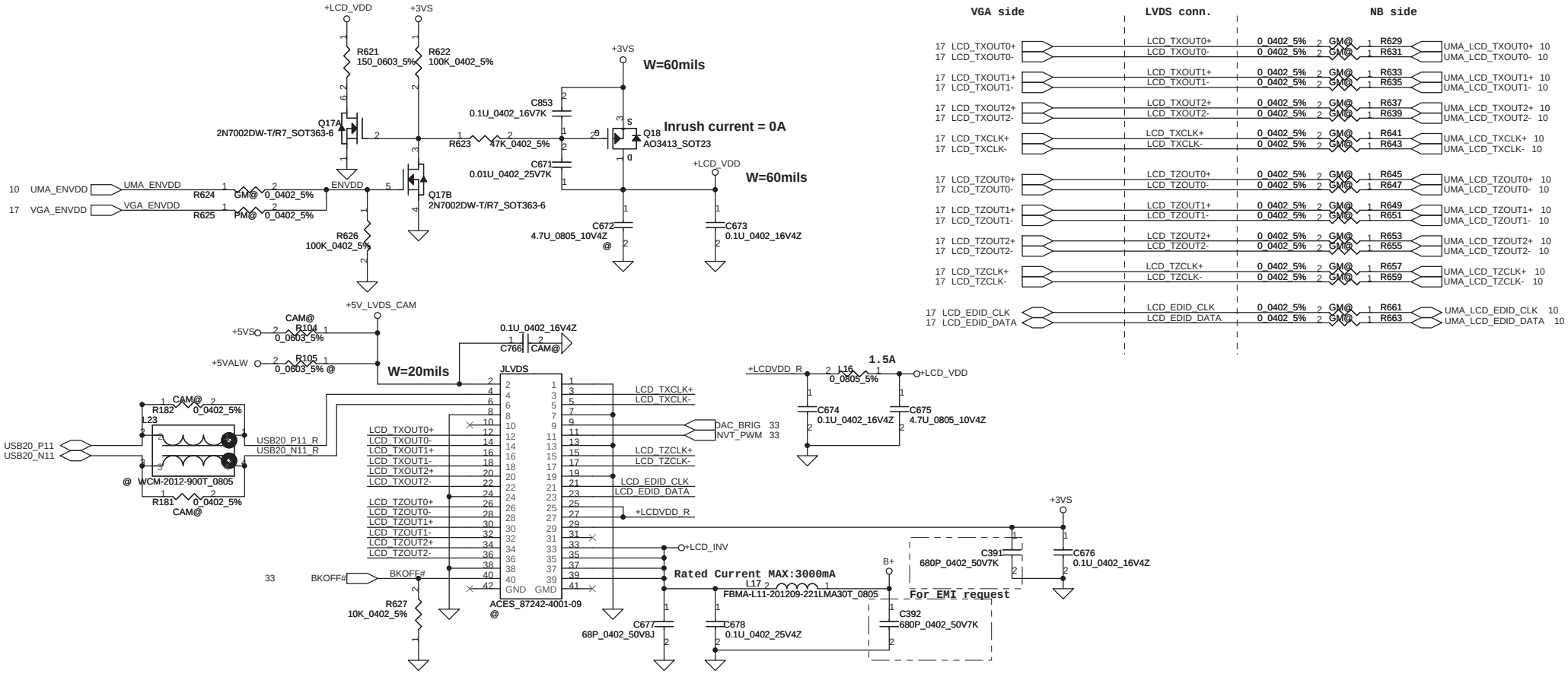
LCD/PANEL BD. Conn.

please link to VGA Conn. then link to LVDS Conn.



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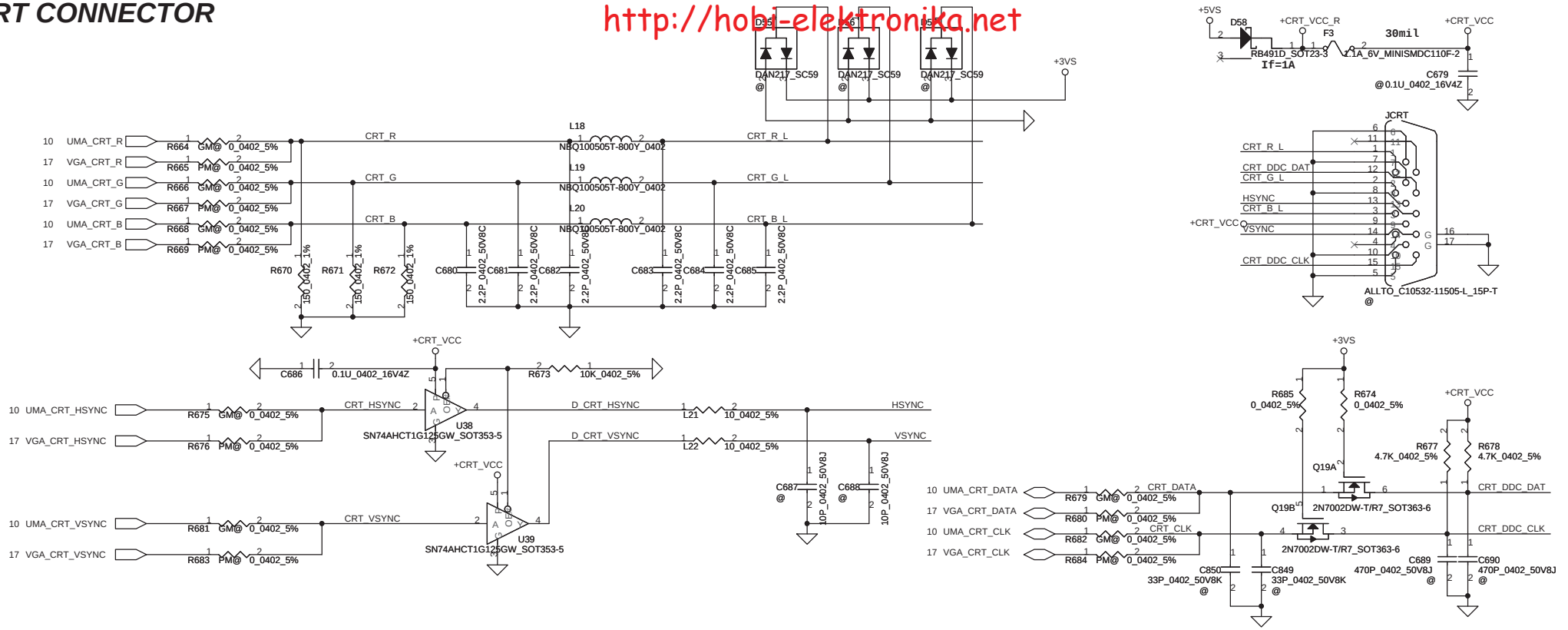
CRT CONNECTOR



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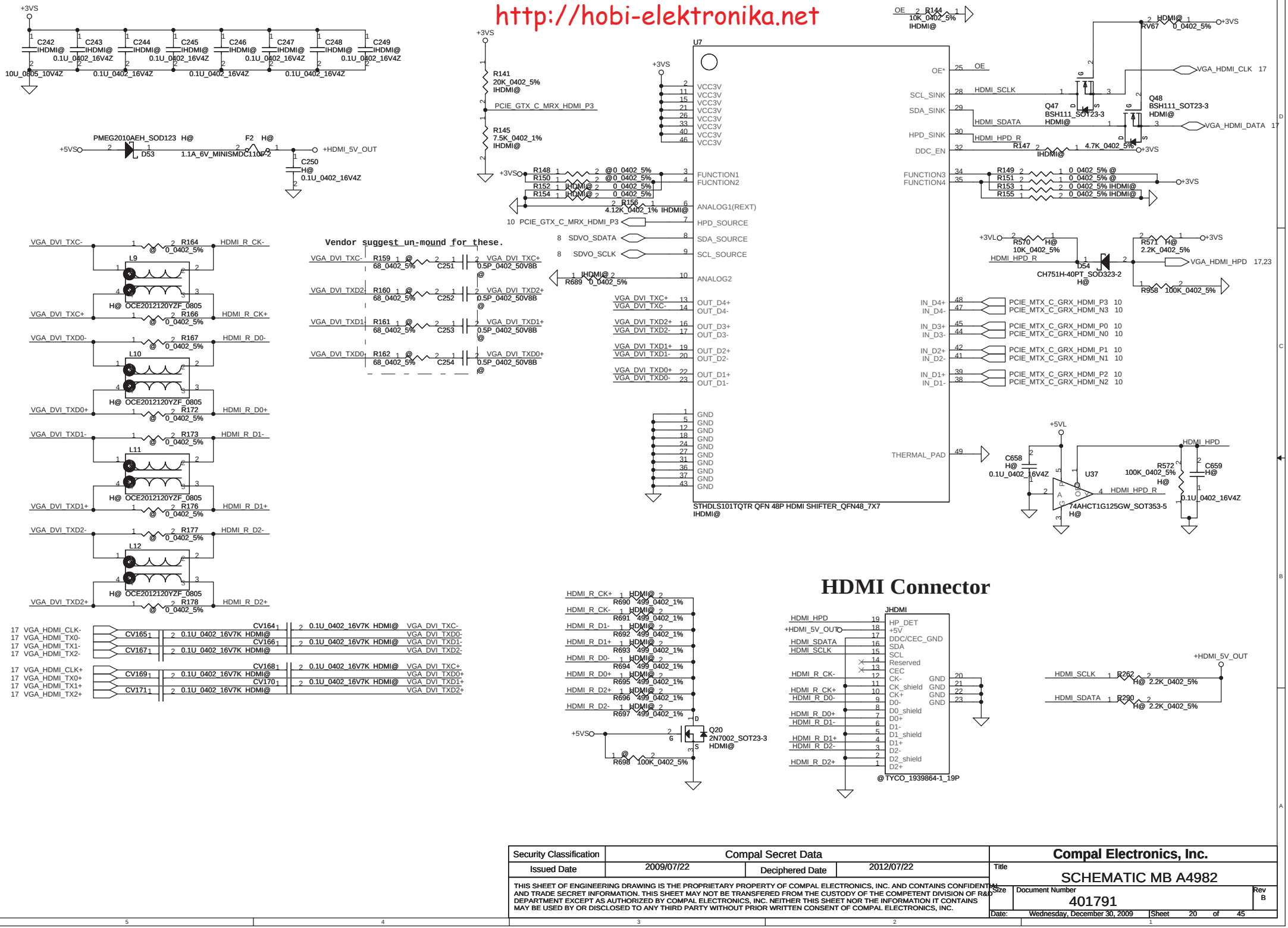

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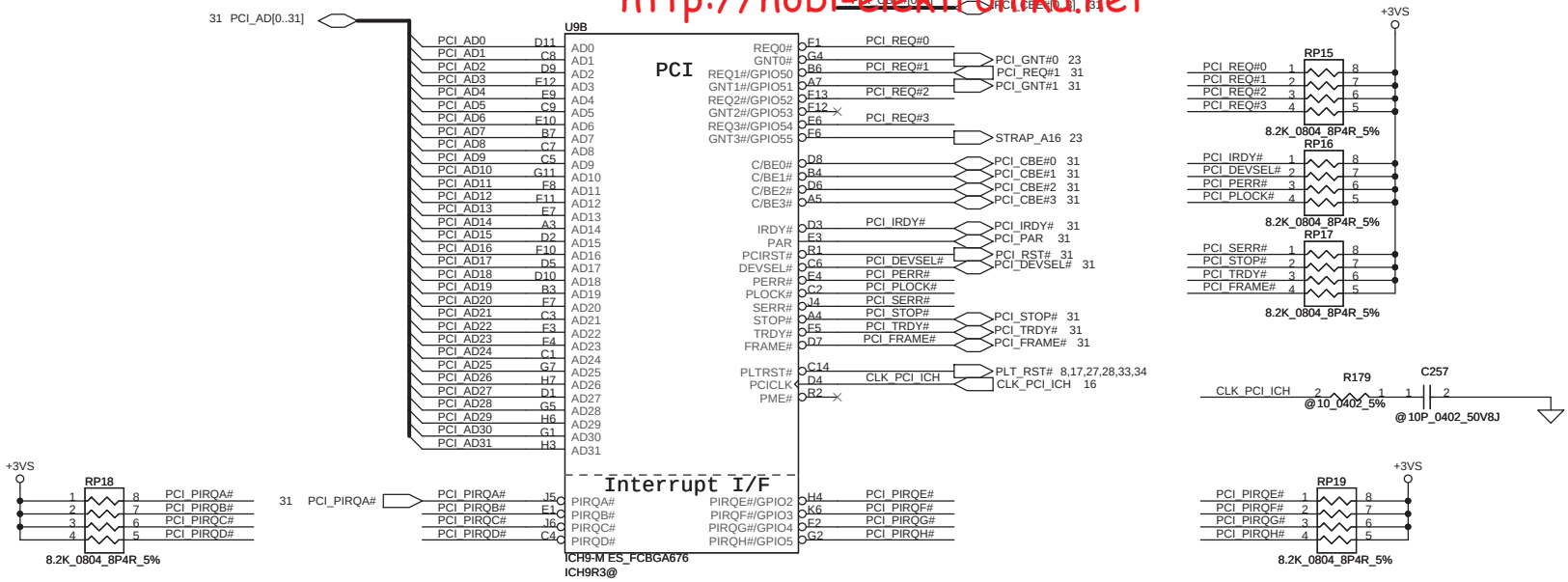

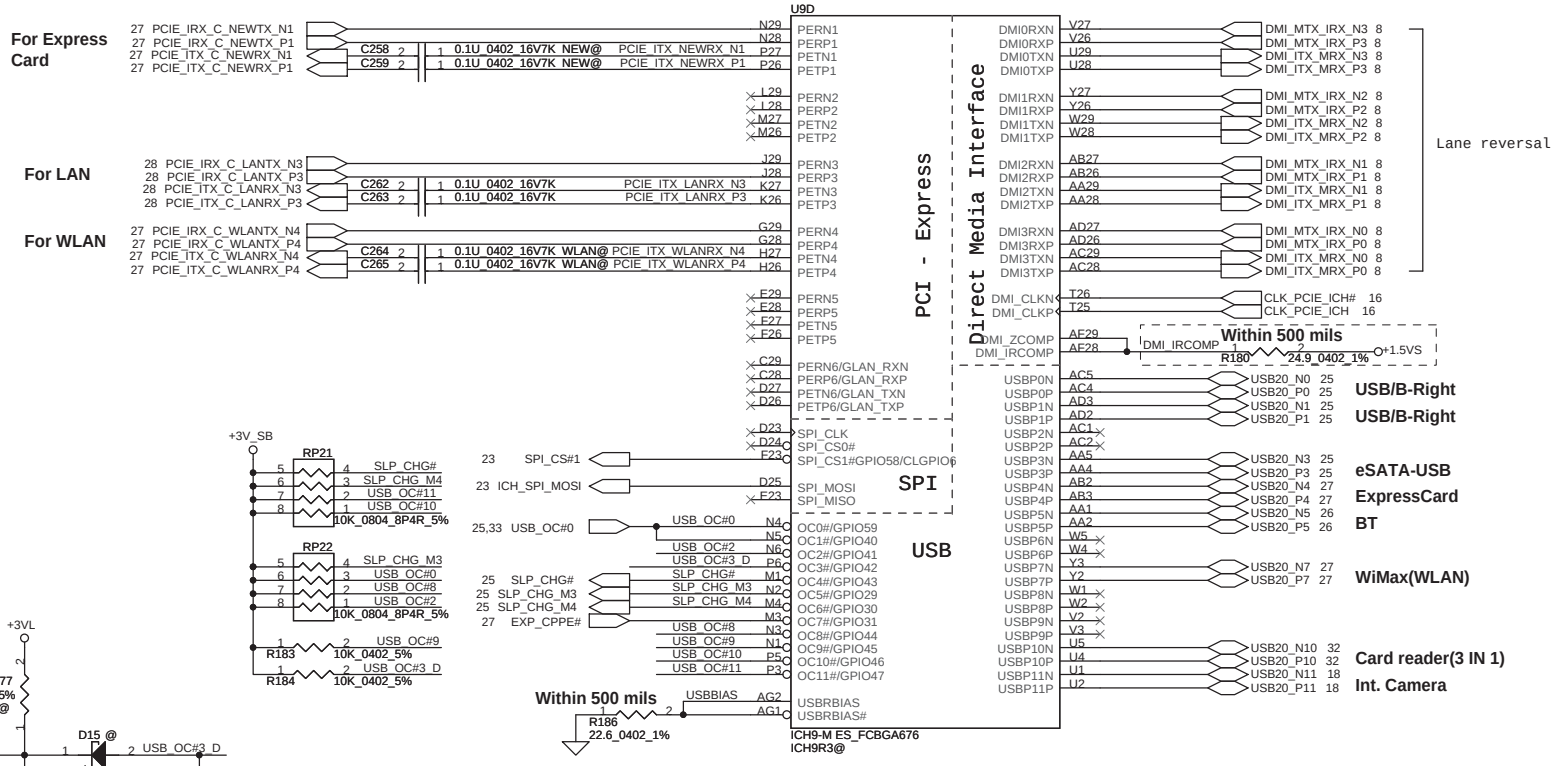

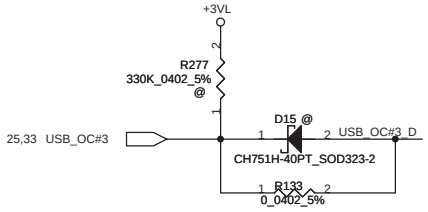

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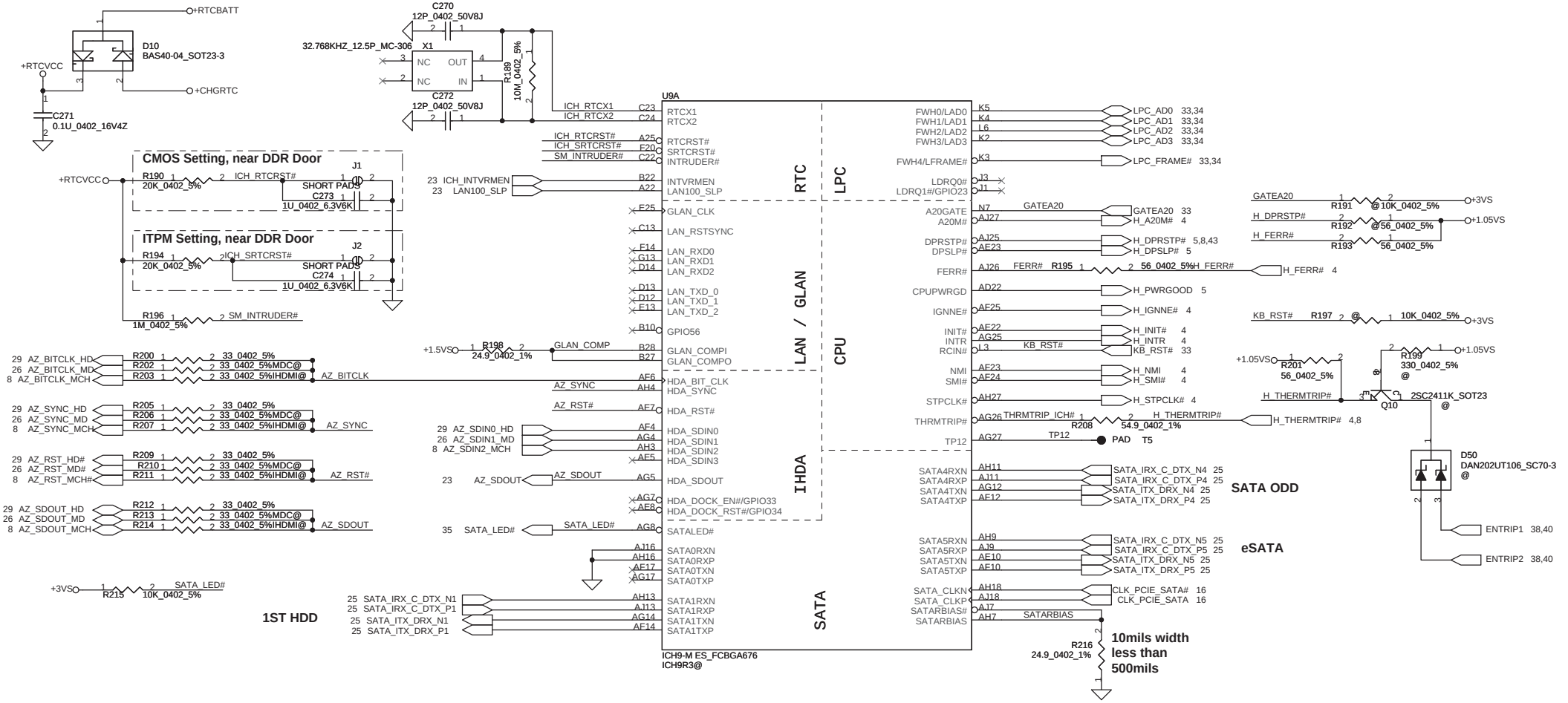

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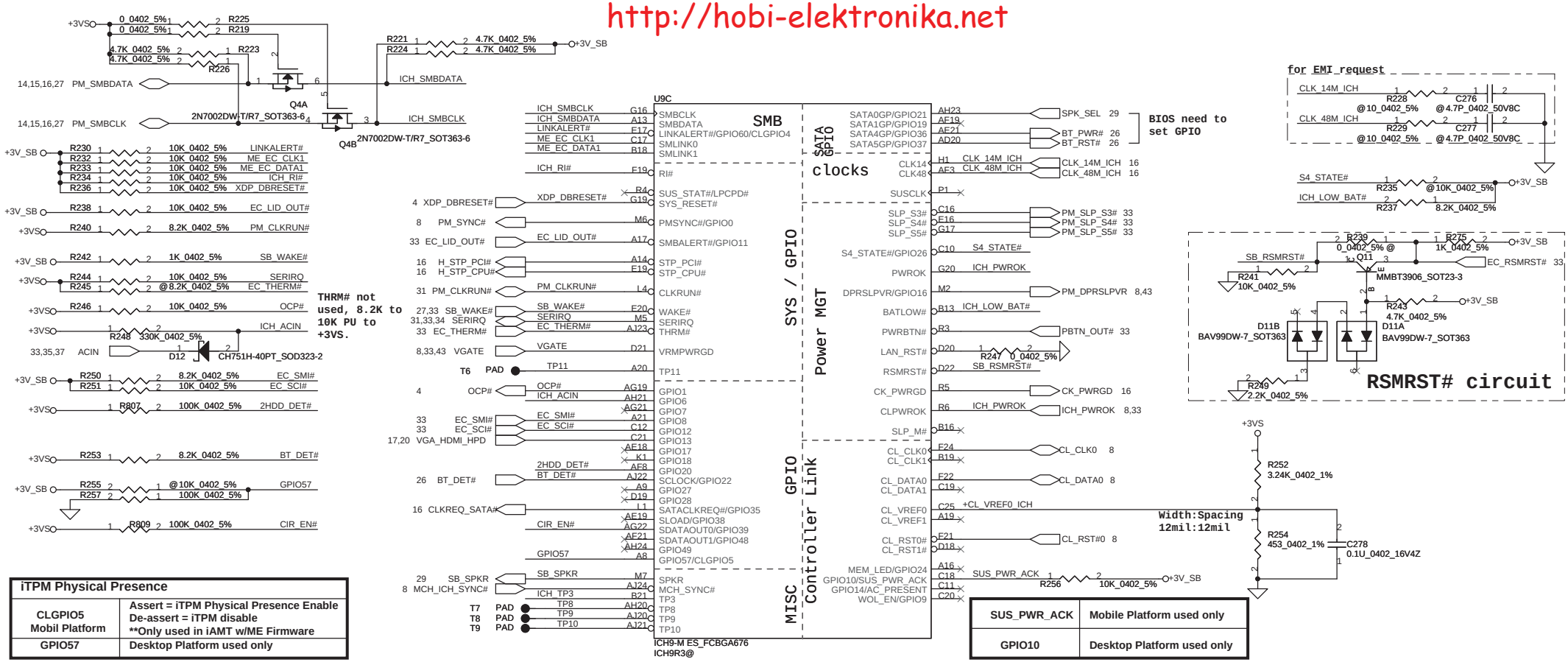
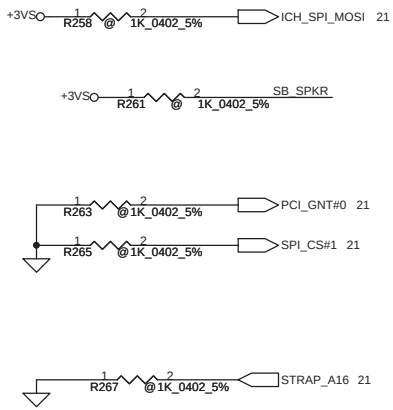


iTPM Physical Presence	
CLGPIO5 Mobil Platform	Assert = iTPM Physical Presence Enable De-assert = iTPM disable **Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin

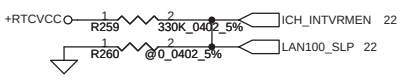


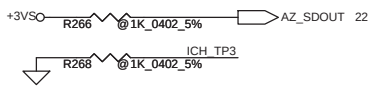
Internal TPM Strap(Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)





Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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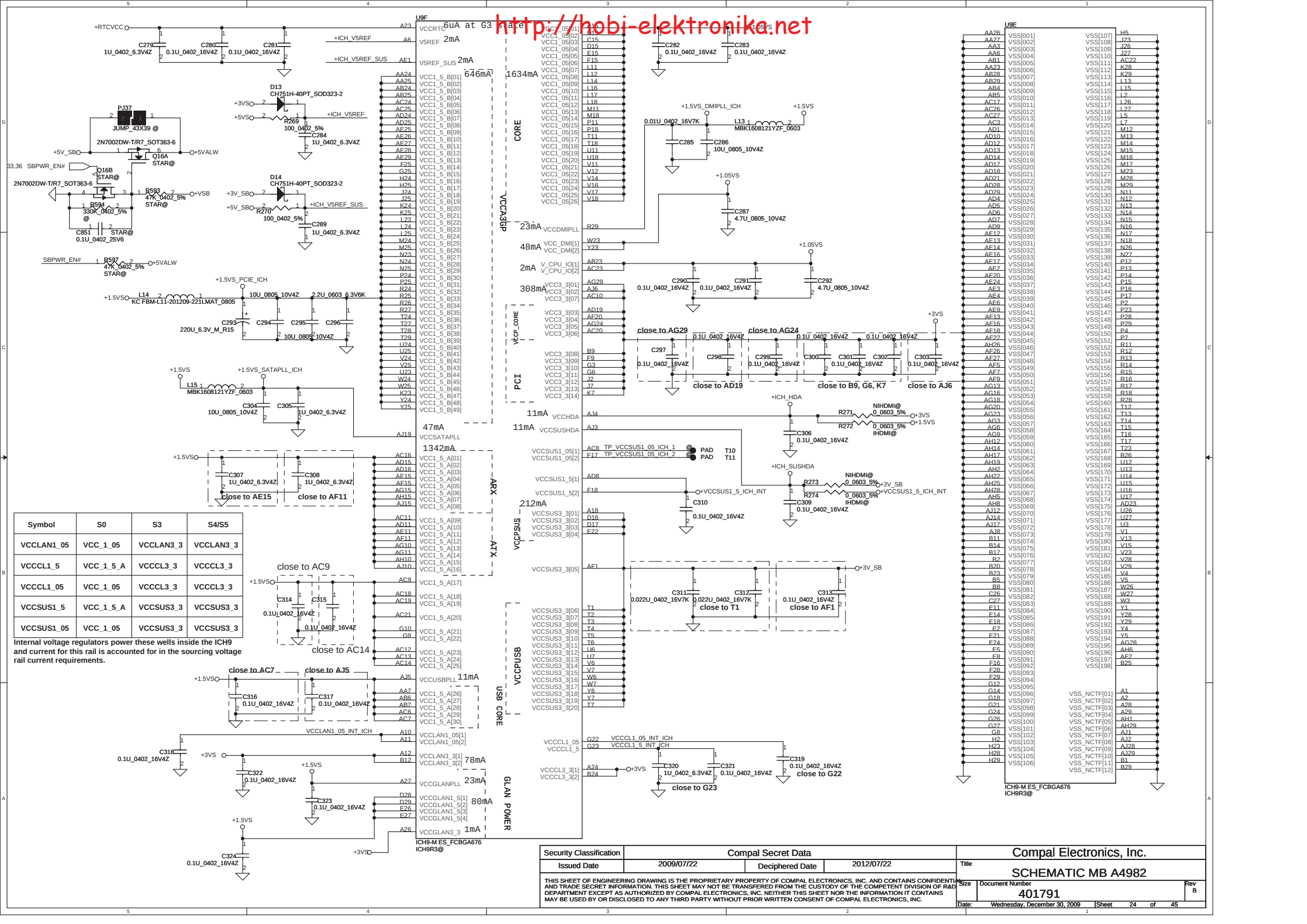

Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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SATA HDD Conn.

Place closely JP25 SATA CONN.

+5VS 1.2A

C697 10U_0805_10V4Z
C698 0.1U_0402_16V4Z
C699 0.1U_0402_16V4Z
C700 0.1U_0402_16V4Z

JHDD

GND A+ A- GND B- B+ GND V33 V33 V33 GND GND GND V5 V5 V5 GND Reserved GND V12 V12 V12 GND GND

SATA_ITX_C_DRX_P1 C713 0.01U_0402_25V7K SATA_ITX_DRX_P1 22
SATA_ITX_C_DRX_N1 C715 0.01U_0402_25V7K SATA_ITX_DRX_N1 22
SATA_IRX_DTX_N1 C717 0.01U_0402_25V7K SATA_IRX_C_DTX_N1 22
SATA_IRX_DTX_P1 C719 0.01U_0402_25V7K SATA_IRX_C_DTX_P1 22

+3VS
+5VS

SANTA_19A202-1_22P
@
this is temp. footprint

SATA ODD Conn.

Place component's closely ODD CONN.

+5VS 1.1A

C721 10U_0805_10V4Z
C722 10U_0805_10V4Z
C723 @ 1U_0402_6.3V4Z
C724 0.1U_0402_16V4Z
C725 0.1U_0402_16V4Z

for 16" use

JODD

GND A+ A- GND B- B+ GND DP +5V +5V MD GND GND

SATA_ITX_C_DRX_P4_ODD
SATA_ITX_C_DRX_N4_ODD
SATA_IRX_DTX_N4_ODD
SATA_IRX_DTX_P4_ODD
+5VS

SANTA_206401-1_RV
@

for 17" expansion using

JODDB

SATA_IRX_DTX_P4
SATA_IRX_DTX_N4
SATA_ITX_C_DRX_N4
SATA_ITX_C_DRX_P4

E&T_6905-E12N-00R
@

SATA_ITX_C_DRX_P4_ODD C733 16@ 0.01U_0402_25V7K
SATA_ITX_C_DRX_N4_ODD C734 16@ 0.01U_0402_25V7K
SATA_IRX_DTX_N4_ODD C735 16@ 0.01U_0402_25V7K
SATA_IRX_DTX_P4_ODD C736 16@ 0.01U_0402_25V7K
SATA_IRX_DTX_P4 C732 17@ 0.01U_0402_25V7K SATA_IRX_C_DTX_P4 22
SATA_IRX_DTX_N4 C731 17@ 0.01U_0402_25V7K SATA_IRX_C_DTX_N4 22
SATA_ITX_C_DRX_N4 C730 17@ 0.01U_0402_25V7K SATA_ITX_DRX_N4 22
SATA_ITX_C_DRX_P4 C729 17@ 0.01U_0402_25V7K SATA_ITX_DRX_P4 22

USB Board

W=60mils

+5VALW 1.4A +USB_VCCA

U42 GND IN IN EN# OUT OUT OUT FLG G528_SO8

For_EMI_request
C693 1000P_0402_50V7K
33 USB_EN#
USB_OC#0 21,33
C752 4.7U_0805_10V4Z @

W=60mils +USB_VCCA

JUSBB

21 USB20_N0
21 USB20_P0
21 USB20_N1
21 USB20_P1

E&T_6905-E12N-00R
@

eSATA/USB

+USB_VCCB +USB_VCCB

R949 75K_0402_1% @
R952 43K_0402_1% @
USB20_P3_S_O
USB20_N3_S_O
R951 51K_0402_1% @
R950 51K_0402_1% @

USB20_P3 R130 0_0402_5% USB20_P3_R
USB20_N3 R132 0_0402_5% USB20_N3_R

mount the two resistor
when un-mount USB sleep$charge function

please close to SB under 30mm

+3VALW

U52 1D+ 1D- 2D+ 2D- GND VCC S D+ D- OE#

21 USB20_P3
21 USB20_N3
USB20_P3_S
USB20_N3_S
USB20_P3_R
USB20_N3_R
C353 0.1U_0402_16V4Z @
SLP_CHG# 21

TS3USB221RSER_QFN10_2x1P5~D
@

S	OE#	function
X	H	disconnect
L	L	D=1D
H	L	D=2D

U53 1OE# 2OE# 3OE# 4OE# 1A 2A 3A 4A 1B 2B 3B 4B VCC GND

21 SLP_CHG_M3
21 SLP_CHG_M4
USB20_P3_S
USB20_N3_S
USB20_P3_S_O
USB20_N3_S_O
R114 100_0402_5% @
+USB_VCCB
C354 0.1U_0402_16V4Z @

SN74CBT3125PWRG4_TSSOP14
@

OE#	function
H	A port= B port
L	disconnect

W=60mils

+5VALW 1.4A +USB_VCCB

U40 GND IN IN EN# OUT OUT OUT FLG G528_SO8

33 USB_CHG_EN#
USB_OC#3 21,33
C692 1000P_0402_50V7K
For EMI request
C743 4.7U_0805_10V4Z @

D62 @
PJDLC05_SOT23-3

USB_N3_R
USB_P3_R

+USB_VCCB W=60mils

220U_6.3V_M_R15
1000P_0402_50V7K
C84
C749
C750
0.1U_0402_16V4Z

eSATA/USB Conn

JESATA USB VBUS D- D+ GND ESATA A- B- B+ GND SHIELD

22 SATA_ITX_DRX_P5
22 SATA_ITX_DRX_N5
C739 0.01U_0402_25V7K SATA_ITX_C_DRX_P5
C740 0.01U_0402_25V7K SATA_ITX_C_DRX_N5
22 SATA_IRX_C_DTX_N5
22 SATA_IRX_C_DTX_P5
C742 0.01U_0402_25V7K SATA_IRX_DTX_N5
C744 0.01U_0402_25V7K SATA_IRX_DTX_P5

FOX_3Q318111
@

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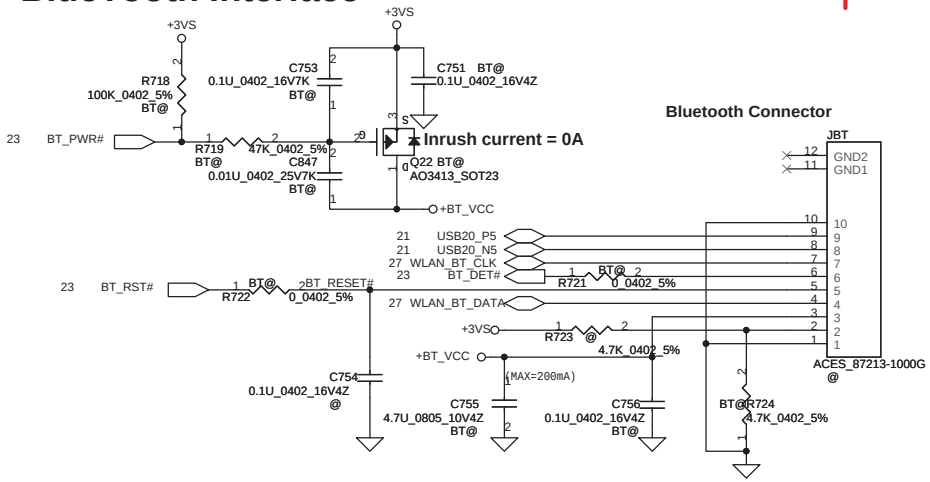
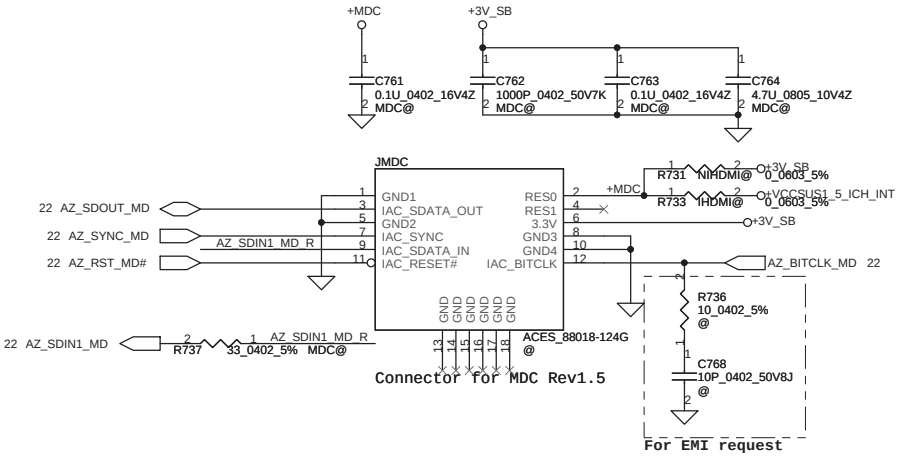
BlueTooth Interface

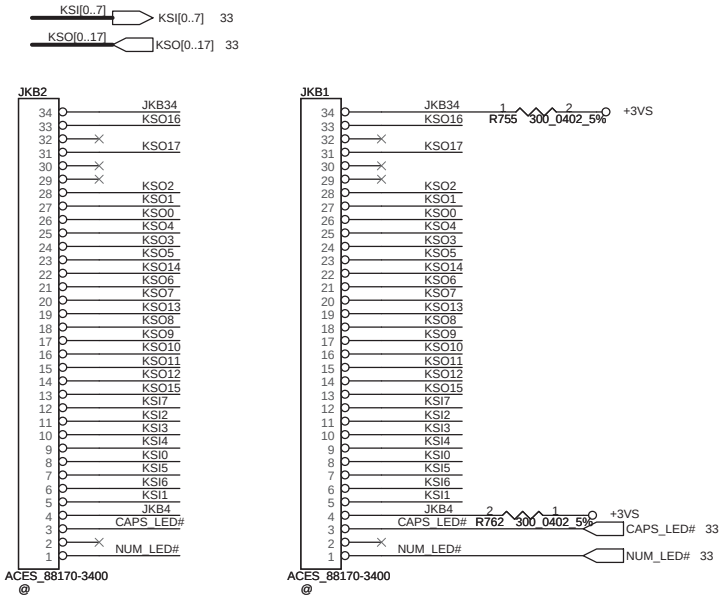


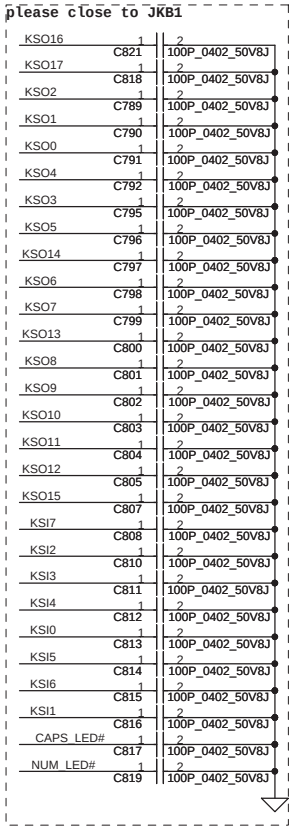
MDC 1.5 Conn.



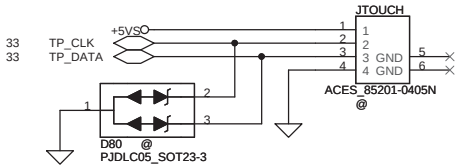
KEYBOARD CONN. for 17"

KEYBOARD CONN. for 16"

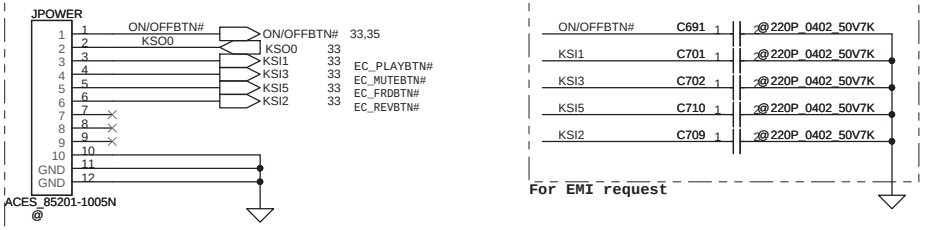




Touch/B Connector



SW/B Connector



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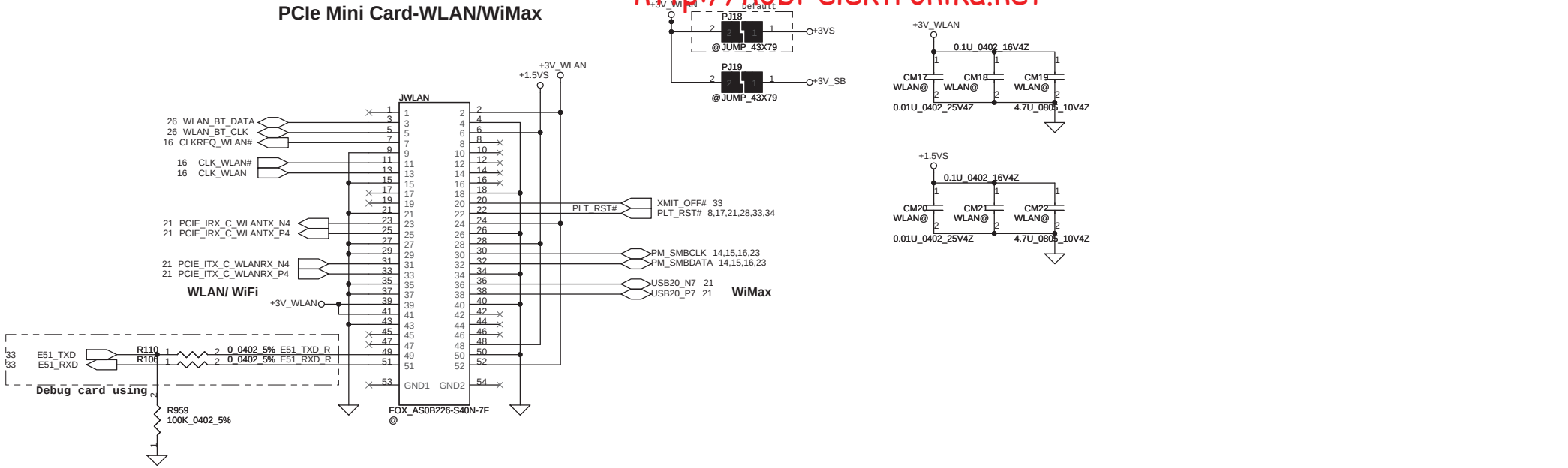
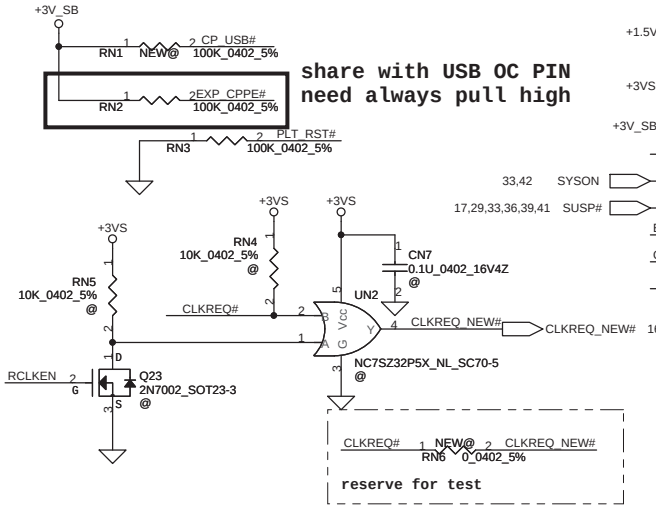
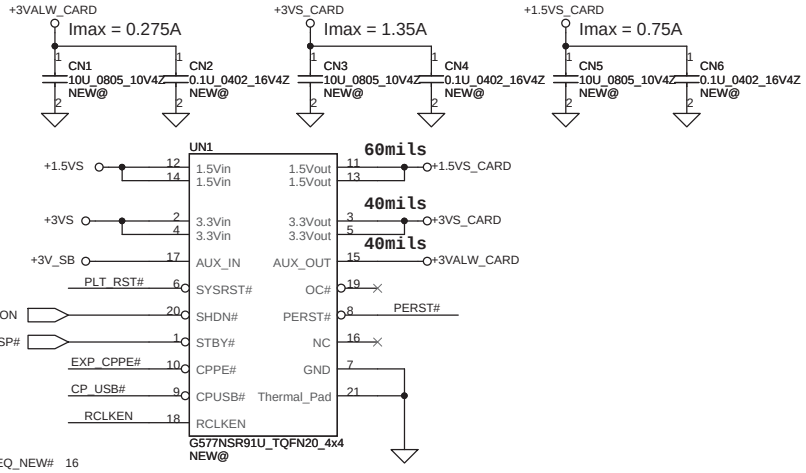
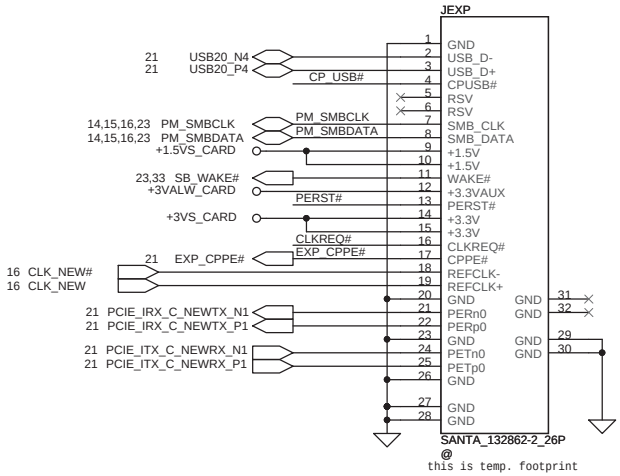
PCIe Mini Card-WLAN/WiMax









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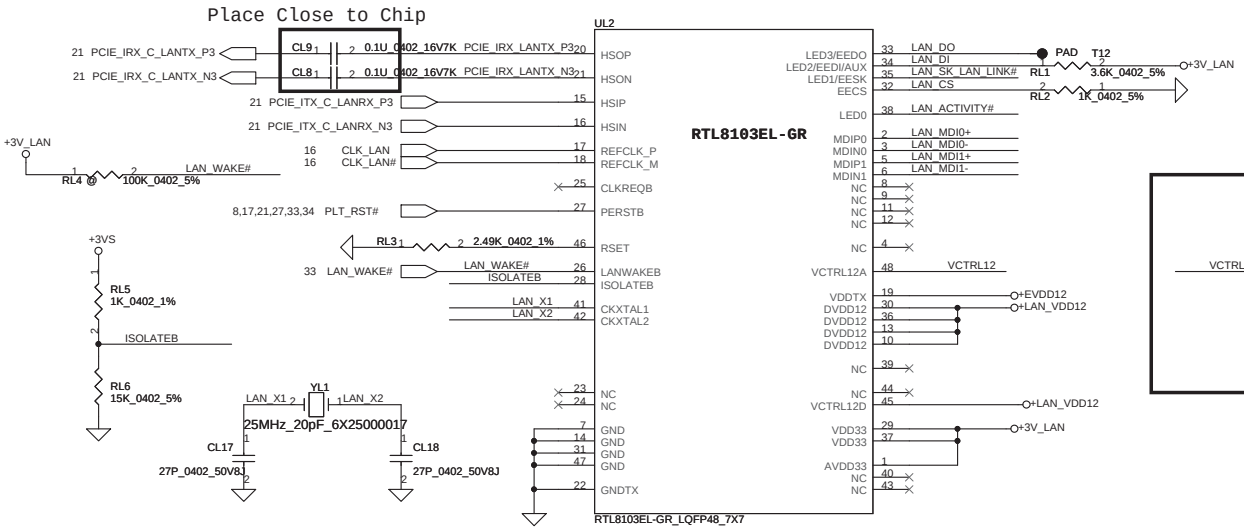

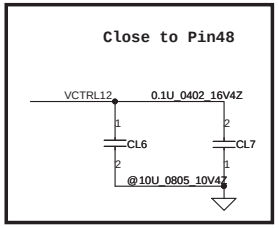

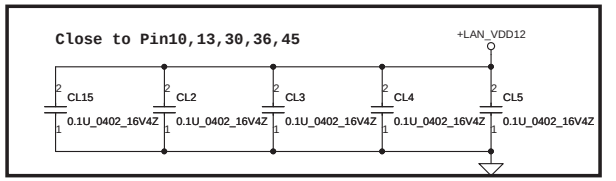

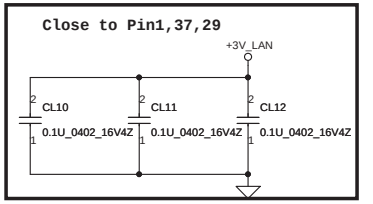

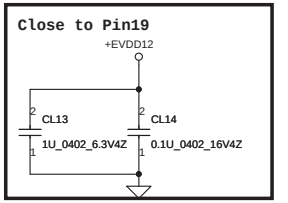

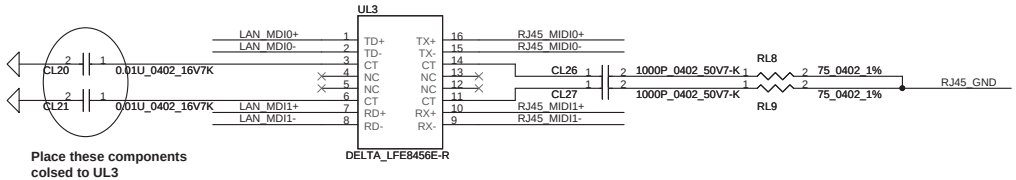

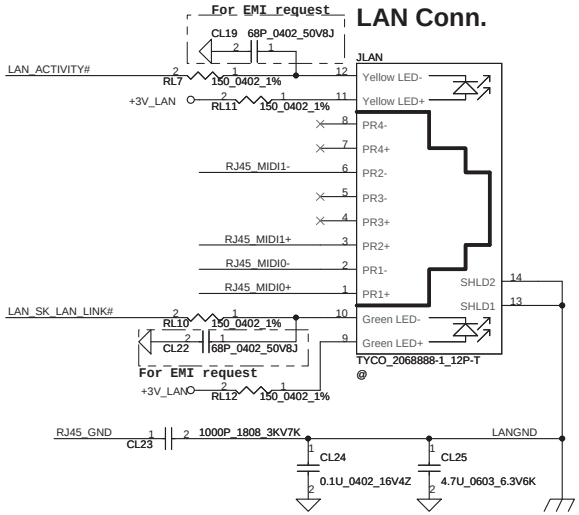

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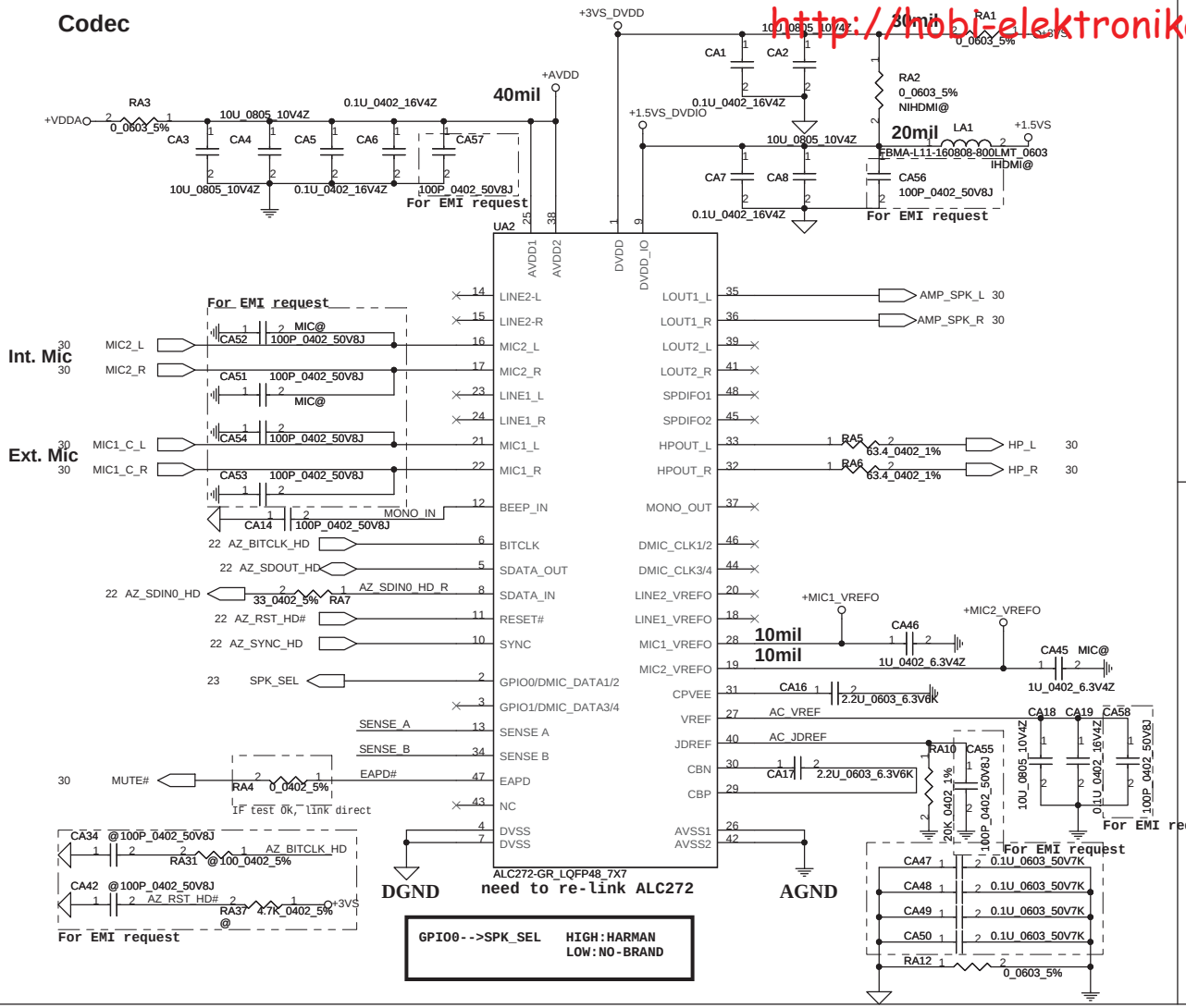
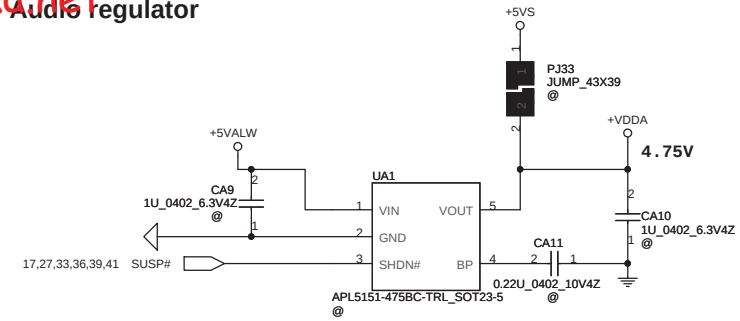
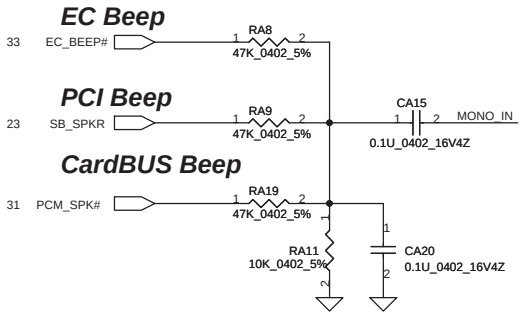
Codec



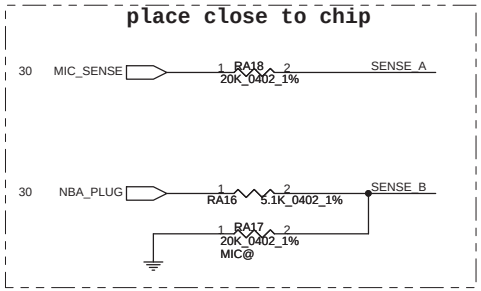
Audio regulator



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



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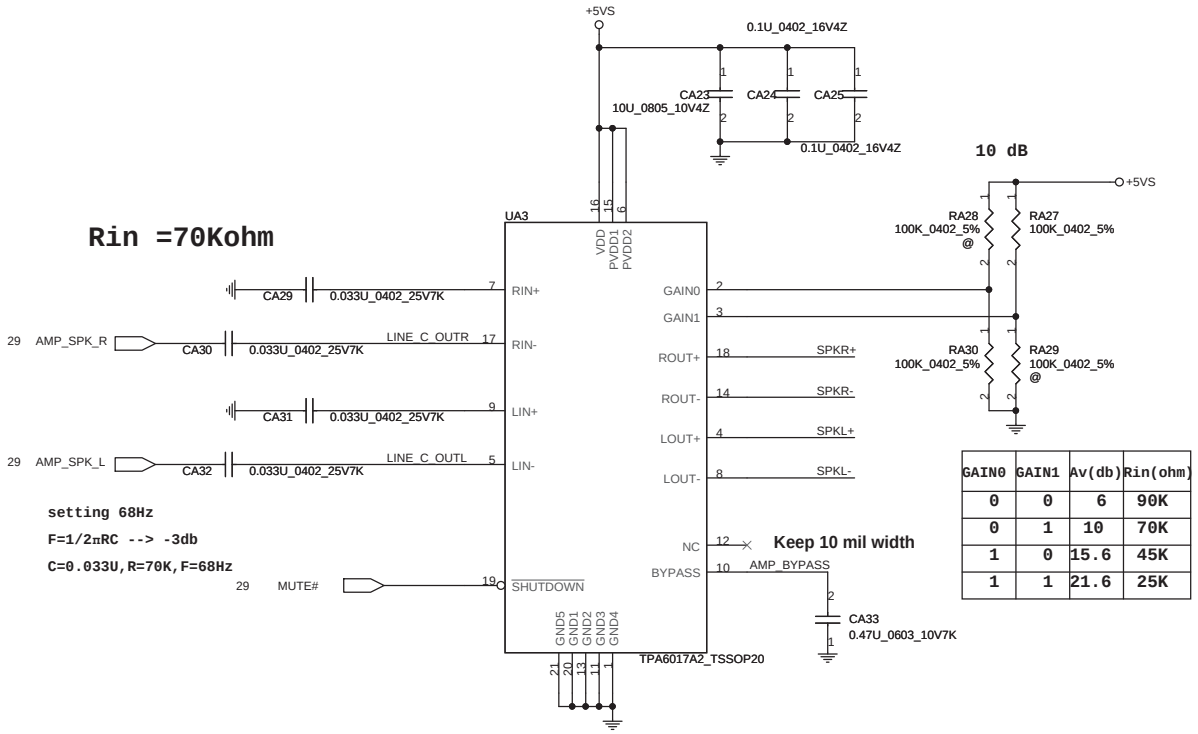
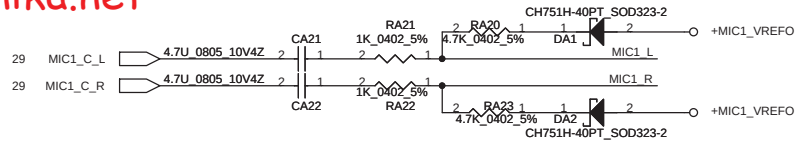
TPA6017 Medium Range Amplifier

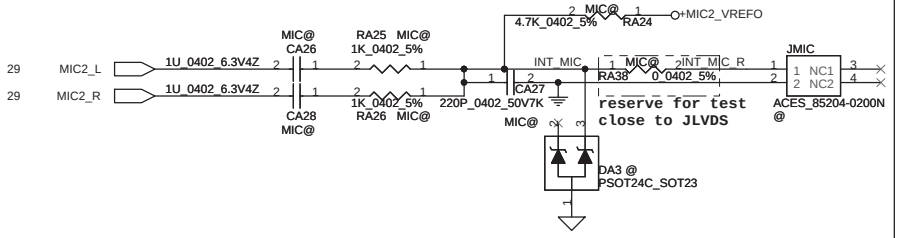


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

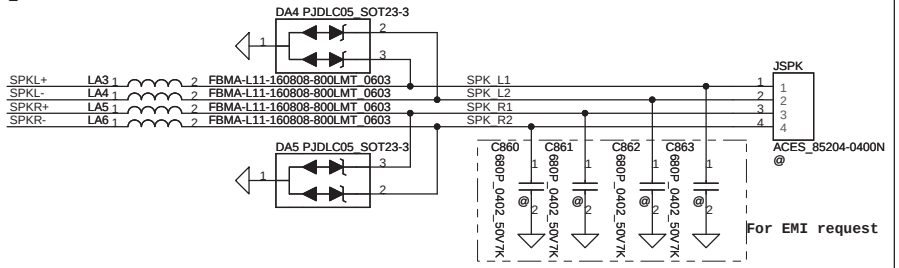
Ext. Mic



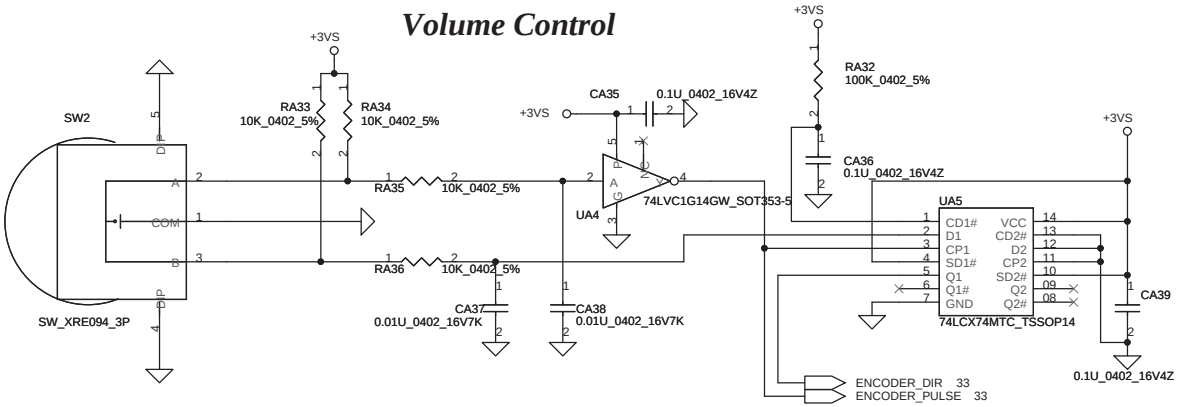
Int. Mic



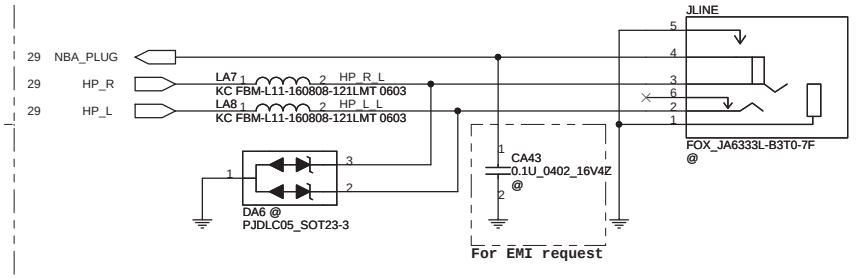
Speaker Connector



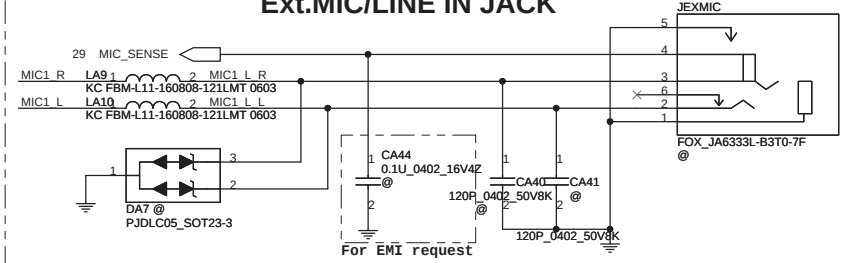
Volume Control



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



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21 PCI_AD[0..31] — PCI_AD[0..31]

21 PCI_CBE#[0..3] — PCI_CBE#[0..3]

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

UB1

OZ601TN_TQFP128~D
PCM@

22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

for EMI request

CLK_PCI_PCM — RB21 10_0402_5% @ — CB14 10P_0402_50V8J @

VCC5# (124)	VPP_PGM (125)	IDSEL SELECT
0	0	AD18
0	1	*AD20
1	0	AD25
1	1	PIN F4

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

PCMCIA Socket

JPCM — SANTA_130675-4_68P @ this is temp. footprint

PVT

SA000026P10 (S IC OZ2210GN-B1 SO 8P)

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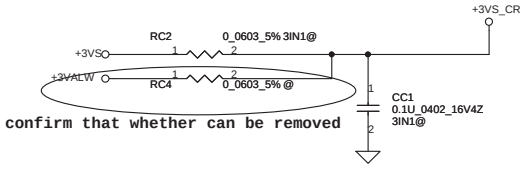
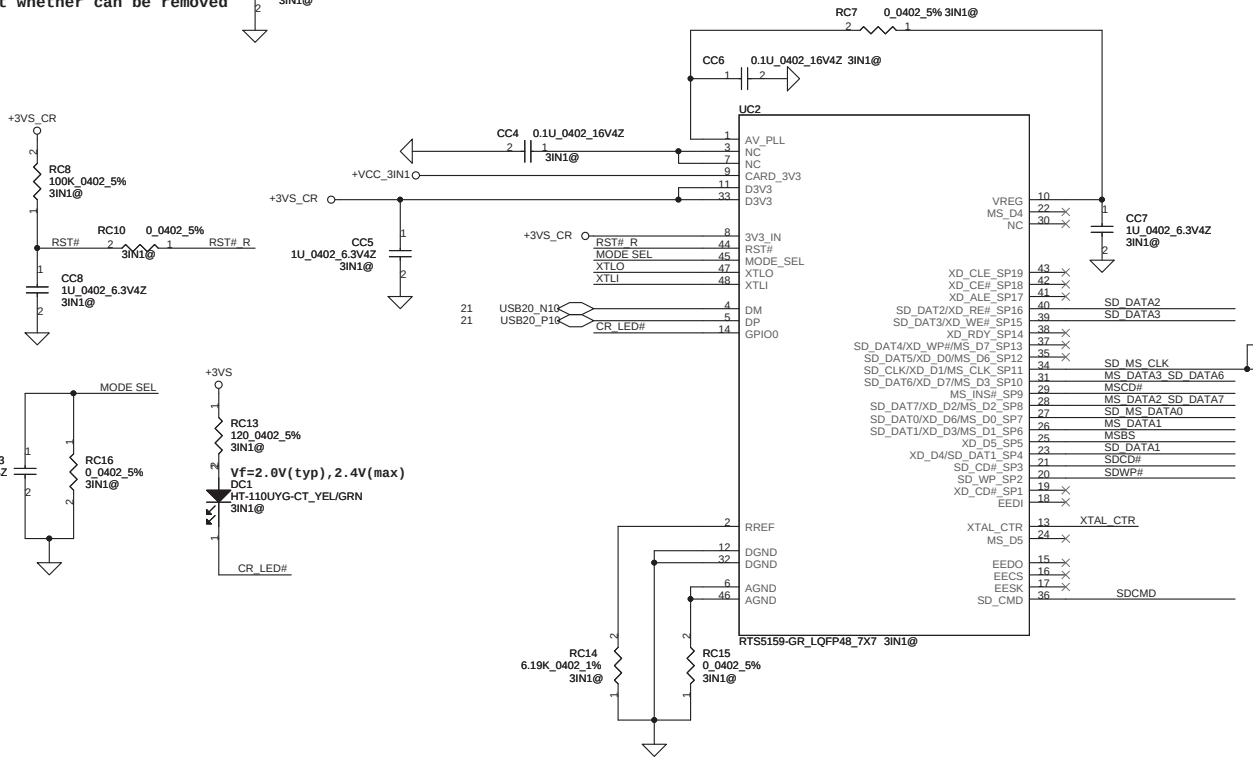
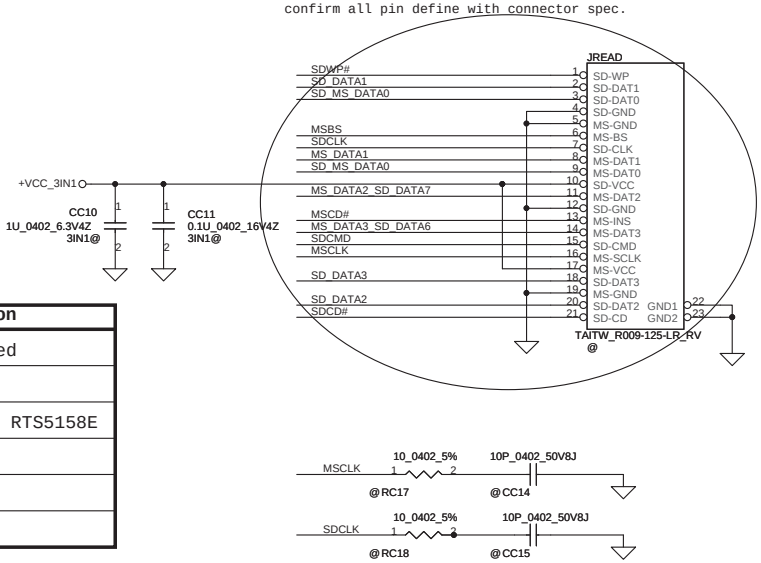
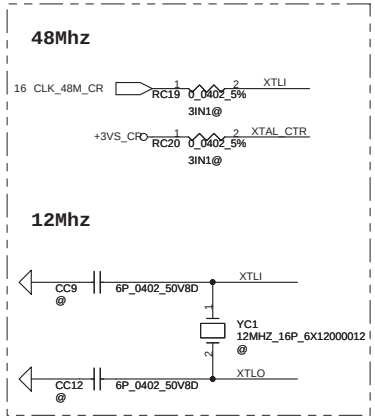




3 in 1 Card Reader





R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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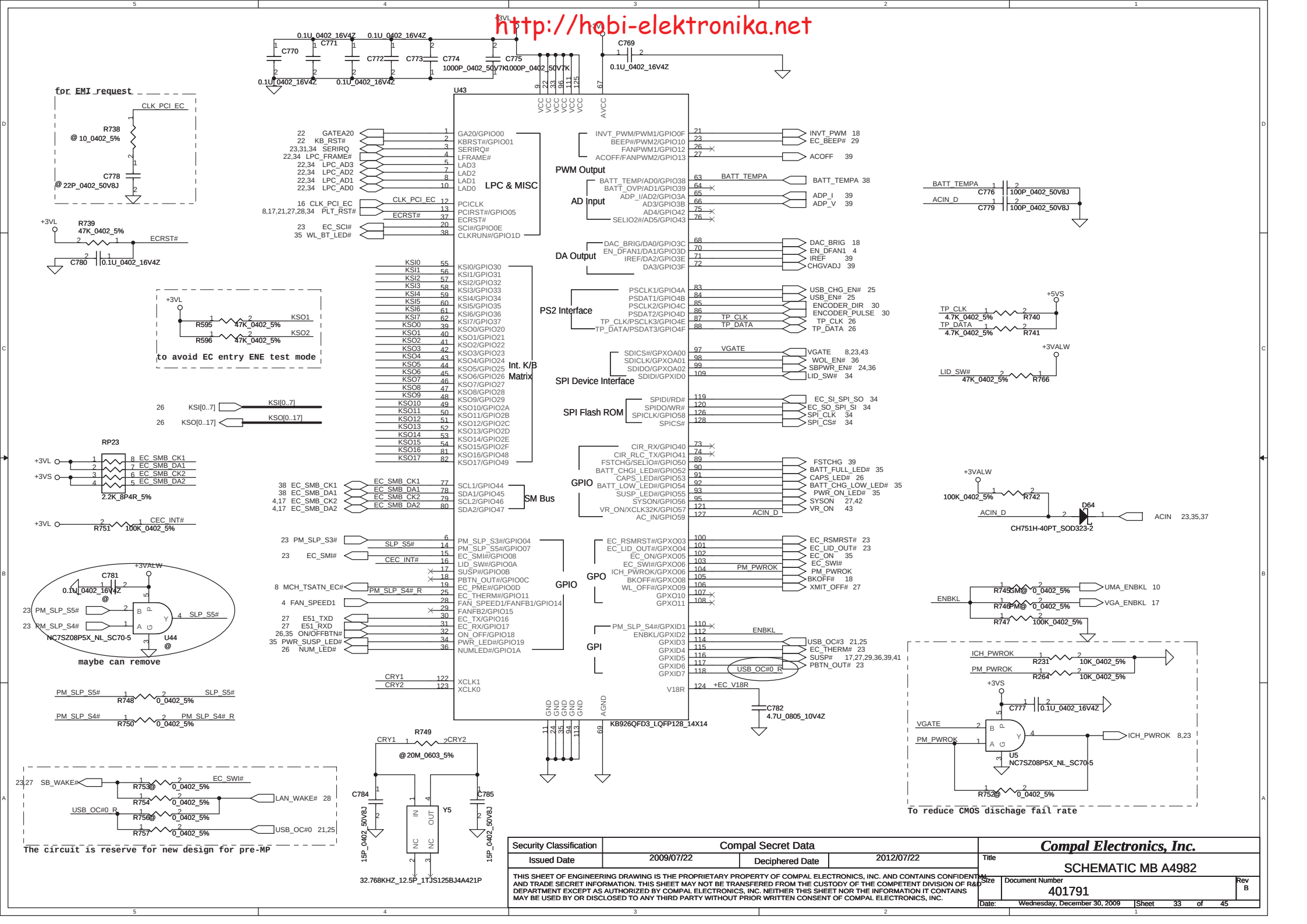

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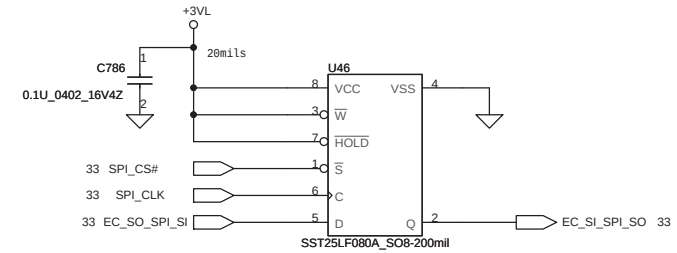
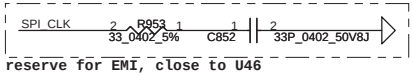
SPI Flash (16Mb*1)

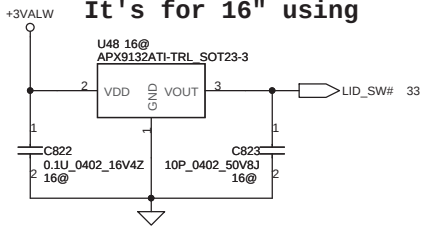




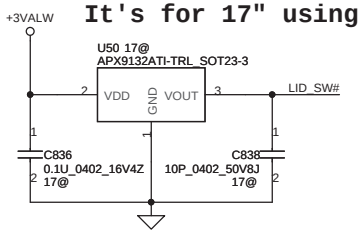
reserve for EMI, close to U46

Lid SW

It's for 16" using

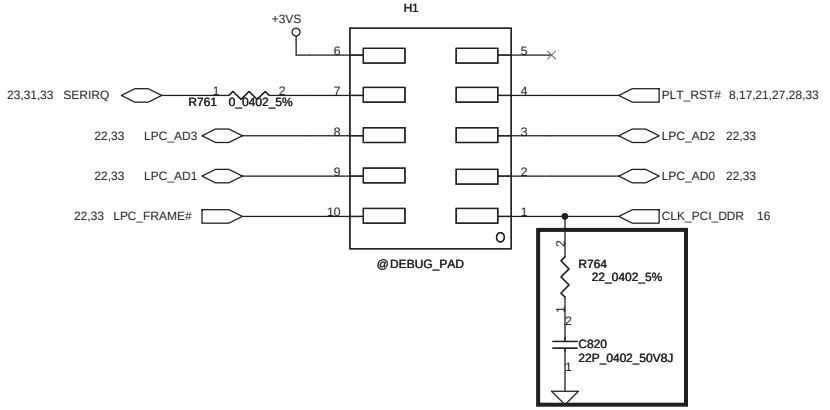


It's for 17" using



I PC Debug Port

Please place the PAD under DDR DIMM.



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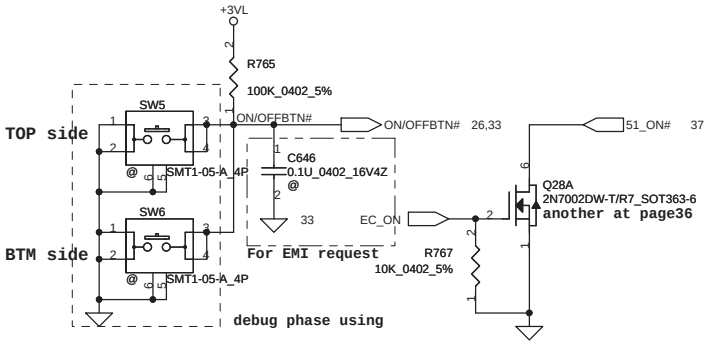
Power Button

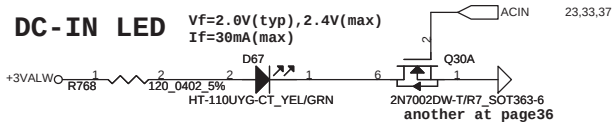


ISPD

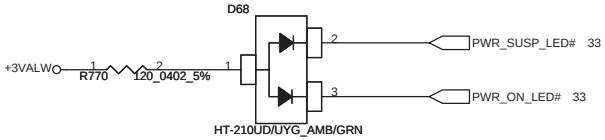
PCB	ZZZ PCB ZKU LA-4982P REV1	NB_PM_R3	U3 CANTIGA PM PMR3@	NB_PM_R1	U3 CANTIGA PM PMR1@
DC-IN 16	PJP1 PJP1 KSWAA45@	NB_GL40_R3	U3 CANTIGA GL40 GL40R3@	NB_GL40_R1	U3 CANTIGA GL40 GL40R1@
DC-IN 17	PJP1 PJP1 KTWAA45@	NB_GM45_R1	U3 CANTIGA GM45 GM45R1@	SB_R1	U9 ICH9-M ES ICH9R1@

DC-IN LED

Vf=2.0V(typ),2.4V(max)
If=30mA(max)

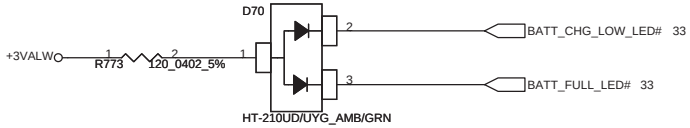


POWER/SUSPEND LED

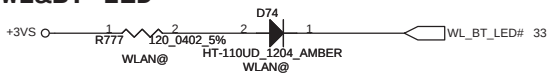


BATT CHARGE/FULL LED

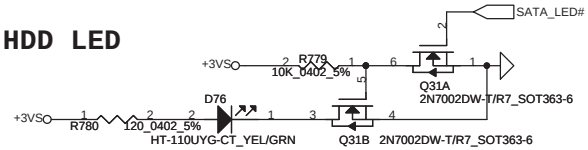
Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)



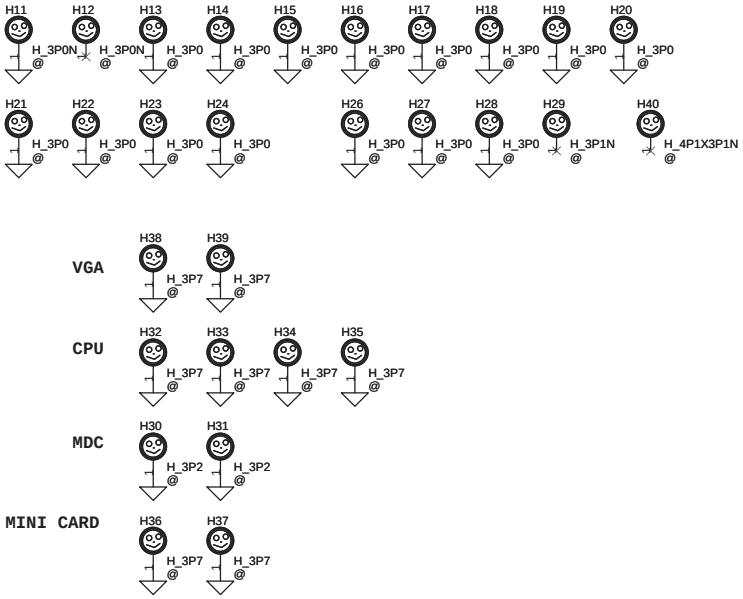
WL&BT LED



HDD LED



Screw Hole



PCB Fedical Mark PAD

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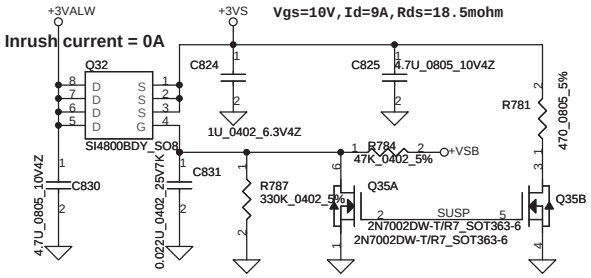
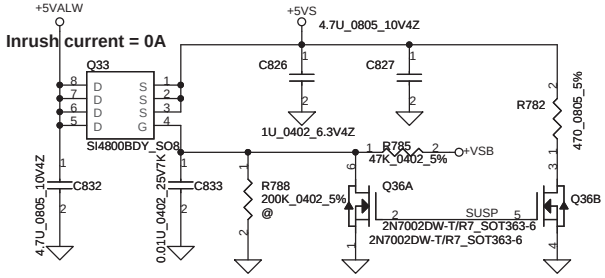
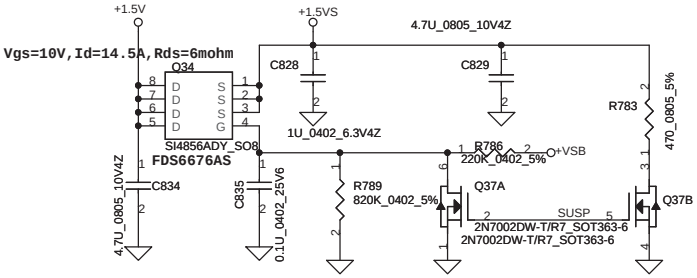
+3VALW TO +3VS



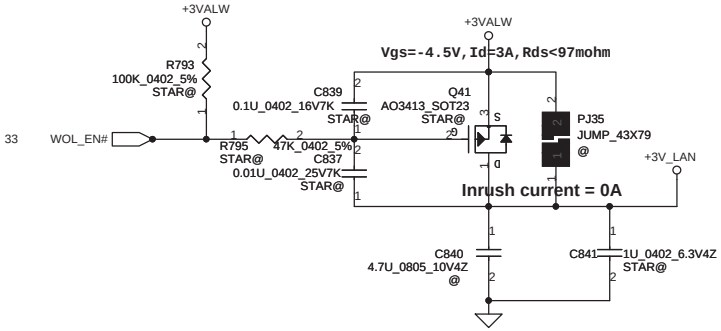
+5VALW TO +5VS



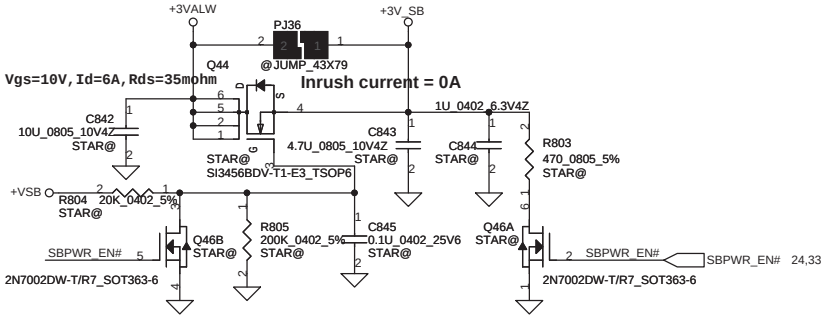
+1.5V to +1.5VS

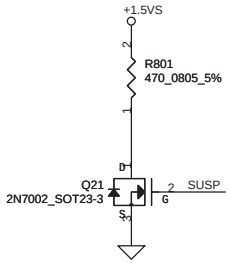


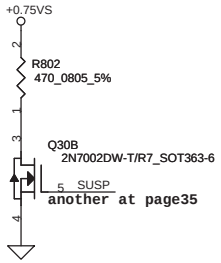
+3VALW TO +3V_LAN

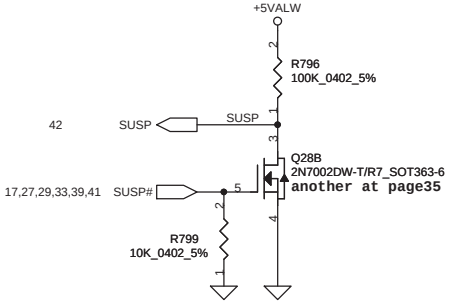


+3VALW TO +3V_SB









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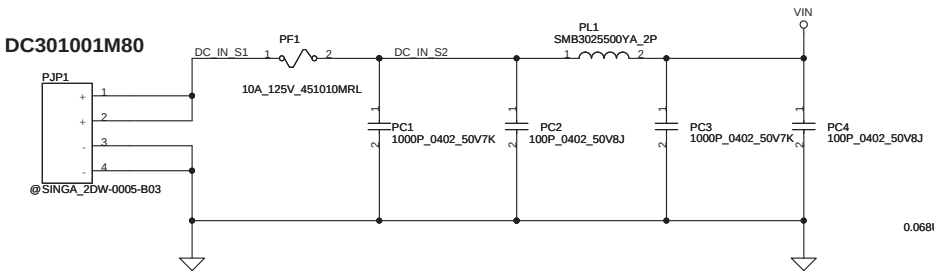
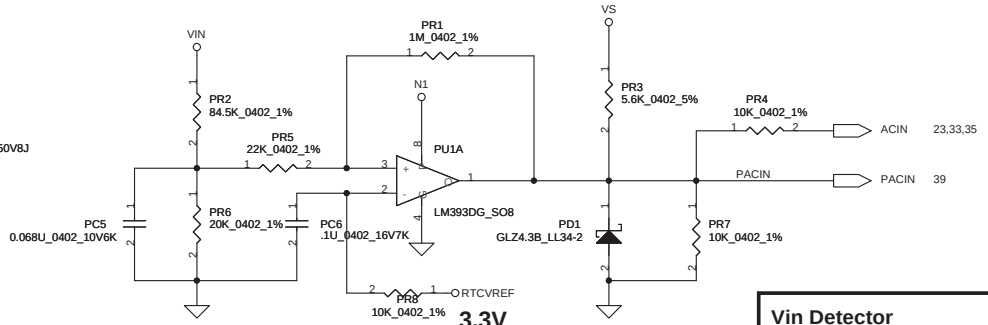
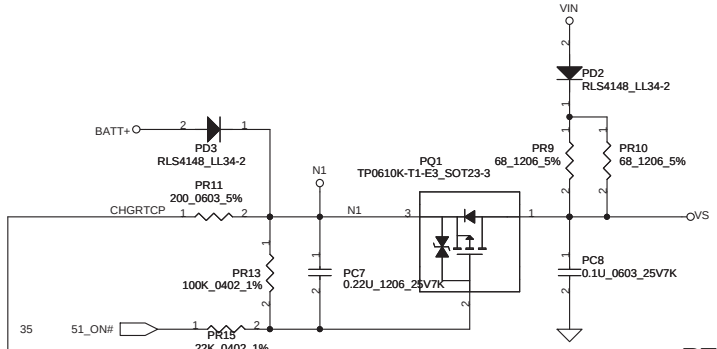
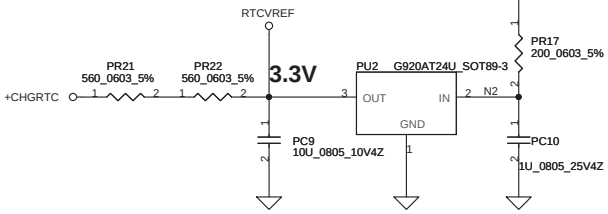




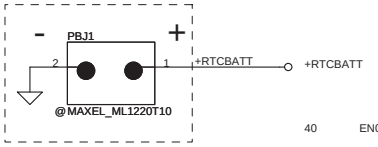
Vin Detector

High	18.384	17.901	17.430
Low	17.728	17.257	16.976

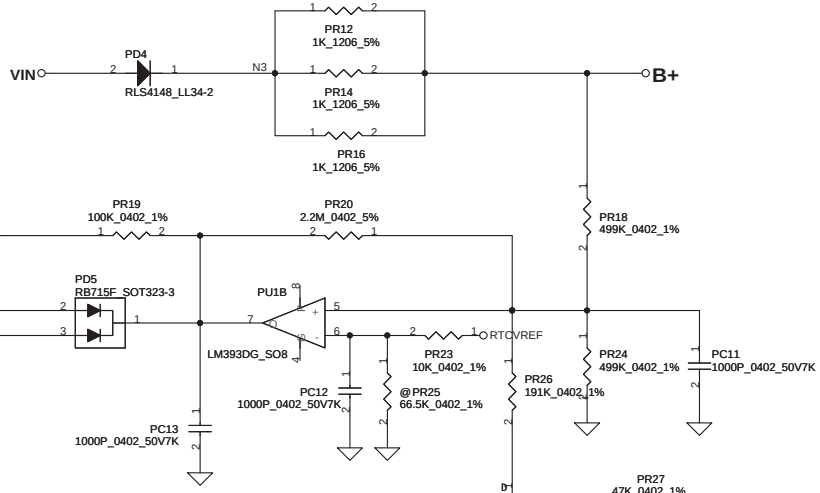




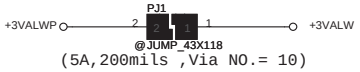
RTC Battery



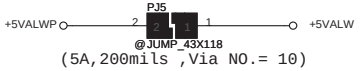
SP093MX0000



Precharge detector
15.97V/14.84V FOR ADAPTOR

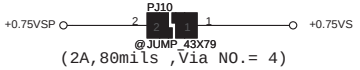


(5A,200mils ,Via NO.= 10)
OCP(min)=7.7A

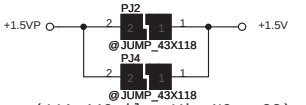


(5A,200mils ,Via NO.= 10)
OCP(min)=7.9A

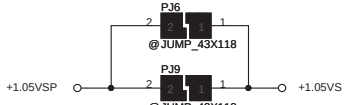
(120mA,40mils ,Via NO.= 1)



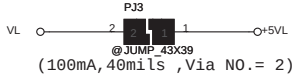
(2A,80mils ,Via NO.= 4)



(11A,440mils ,Via NO.= 22)
OCP(min)=12.97A

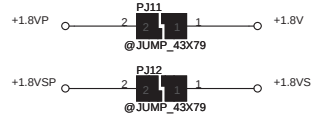


(10A,400mils ,Via NO.=20)
OCP(min)=12.16A



(100mA,40mils ,Via NO.= 2)

(100mA,40mils ,Via NO.= 2)



(2A,100mils ,Via NO.=6)
OCP(min)=2.55A

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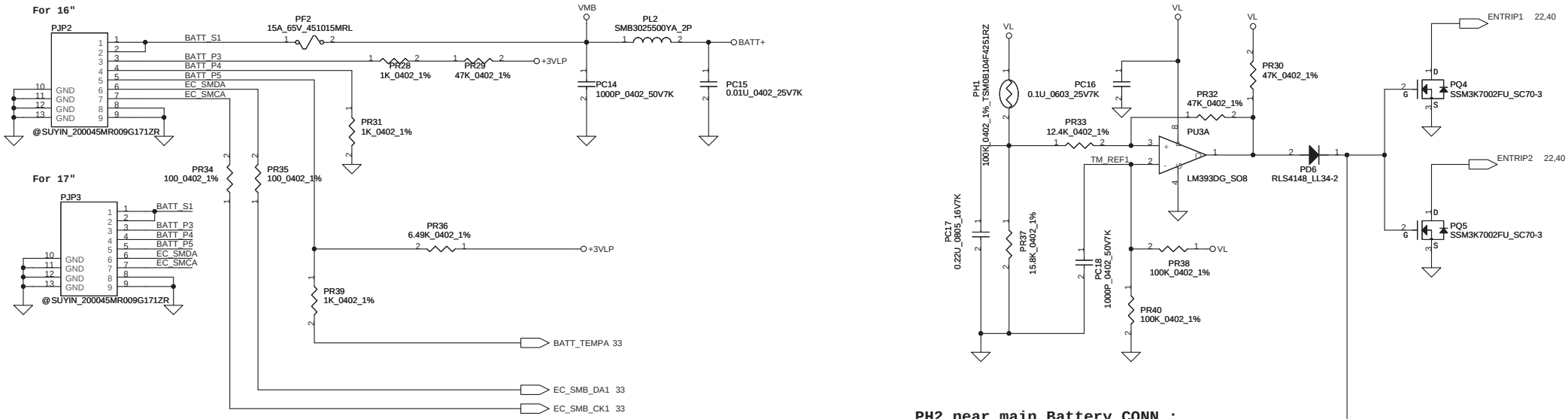
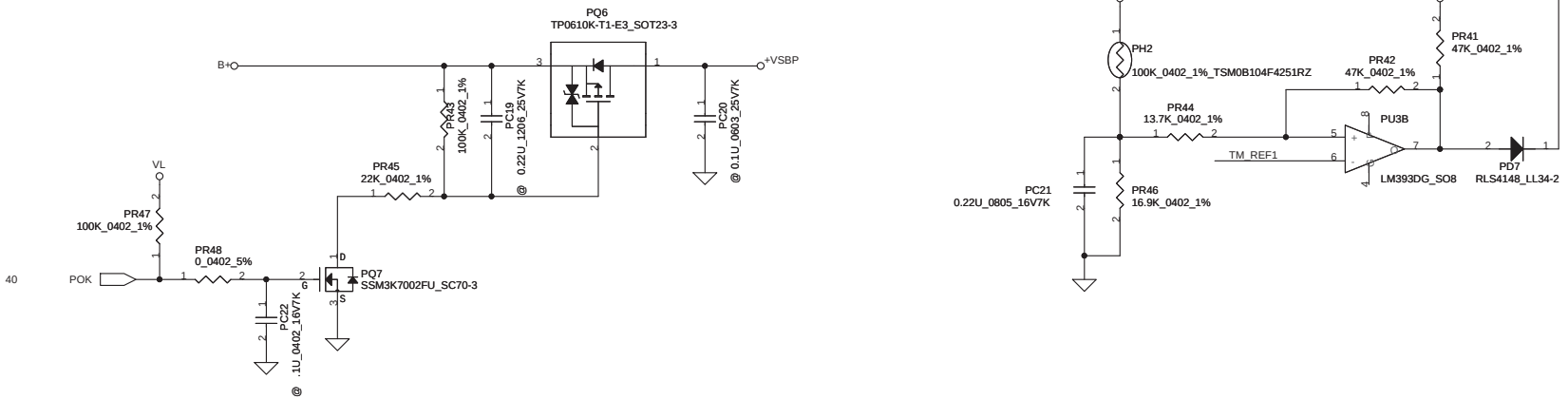
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 53 degree C



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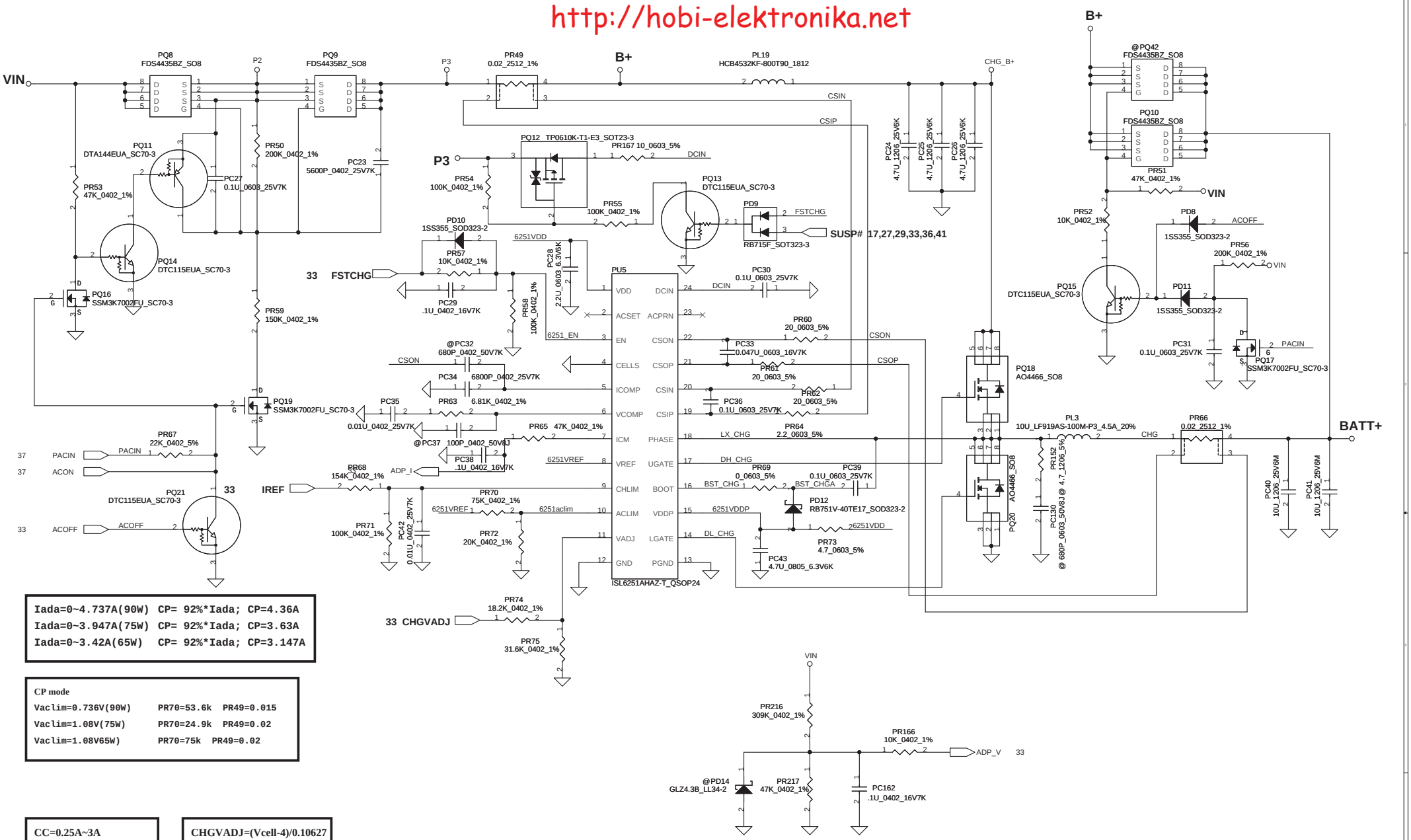


```
Iada=0~4.737A(90W)  CP= 92%*Iada; CP=4.36A
Iada=0~3.947A(75W)  CP= 92%*Iada; CP=3.63A
Iada=0~3.42A(65W)   CP= 92%*Iada; CP=3.147A
```

```
CP mode
Vaclim=0.736V(90W)      PR70=53.6k  PR49=0.015
Vaclim=1.08V(75W)       PR70=24.9k  PR49=0.02
Vaclim=1.08V65W)        PR70=75k  PR49=0.02
```

```
CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV
```

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

Security Classification	Compal Secret Data		
Issued Date	2009/07/22	Deciphered Date	2012/07/22

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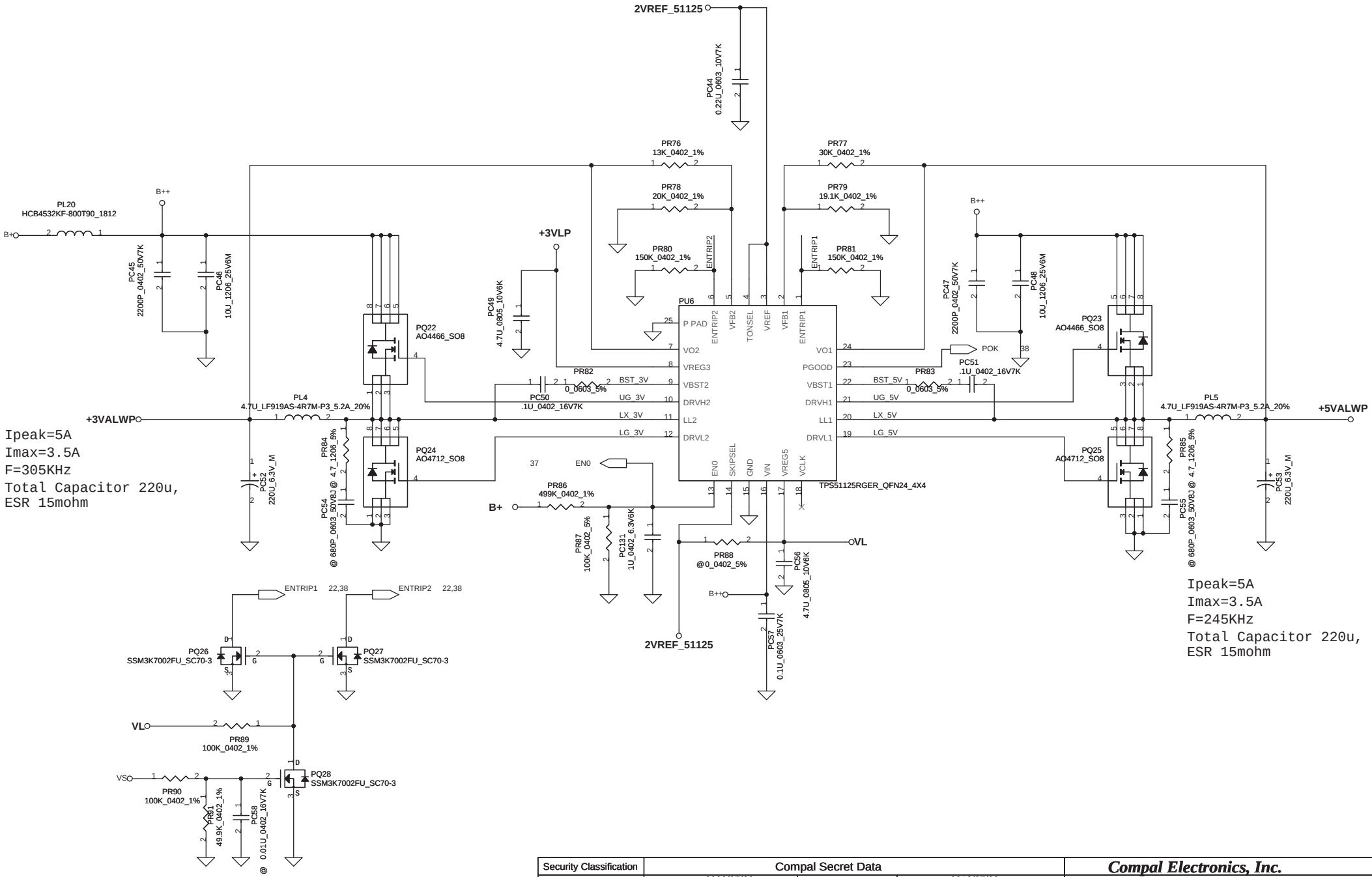

Security Classification	Compal Secret Data		
Issued Date	2009/07/22	Deciphered Date	2012/07/22

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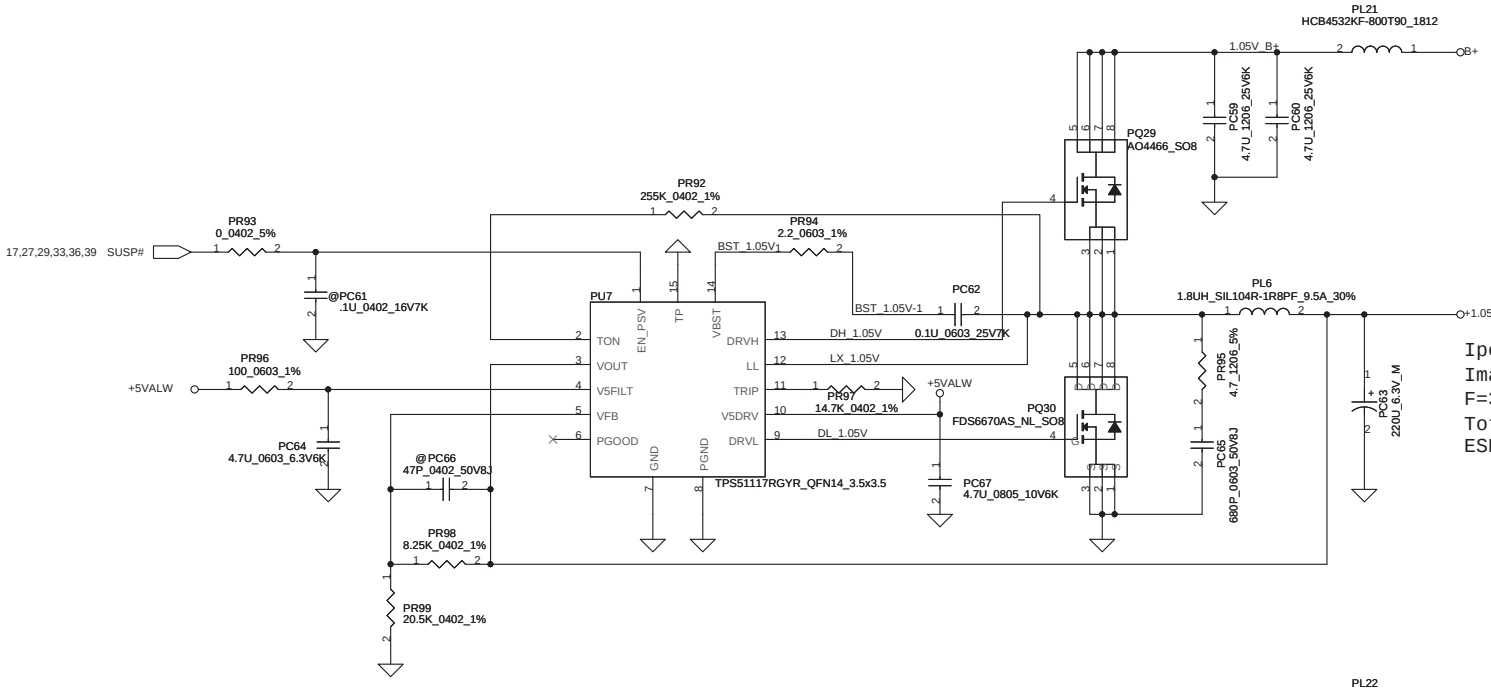
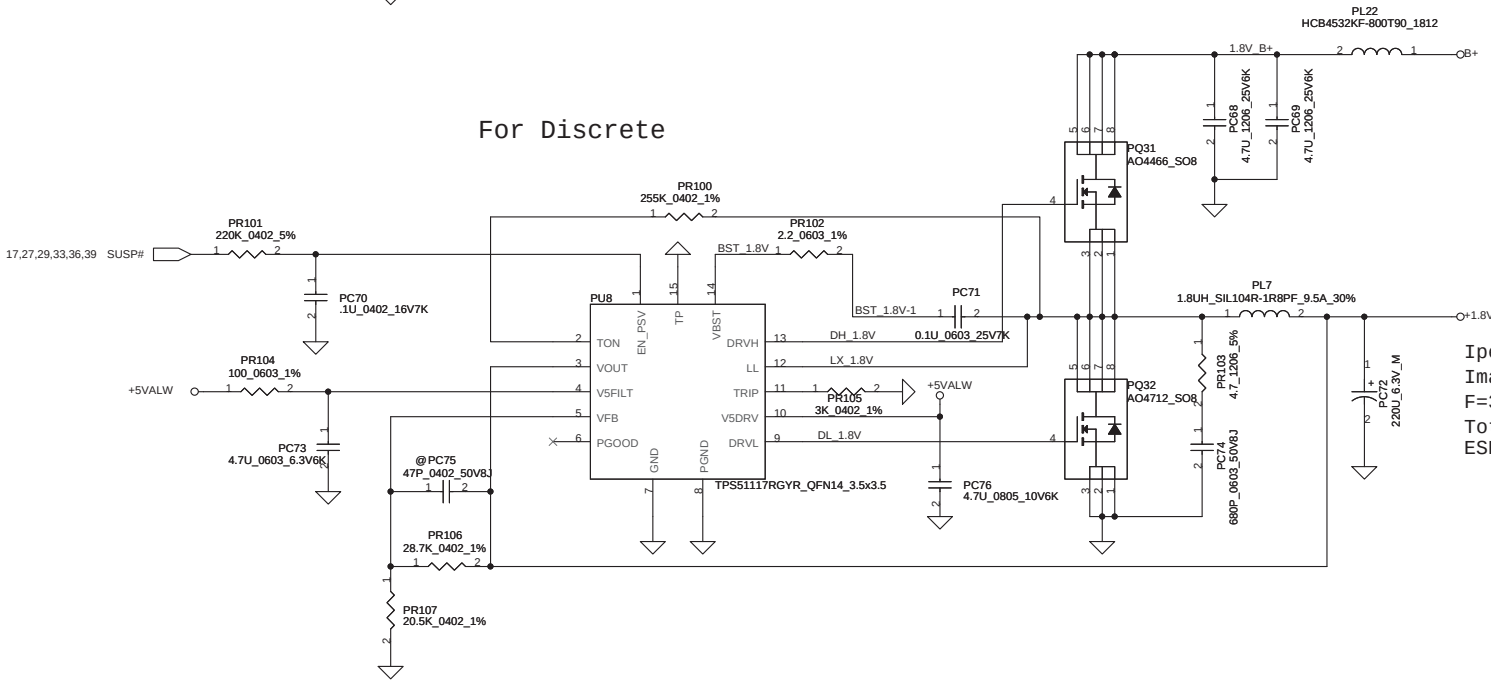


Ipeak=10A
Imax=7A
F=315KHz
Total Capacitor 1430u,
ESR 2.5mohm

For Discrete



Ipeak=2A
Imax=1.4A
F=315KHz
Total Capacitor 220u,
ESR 15mohm

Security Classification	Compal Secret Data		
Issued Date	2009/07/22	Deciphered Date	2012/07/22

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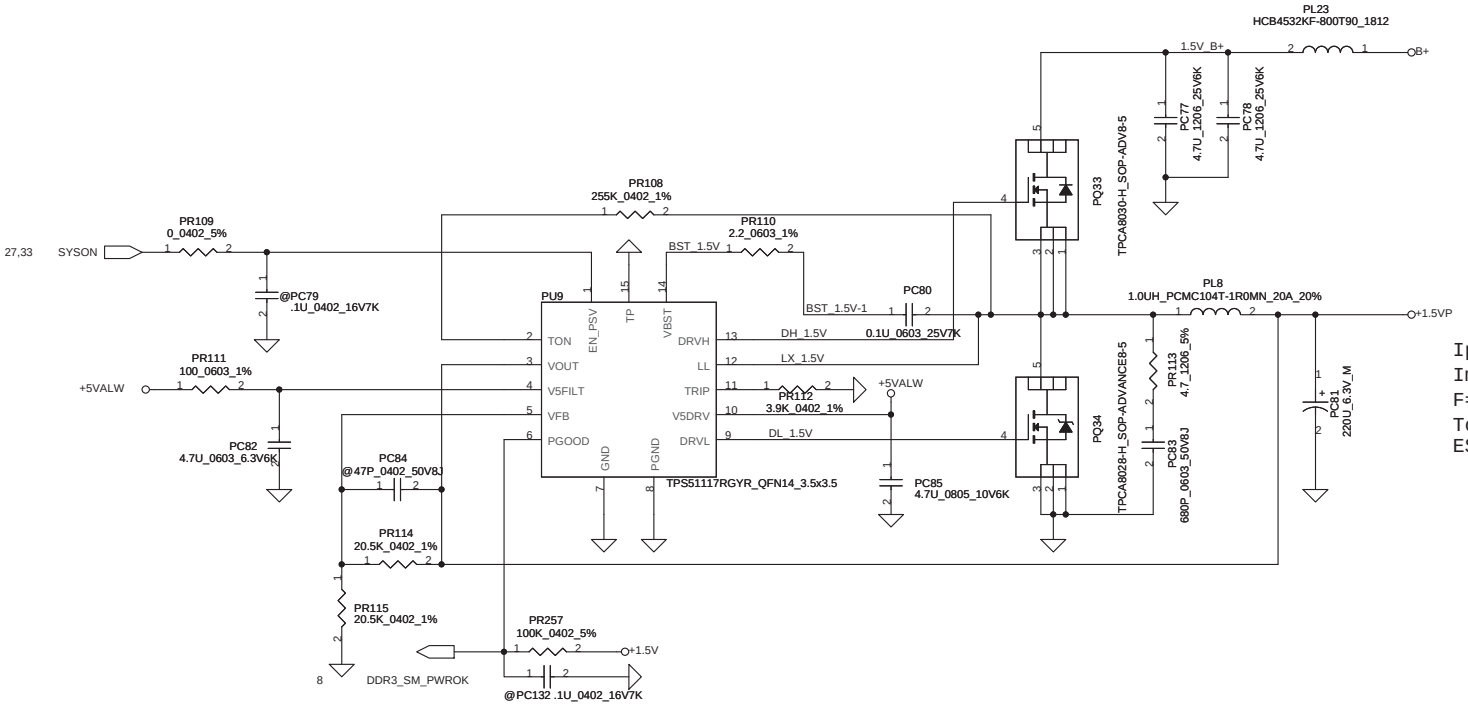
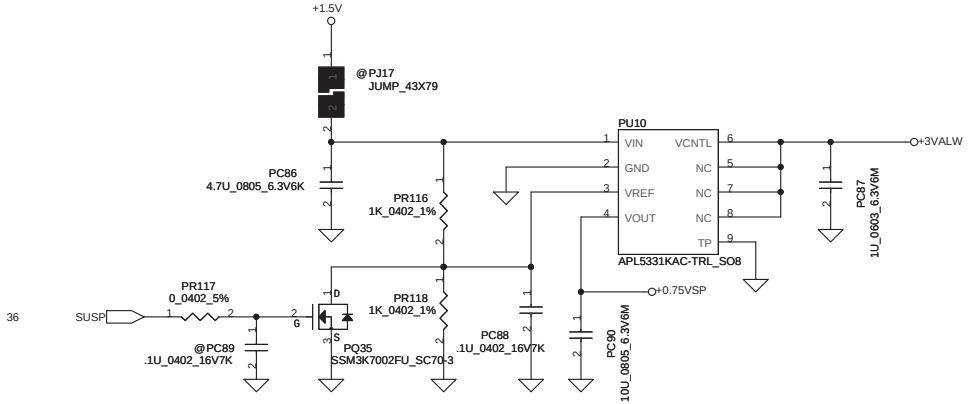
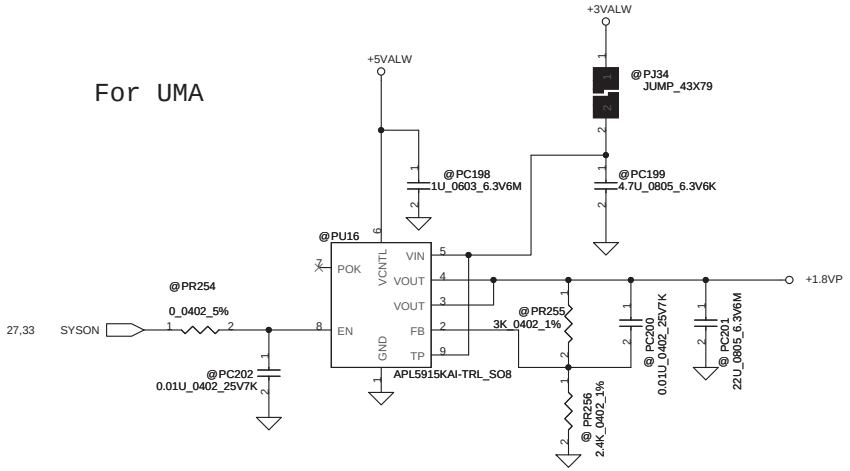


Ipeak=11A
Imax=7.7A
F=315KHz
Total Capacitor 940u,
ESR 4.286mohm

For UMA





Security Classification	Compal Secret Data		
Issued Date	2009/07/22	Deciphered Date	2012/07/22

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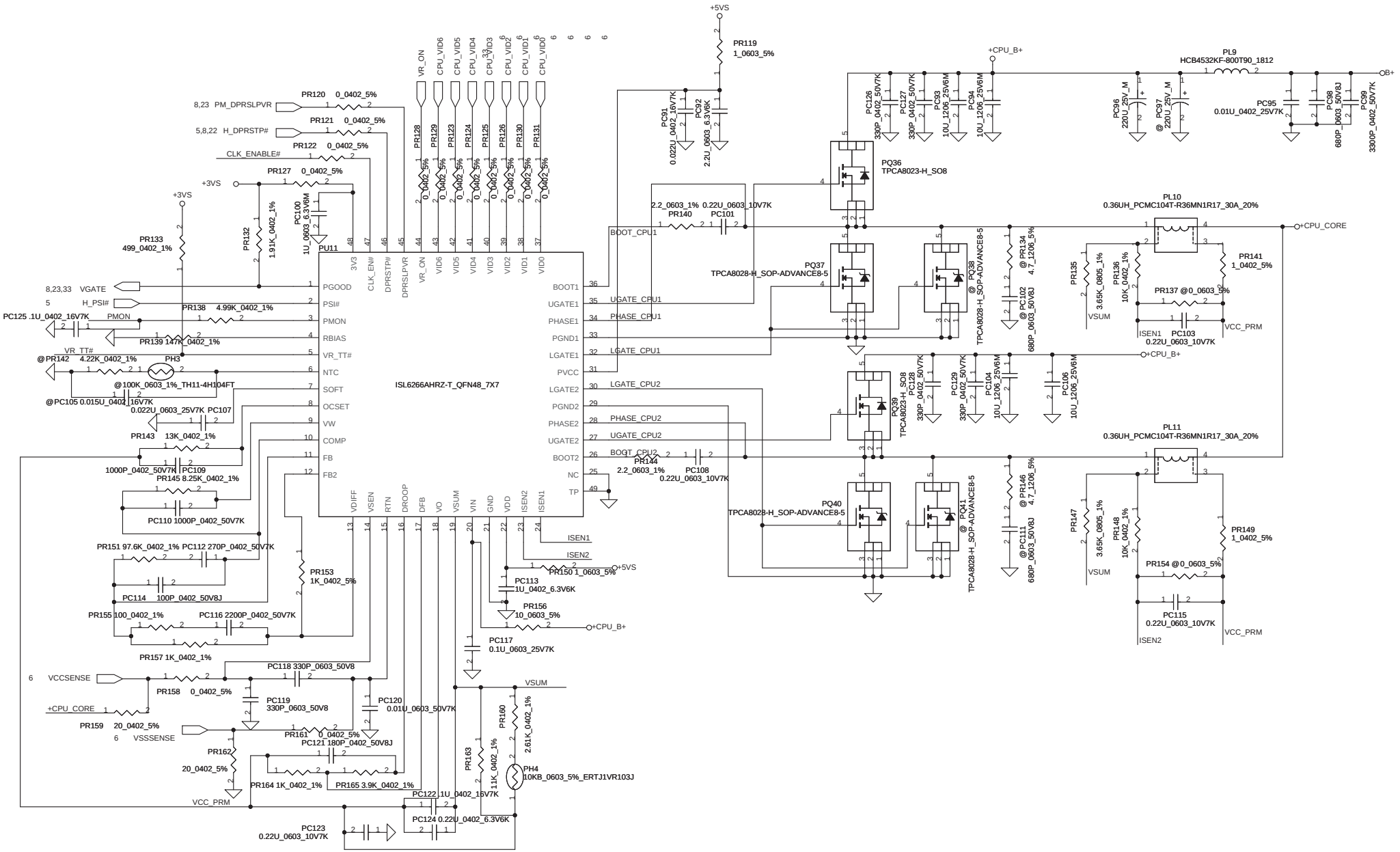

Security Classification	Compal Secret Data		
Issued Date	2009/07/22	Deciphered Date	2012/07/22

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P42-+CPU_CORE	change PU11 ISL6262 to ISL6266	change CPU_CORE IC
			Change PR145 6.81k to 8.25k	modify the parameter for ISL6266
			Change PC112 470P to 270P	
			Change PC114 220P to 100P	
			Change PC116 1000P to 2200P	
			Change PR155 255 to 100	
			Change PC118 0.018U to 330P	
			Change PC119 0.018U to 330P	
			Change PC120 0.018U to 0.01U	
			Change upop component PC96 to PC97	
EVT		P40-1.05V/1.5V	Change PR97 13.7k to 14.7k	Modify trip resistor for ocp
EVT		P41-1.8VP/0.9VSP	Change PR112 15.4k to 18k	Modify trip resistor for ocp
EVT		P38-CHARGER	Add PC162 0.1U	Add detect adapter function
			Add PR216 309k	
			Add PR217 47k	
			Add PD14 GLZ4.3B	
EVT		P38-CHARGER	Change PR49 0.02 to 0.015	Set CP for 90W(X6366051L02)
			Change PR70 24k to 53.6k	
			Change PQ8,PQ9,PQ10,PQ42 FDS4435 to AO4407A	For 90W(X6366051L02)
			Change PR69 2.2 to 0	
EVT		P38-CHARGER	Change PR70 24k to 24.9k	Set CP for 75W(X6366051L01)
DVT		P36-DCIN/DECTOR	Delete PD13	Precharge detector circuit modify
			ENTRIP1 signal change to EN0	
			ENTRIP2 signal change to ACON	
			Change PR23 34k to 10k	
			Add @ lable to PR25 66.5k	
DVT		P39-3VALWP/5VALWP	Add EN0 signal from PU6 pin 13	Precharge detector circuit modify
DVT		P38-CHARGER	Change PR70 24k to 75k	Set CP for 65W(X6366051L03)
DVT		P42-+CPU_CORE	Add PC126,PC127,PC128,PC129 330PF	For EMI solution
			Add PR134,PR146 4.7 ohm	
			Add PC102,PC111 680PF	
			Change PR140,PR144 0ohm to 2.2ohm	
DVT		P38-CHARGER	Change PR71 100k to 120k	Modify charging current for 12 cell
			Change PL3 16U to 10U	
DVT		P42-+CPU_CORE	Change PR145 8.25k to 11.3k	Modify switching frequency
PVT		P38-CHARGER	Change PL3 Part NO SH000003080 to SH162100M10	SH000003080 footprint is wrong
PVT		P36-DCIN/DECTOR	Change PU1 8 pin connect to N1	For precharge function
PVT		P38-CHARGER	Add PR166 10k Ohm	Modify ADP_V circuit(2009/02/18)
PVT		P38-CHARGER	Remove PD14	Modify ADP_V circuit(2009/02/18)
PVT		P38-CHARGER	Change PR74 18.2k to 15.4k	Change CHGVADJ voltage dividers value(2009/02/18)
PVT		P42-+CPU_CORE	Change PC126,PC127,PC128,PC129 (SE068331K80) to (SE00000FD80)	Change temperature tolerance K(10%) to J(5%)(2009/02/23)
PREMP		P38-CHARGER	Add PR167 10_0603_5%	Add 10 Ohm to DCIN circuit(2009/03/12)
PREMP		P38-CHARGER	Add PL19 HCB4532KF-800T90_1812 and delete PJ12	Add bead on B+ node(2009/03/12)
PREMP		P39-3VALWP/5VALWP	Add PL20 HCB4532KF-800T90_1812 and delete PJ13	Add bead on B+ node(2009/03/12)
PREMP		P40-1.05V/1.5V	Add PL21 HCB4532KF-800T90_1812 and delete PJ14	Add bead on B+ node(2009/03/12)
			Add PL22 HCB4532KF-800T90_1812 and delete PJ15	Add bead on B+ node(2009/03/12)
PREMP		P41-1.8VP/0.9VSP	Add PL23 HCB4532KF-800T90_1812 and delete PJ16	Add bead on B+ node(2009/03/12)
PREMP		P39-3VALWP/5VALWP	Change PR79 19.6k to 19.1k	Modify 5V to 5.14V(2009/04/08)
PREMP		P38-CHARGER	Change PR65 100 to 47k	For CPU throtting setting(2009/04/08)
PREMP			Change PR82,PR83,PR94,PR102,PR110 SD014000080 (0 +-1% 0603) to SD013000080 (0 +-5% 0603)	Component not haven 0_+-1%, change to 0_5%(2009/04/08)
PREMP		P42-+CPU_CORE	Change PC126,PC127,PC128,PC129 (SE0000FD80) to (SE074331K80)	Change property NPO to X7R(2009/04/08)
PREMP		P41-1.05VSP/1.8VP	Change PR96 422 ohm to 100 ohm	Avoid 2nd source RT8209B can not power on(2009/07/27)
			Change PC64 1U to 4.7U	
PREMP		P42-1.5VP/0.75VSP	Change PR111 422 ohm to 100 ohm	Avoid 2nd source RT8209B can not power on(2009/07/27)
			Change PC82 1U to 4.7U	
PREMP		P42-1.5VP/0.75VSP	Change PR112 14.7k to 3.9k	Set 1.5V OCP to 13.25A(2009/07/27)
PREMP		P40-3VALWP/5VALWP	Change PC52, PC53 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
PREMP		P41-1.05VSP/1.8VP	Change PC63, PC72 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
PREMP		P42-1.5VP/0.75VSP	Change PC81 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
MP		P42-1.5VP/0.75VP	Change High,Low side Mosfet and Choke.	(2009/06/18)
			Add bead on B+ node	
MP		P38-BATTERY CONN / OTP	Change PR33 13.7k to 12.4k	Change resistor for OTP (2009/09/01)
			Change PR37 15.4k to 15.8k	

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PIR (Product Improve Record)

KSWAA LA-4982P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/22	15	delete C604~C610,C643~C645	Change reference plane of control from VCC to GND
2	7/24	35	change PCB P/N to DAZ07300200	For load BOM
3	7/27	14	add CD45 and un-mount CD17,CD39 on DDR 1.5V	design change

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